Welcome to the NEREID

2nd General Workshop

April 6th- 7th, 2017

NanoElectronics Roadmap for Europe: Identification and Dissemination

Location: Divani Caravel Hotel Vassileos Alexandrou 2, 16121 Athens (Greece)

At A Glance: NEREID
H2020 NanoElectronics Roadmap for Europe: Identification and Dissemination
(GRANT AGREEMENT N°685559, Coordination and support action*)*
Duration: 36 months
Start Date: 16 November 2015 Project website*: https://www.nereid-h2020.eu/*

EUROPEAN COMMISSION COORDINATION
Francisco J. Ibáñez, Project Officer,
Directorate-General for Communications Networks, Content and Technology Unit A4 – Components

PROJECT COORDINATION
Francis Balestra, Project Coordinator, Grenoble INP
Enrico Sangiorgi, Project Technical Coordinator, SINANO Institute
Livio Baldi, Project Co-industrial Leader, Consultant

ABSTRACT
The objective of this project is to elaborate a new roadmap for Nanoelectronics, focused on the requirements of European semiconductor and applications industry, and the advanced concepts developed by Research centers in order to achieve an early identification of promising novel technologies, and cover the R&D needs all along the innovation chain.
The final result will be a roadmap for European micro- and nano-electronics, covering all TRL, with a clear identification of short, medium and long term objectives. The roadmap will be divided into main technology sectors and include also cross-functional enabling domains.
A proper dissemination of results will take place through the close relationship of the project with the leading European organizations in the field of micro- and nano-electronics, and sanity checks are foreseen during the project with the users' world.

Workshops: Three major General Workshops will be organised starting with a General Workshop (April 12-13th, 2016 in Grenoble) with a large participation of technology users in order to better define the technology roadmap in terms of applications requirements. General Workshops will involve all technology sectors, and allow for synergies among different topics and roadmap coordination. Specific application requirements will also be included, based also on the progress of the roadmap and the evolution of technology.

Consortium of NEREID

	Organisation	short name	country
1	INSTITUT POLYTECHNIQUE DE GRENOBLE	GRENOBLE INP	France
2	INSTITUT SINANO ASSOCIATION	INSTITUT SINANO	France
3	edacentrum GmbH	EDAC	Germany
4	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
5	FRAUNHOFER GESELLSCHAFT ZUR FORDERUNG DER ANGEWANDTEN FORSCHUNG EV	Fraunhofer	Germany
6	FUNDACIO INSTITUT CATALA DE NANOCIENCIA I NANOTECNOLOGIA	ICN2	Spain
7	INTERUNIVERSITAIR ICROELECTRONICACENTRUM IMEC VZW	IMEC	Belgium
8	CONSORZIO NAZIONALE INTERUNIVERSITARIO PER LA NANOELETTRONICA	IUNET	Italy
9	COMMISSARIAT A L ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES	CEA	France
10	POLITECNICO DI TORINO	POLITO	Italy
11	UNIVERSITY COLLEGE CORK - NATIONAL NIVERSITY OF IRELAND, CORK	Tyndall-UCC	Ireland
12	Teknologian tutkimuskeskus VTT Oy	VTT	Finland
13	AENEAS	AENEAS	France

General agenda

DAY1: Thursday April 6th, 2017

Session1 8:30 – 13:00 New Applications experts or new presentations - *Room VERGINA*

8:30 – 8:45 *Introduction (Francis Balestra)*

8:45 – 9:25 ***Orange*** *for Nanotechnologies: an opportunity for green networks: Thomas Rivera*

9:25 – 10:05 ***SCHNEIDER Electric*** *for Energy: Miao-Xin Wang*

10:05 – 10:45 ***IMEC*** *for Health: Maaike Op de Beeck*

10:45 – 11:05 Coffee Break (Vergina Foyer)

11:05 – 11:45 ***Bosh*** *for Automotive: Christian Silber*

11:45 – 12:25 ***GEMALTO*** *for Security: Jean-Pierre Tual*

12:25 – 13:00 SINTEF *for IoT: Ovidiu Vermesan*

13:00 – 14:00 Lunch (Room Constantinople)

Session2 14:00 – 18:00 Feedback from the Domain Workshops by Tasks & WP leaders – Interactions with Application experts – Discussions – *Room VERGINA*

14:00 – 14:15 *Introduction (E. Sangiorgi)*

14:15 – 14:55 *Domain workshop "Nanoscale FET" (Task 3.1) Francis Balestra*

14:55 – 15:35 *Domain workshop "Connectivity" (Task 3.2) Didier Belot*

15:35 – 16:15 *Domain workshop "Smart Energy" (Task 4.2) Wolfgang Dettmann/Gaudenzio Meneghesso*

16:15 – 16:40 Coffee break (Vergina Foyer)

16:40 – 17:20 *Domain workshop "Energy for Autonomous system" (Sub TaskT4.2) Gustavo Ardila*

17:20 – 18:00 *Domain workshop "Smart Sensors" (Task 4.1) Montserrat Fernandez-Bolanos*

19:00- 22:00 Cocktail Dinner (Athens View)

DAY2: Friday April 7th, 2017

Steering Committee Meeting 8:00- 9:00 (Room Vergina)

Session3 9:00 – 12:10 Feedback from the Domain Workshops by Tasks & WP leaders – Interactions with Application experts – Discussions – *Room VERGINA*

9:00 – 9:15 Introduction (E. Sangiorgi)

9:15 – 9:55 Domain workshop WP2 Beyond CMOS "Emerging devices" (Task 2.1) Jouni Ahopelto / Clivia Sotomayor-Torres

9:55 – 10:35 Domain workshop "System Design" (Task 5.1) Danilo DeMarchi

10:35 – 10:50 Coffee Break (Vergina Foyer)

10:50 – 11:30 Domain workshop "Heterogeneous Integration" (Task 5.2) Georgios Fagas

11:30 – 12:10 Domain workshop WP6 "Equipment & Manufacturing Science" Markus Pfeffer

12:10-13:00 Lunch (Room Constantinople)

Session4 13:00 – 15:30 IRDS Presentations - Conclusions and next steps (F. Balestra) – *Room VERGINA*

Paolo Gargini (IRDS)– "General presentation of IRDS" IRDS - 20mn

Mustafa Badaroglu (Qualcomm) "More Moore roadmapping activities in IRDS" – 20mn

Convergence Technologies – Applications

Draft of preliminary Roadmap and next steps

15:30 – 16:30 Farewell Coffee (Vergina Foyer)

Advisory Board Meeting 17:00- 19:30 – Room VERGINA