NanoElectronics Roadmap for Europe: Identification and Dissemination

Draft of the Roadmap at M18

ABSTRACT:

The Nereid Nanolectronic Roadmap takes into account the specificity of the European industrial and academic landscape, and is very important to better coordinate academic and industrial research for equipment, semiconductors and application developments. It will be used as input for future research programmes at European and National levels in order to join our effort to overcome the main nanoelectronic challenges and put the EU at the forefront of future technological developments.

The project solicits application and technology experts from leading industrial and academic research organizations to participate to General and Domain (WPs) Workshops while in return covering their travel expenses. These Workshops allow the consortium to better define the technology roadmap according to application requirements (in the fields of Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing) and technology evolution (Advanced Logic and Connectivity, Functional diversification, Beyond-CMOS, Heterogeneous Integration and System design, Equipment, Materials and Manufacturing Science). Structured discussion and debate provide the convergence between applications and technologies.

This common work between technology and application experts leads to the early identification of the most promising technologies needing additional R&D actions, which could be very useful for the future electronic products of European companies leading to a strong impact on the European economy and society.

This work has been achieved within the project NEREID, a Cooperation and Support action that receives funding for three years from the European Union's Horizon 2020 research and innovation programme under grant agreement No 685559.

https://www.nereid-h2020.eu

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I General Introduction (main objectives of NEREID roadmap)

The H2020 NEREID Coordination and Support Action (n° 685559) entitled "NanoElectronics Roadmap for Europe: Identification and Dissemination" has been funded by the European Commission following at the Nanoelectronics call "H2020-ICT-2015 Generic micro- and nano-electronic technologies" and has been launched at the European Nanoelectronics Forum in Berlin in December 2015 for a duration of 3 years.

The objective of this project is to elaborate a new Roadmap for Nanoelectronics, focused on the requirements of European semiconductor and applications to address societal challenges, and the advanced concepts developed by Research Centres and Universities in order to achieve an early identification of promising novel technologies covering the R&D needs all along the innovation chain. The final result will be a roadmap for European micro- and nano-electronics, with a clear identification of medium and long term objectives. The roadmap is divided into main technology sectors: Advanced Logic (including Nanoscale FETs and Memories) and Connectivity, Functional diversification (Smart Sensors, Smart Energy, Energy for Autonomous Systems), Beyond-CMOS (Emerging devices and Computing Paradigms), Heterogeneous Integration and System design, Equipment, Materials and Manufacturing Science, and also includes cross-functional enabling domains.

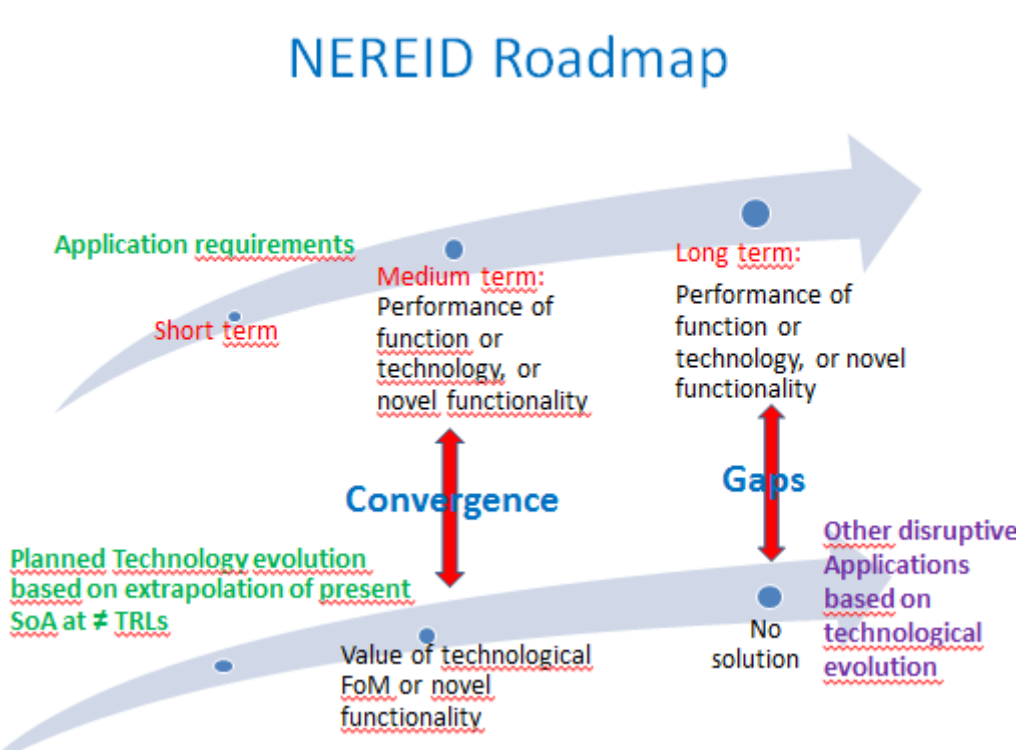
Understanding the dependencies between short/medium term (e.g. More Moore and More than Moore) and long/very long term (e.g. Beyond CMOS) activities is also very important to speed-up technology transfer between academia and industry using disruptive technologies leading to possible new large future markets.

The NEREID Roadmap, focused on medium and long term time horizons, is complementary to the AENEAS Strategic Agenda and the ECSEL MASRIA, which are focusing on shorter terms. NEREID has some commonalities and is developing joint collaboration with the new International IRDS Roadmap especially in the fields of More Moore, Beyond CMOS and computing systems, but is also complementary to IRDS with very important NEREID activities in the More than Moore domain (e.g. Smart Sensors, Smart Energy, Energy Harvesting), which is a sound European competence, leading to a large diversity of electronic systems useful for many applications. In the More Moore field, there are also strong interests in Europe for specific activities dealing with very low power systems, leading to possible disruptive applications for instance for future IoT systems.

Therefore, the Nereid Roadmap takes into account the specificity of the European industrial and academic landscape, and will be very important to better coordinate academic and industrial research for equipment, semiconductors and application developments, as well as serving as the input for future research programmes at European and National levels in order to join our efforts to overcome the main Nanoelectronic challenges and put the EU at the forefront of future technological developments.

II Roadmapping Process

The project supports the participation of many application and technology experts, coming from leading research actors in industry and academia, to workshops during which they present the state-of-the-art. Three major general Workshops and many Domain Workshops (for WPs and Tasks) are organized with a large participation by application experts/technology users and technological experts (more than 100 experts) in order to better define the technology roadmap in terms of applications requirements and technology evolution, and discuss the convergence between applications and technologies, as shown in the figure below:



The proposed idea is that the scenarios of evolution of the products/applications will result in performance evolution scenario for the functions, which could be generic enough to apply to many products. The next step is then to derive, from the evolution of functions, the evolution of the underlying technologies and devices using the expertise of technology experts. Insights on future technology evolution and availability can also prompt new ideas for disruptive products and applications, which are discussed in Domain Workshops and also presented by technology experts during the General Workshops.

This common work between technology and application experts is leading to the early identification of the most promising technologies needing additional R&D activities in order to become useful for the future electronic products of European companies, thus leading to a strong impact on the European economy and society.

III Application domains and Societal benefits of a new European Roadmap

We have proposed to start from the different very important European application areas (Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing) in order to define the roadmap.

We have therefore invited potential users of the nanoelectronic technologies in the NEREID General Workshops to provide insight on the technology requirements in terms of both performance and timescale for the future applications and/or (generic) functions envisioned by their Companies.

These requests are then used by technology experts for the identification of the most promising technologies and functions that can satisfy the functionalities and performances needed for these different applications.

Societal benefits:

Future electronic systems will play a vital role in all of the very important European application areas mentioned above. The world of connected objects and the development of “Smart Everything Everywhere”, with huge future markets, imply the development of dedicated technologies like low power

devices and the development of many new functionalities for sensing, computing, communicating, energy harvesting, etc.

The use of renewable energy sources is becoming one of the most important topics in our society. Among the benefits, it is possible to envisage the development of autonomous, wearable, or even implantable sensor nodes for health applications or environmental monitoring for instance. The development of "green" materials, replacing toxic/rare materials used nowadays, is also of paramount importance for future sustainable systems and society.

On the other hand, the estimated energy savings potential that can be achieved by introducing power electronics into systems is enormous, estimated at more than 25% of the current electricity consumption in the EU countries.[1] Since power electronics is a key technology in achieving a sustainable energy society, the demand for power electronics solutions will show significant growth in the coming decades.

In the health sector, the strong incidence of chronic diseases, such as cancer, cardiovascular diseases, obesity, diabetes, autoimmune and psychiatric diseases will increase the demand for diagnostic devices (activity trackers, body monitors and multi-parameter real-time sensing) and for most devices a low-cost, portable and fast diagnostic solution does not exist in the market yet. Moreover, devices could also serve to detect the incidence of health hazards caused by pollution (air quality, water and food monitoring, …) and address rising concerns about health and well-being. These emerging medical devices (wearable sensors, implantable sensors and others) would benefit healthcare facilities and simplify the acceptance of personalized, more-efficient medicines.

The connectivity functions will be everywhere in the future connected world, from the physical world, things and the persons, the autonomous objects, factory 4.0, to the cloud.

An early consideration of all these trends, which are taken into account in the NEREID Roadmap, will be beneficial to the EU. NEREID will lead to disruptive technologies and applications and many new markets, strengthening the international position of the European economy and having a great potential impact on the European society.

IV Interactions with other international activities

The activities of NEREID account from the international context of roadmapping through the Advisory Board that include personalities involved in USA and Asia in similar activities. They are proving systematic feedback about the coherence and complementarity of NEREID with the global context, while constructively recognizing the European focus on priorities, specific to NEREID.

On the other hand, NEREID has concretely started and implemented a series of actions of reciprocal benefits with the International Roadmap of Devices and Systems (IRDS) supported by IEEE organization. In fact, almost simultaneously with the launch of NEREID, in May 2016, IEEE announced the formation of the IRDS under their sponsorship to addresses the mapping of the ecosystem of newly reborn electronics industry. The migration from ITRS to IRDS is currently proceeding seamlessly, with all reports produced in the past by the ITRS 2.0 representing the starting point, and including contributions and groups from USA, Asia and Europe (i.e. an international dimension). This was a unique opportunity of NEREID to forge a partnership with IRDS and have reciprocal participations in meetings, and building a vision about the future of nanoelectronics, to which each initiative contributes with its specific strong points. Of particular

[1] Quotations from the CATRENE White Book: Public Final Report of the E4U Project *Electronics enabling efficient energy usage,* funded by the European Commission´s ICT programme in FP7 (project no. 224161), 2009
(2) J. Popovic, Gerber et al, *´Power electronics enabling efficient energy usage: energy savings potential and technological challenges´* IEEE Transactions on Power Electronics, vol. 27, no. 5, pp. 2338 -2353, May 2012

importance is the concrete actions taken to compare roadmaps between NEREID and IRDS in the following fields, in which the interests of the two initiatives overlap:

- *Systems and Architectures: Cloud computing, IoT, Smartphone, Cyber Physical* systems,
- *Outside System Connectivity*: RF & Analog & Mixed Signal, Photonic Interconnects,
- *Beyond CMOS*: Emerging memory and storage devices, Emerging information processing and logic devices, Emerging devices for functional diversification, Interface between emerging devices and novel computing architectures/paradigms,
- *Metrology,*
- *Yield,*
- *More Moore*: Logic technology, Memory technology, Interconnect technology,
- *Factory Integration.*

V Workpackage chapters

V. 1 Introduction

The following Chapters (V.2 to V.6) cover the main Nanoelectronic Technology sectors included in the NEREID Roadmapping:

- Beyond-CMOS

- Advanced Logic and Connectivity: More Moore (Innovative FETs and Memories) and Connectivity (Wireline and Wireless)

- Functional diversification: Smart Sensors, Smart Energy and Energy for Autonomous Systems

- System Design and Heterogeneous Integration

- Equipment and Manufacturing Science.

The common work presented below between technology and application experts is leading to the early identification of the most promising nanoelectronic technologies, which are needed for the future electronic products of European Companies leading to a substantial impact on the European economy and society.

V. 2 Beyond CMOS (WP2)

V. 2.0. Executive summary of Beyond CMOS

The Beyond CMOS chapter surveys the potential of the emerging technologies, new state variables and computing paradigms to provide efficient approaches to information processing, either for distributed computation within the expanding IoT or to realise accelerators on CMOS platforms to increase the processing speed. The focus is also on more fundamental issues like heat dissipation at nanoscale which has turned out to be the most critical bottleneck in information processing. The tables below are based on the discussions during the two workshops held in May 2016 in Espoo, Finland and in May 2017 in Sitges, Spain.

This chapter deals with “Non-conventional information processing approaches and devices”, focusing on the technology aspects of emerging information processing methods, and with “Designs and architectures for non-conventional information processing”, concentrating on the potential of these new technologies for

information processing and computing. The role of design and architectures (see Chapter 5) is crucial in emerging computation paradigms.

Category	Coverage
Quantum computing	Technologies to build qubits and transport information between them, including algorithmic and architecture
Molecular electronics	Solid-state information processing functions built on organic molecules including biomolecules; molecular spintronics
Spintronics	Spin-based electronics and related materials
2D materials	Carbon-based and transition metal dichalcogenides, as well as electronic and spintronic functions based on these
Extended & beyond CMOS	Non mainstream semiconductor transistors, including III-V materials, steep-slope devices, single electron transistors, etc.
Neuromorphic computing	Hardware implementation of neural networks, analogue and digital, architectures and applications

Areas of the current EU portfolio on Alternative Computing. Thermal issues and entropy driven approaches would enrich the palette. (From the presentation of Mr Eric Fribourg-Blanc, NEREID Sitges workshop on Alternative Computing Paradigms.)

V. 2.1 Relevance and competitive value

The chapter on Beyond CMOS follows the approach of the original EU Nanoelectronics Road Map of 1998 published in 1999[2], which was adopted by the ITRS in 2000-2002 version(s) and in the 2004 update onwards. It also builds on the document Beyond CMOS: NANO-TEC Project recommendations for research in nanoelectronics…. [3] and considers the IRDS 2.0 2015 section on Beyond CMOS. It is firmly anchored in research topics at the technology readiness level (TRL) 1.

The approach considers current research and development towards potential new information processing technologies. Thus, some of the research mentioned in the Beyond CMOS chapter is likely to underpin the complete ecosystem of the successful technologies in terms of knowledge, highly trained scientist and engineers, new experimental and theoretical tools, new fabrication tools and methods impacting on society.

The Beyond CMOS activities represent medium and long-term research, the cutting edge case-specific and targets tailored performance that can enhance information processing and energy efficiency. These emerging concepts constitute the source of potentially winning concepts for future disruptive technologies moving to higher TRLs in the 5 to 15 years time scales. Key to a realistic assessment and development of these emerging concepts and technologies is the early link to possible designs and architectures as well as to tools and manufacturing methods. European strength in low TRL research is widely accepted and, therefore, by starting the dialogue with designers and tool makers early enough, the possibility of informed decision making is further enhanced. A key aspect refers to energy consumption. The high power consumption and the consequent over-heating of the today's ICT circuits have led to the stagnation of the clock frequency at around 5 GHz, to the concept of multicore chips and eventually to "dark silicon", where only a part of the circuit is active and the rest remains idle to reduce power consumption. One of the targets of the new technologies is to find solutions to reduce the power consumption and create faster and more efficient devices and circuits.

The development and production of the high-end digital circuits are concentrated in a few factories outside Europe. The European microelectronics industry still relies on production of circuits but the role of MEMS and ASIC applications is growing. This development opens up a possibility to shift the focus to novel intelligent sensing and distributed computation applications, which need a new generation of skilled scientists and engineers for hardware, software, materials and process development. This will then most

[2] http://cordis.europa.eu/pub/esprit/docs/melnarm.pdf

[3] C. M. Sotomayor Torres et al., e-NanoLetters 29 (2014) 15-19.

likely impact in a positive manner economy, employment and academic curricula. For example, in previous EC framework programs and in H2020, the support for Doctoral Schools in advanced topics in nanoelectronics has been crucial to ensure a body of highly qualified scientists and engineers is available to pursue research in research organisations and industry exploring new ideas. Likewise, the EC support for infrastructure in multi-wafer projects, III-V and Si photonics is a sure enabler of the preliminary tests of concepts moving from to higher TRLs.
Efforts on a balanced gender participation are still needed. This issue is of increasingly importance, especially when Beyond CMOS advance toward potentially ubiquitous technologies impacting the whole of society.

V. 2.2 Vision

Emerging technologies cover a wide range of TRLs from 1-2 to 4-5 with a wide range of device concepts, wide range of materials, some of which are compatible with the current CMOS platform, and novel information processing paradigms. The aim is to evaluate the potential of the emerging technologies, try to find the strong points and challenges, and contribute to the recommendations of the NEREID roadmap.

It is not straightforward to define "Beyond CMOS" technologies and make the distinction, for example, from the "More Moore" and "More than Moore" approaches. One way is to use the Technology readiness levels (TRL) and restrict the Beyond CMOS technologies to TRL's 1-4, i.e., well below the level where a technology becomes mainstream. In the ITRS 2.0[4] and IRDS 2016 Edition White Paper[5] the Beyond CMOS devices or Emerging Research Devices include, e.g., scaled-down FETs, like FinFETs and Gate-All-Around nanowire FETs, and FETs in which silicon has been replaced, for example, by germanium, 3-5's or carbons as the channel material. In our vision these devices, although potentially steep-slope, still belong to the More Moore CMOS Extension regime. Tunnel FETs are included here because they have a different operation principle and the new 2-dimensional materials like TMDC's can be used in the fabrication. We have also omitted the More than Moore technology in which, e.g., analog or high power functionalities are added on CMOS platform. Although somewhat indeterminate, the selection of the technologies and information processing paradigms for this Chapter is based on the presentations of the experts dedicated to the Beyond CMOS work package, on the distribution of funding by the European Commission, especially within the FET programmes, and on the activities within the academia in Europe. The implementation of most of the emerging technologies presented here in information processing will probably be a long-term effort. At the same time, the new materials and nanoscale structures have plenty of room for medium-term applications in sensoring.

V. 2. 3 Scope and ambition

This chapter covers several emerging technologies and targets the identification of their potential, challenges and shortcomings in the frame of information processing.

The emerging technologies mapped in the first place included spintroniccs, neuromorphic approaches, heat transport at nanoscale and phononics, 2D materials, topological insulators, nano-optomechanics and molecular electronics. This was followed by a selection of technologies and concepts for Alternative Computing Paradigms.

The 2nd Workshop on unconventional computing paradigms focussed on photonic and nanomechanic computing, computing with spins and magnons, neuromorphic computing, steep-slope devices and

[4] http://www.itrs2.net/
[5] http://irds.ieee.org/reports

statistical/thermal physics and related computing approaches.[6] The tables below are based on the discussions and reports from the two workshops, with the main emphasis on potential to information processing and on the European dimension.

The methodology followed was the survey and discussion of emerging technologies, a selection from this set to further elaboration and an exploration of the selected ones for information processing in the frame of alternative computing paradigms. However, although the focus is on information processing, the potential of the emerging technologies in sensing has been taken into account.

In the long run, it is expected that the new ideas will be taken up by academia and industry. There is already a relatively strong demand and indirect support for the new approaches in Europe through the existing and forthcoming flagships, focussing on 2D materials, neural networks and quantum technology.

V. 2. 4 Main Concepts

V.2.4.1. Concept 1 : Quantum Photonics

a- Table of concept 1 Quantum Photonics

DRAFT	Medium term: 5+	Long term: 10+
Quantum Photonics		
a) Key research questions or issues		
• Photons do not suffer from decoherence so they are highly suitable for computing.	X	
• Single photon detectors for Si quantum photonics, currently relying on hybrid III-V/Si detectors or superconducting wire detectors.	X	
• Some photonic schemes require low temperature operation (2 K).	X	
• Phase change photonic allow brain function emulation.		X
b) Potential for application or Application needs and Impact for Europe		
• Quantum Computation		X
• Neuromorphic computing and their applications (see Concept on Neuromorphic Computing).	X	
• Si-based quantum photonics can use linear circuits, e.g., 8-qubit processor demonstrated.	X	
c) Technology and design challenges		
• More theory is needed to develop alternative architectures.	X	
• Full integration of all components on a chip for quantum computing and phase change materials for opto-neuromorphic computing.		X
• Long-term stability of photonic schemes must be improved, especially concerning the phase change materials, which require high peak temperatures.	X	
• Two-photon absorption losses in detectors need a speed vs loss compromise in optical switching.	X	
• Development needed on the cooling system technology.	X	
• Footprint and scaling challenges for phase change photonic computation.		X
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• Sources: Brightness, jitter and indistinguishability.	X	
• Circuits: Losses in circuit and connections, chip homogeneity, state fidelity when performing processing.	X	

[6] Development of circuits exploiting rapid single flux quanta (RSFQ) has been recently reactivated. An input on RSFQ technology was planned in the 2nd workshop, but unfortunately the expert could not attend the meeting and, consequently, RSFQ technology is not included in this version of the NEREID roadmap.

• Detectors: Efficiency, speed, dark count rate, jitter.	X	
e) Other issues and challenges, and interaction with other Tasks/WPs.		
• Novel architectures and more algorithms that harness the possibilities of quantum computing are needed. • WP5 Equipment and Manufacturing science: Photonics-related manufacturing lags behind that of nanoelectronics. • Dedicated research infrastructure is needed or access to modern nanofabrication facilities.	X X X	X

b- Competitive situation for Concept 1 Quantum photonics

Europe has a leading position in Si-based quantum photonics and SoA research in phase-change nanophotonics.

c- Recommendations for Concept 1 Quantum photonics

The European Commission has decided to launch a flagship project focussing on Quantum Technology. Quantum photonics topic should be addressed in that flagship.

V.2.4.2. Concept 2: Spintronics

a- Table of concept 2 Spintronics

DRAFT	Medium term: 5+	Long term: 10+
Spintronics		
a) Key research questions or issues		
• STT-MRAM is ready for volume production. • Provides reduction of the power consumption. • Lowering critical current for writing. • CMOS compatible. • Magnonics: Wavelength down to nm and frequency up to THz, 300 K operation and long propagation length (~ cm). • Compatibility with waveguide concept. • Efficient non-linear effect. • No Joule heat involved. • Not compatible with CMOS. • Enhancement of existing detecting techniques required.	X X X	X
b) Potential for application or Application needs and Impact for Europe		
• STT-MRAM is expected to fully seize the e-FLASH technology in the next few years. • MRAM usual applications are non-volatile operations, memories, memristor, sensors, bioapplications and energy harvesting. • Magnonics: Potential for computation operation, energy harvesting (spin Seebeck effect), memories among many others. • Size and power consumption reduction	X	X
c) Technology and design challenges		
• Spin wave majority gate exists for logics. • Reduce the temperature dependence of magnetic anisotropy for high T operation. • Reduce the size, time of operations and the power. • Slow group velocity (c/100).	X X X	X

• High attenuation (six order of magnitude higher than for photons in a standard optical fibre). • Fabrication processes, size and reliability. • Expensive material and difficult to grown (YIG). • CMOS compatible.	X	
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• Operation speed up to ~10s of GHz • Large lifetime memory ~ 10^{20} cycles at 0.6V • Insulators, no Joule heating		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
• New materials, equipment and processing technology required (WP5 Equipment and Manufacturing science)	X	X

b- Competitive situation for concept 2 Spintronics

The US Department of Energy founded recently a spin-based research cluster called "SHINES" (Spins and Heat in Nanoscale Electronic Systems) consisting 14 research groups from 7 institutions around USA.

From the academic point of view it can be argued that Europe, and specially France, leads the spintronic revolution. Germany included in its priority program SPINCAT: "Spin Caloric Transport" (2011-2017) and there is another priority program of the German Physical Society. At European level, the community of spintronics started its consolidation process led by France and formed in 2016 the network SpinTronicFactory.[7] Its mission is to promote research and innovation in Europe based on spintronics.

In Europe the participation of academia is very strong with a high profile global position. However, the participation of industry in spin-based memories, which is the main proven technology so far, is poor and almost inexistent. Nevertheless, several European start-up companies focussing on sensor technology have appeared in the last few years, for example, Crocus, Evaderis, Antalos, Capres and Singulus.

c- Recommendations for concept 2 Spintronics

Stronger industry-academia interactions are needed to identify jointly solutions to challenges. Spinwaves (magnons) have potential to ultra-low power operation (non-charge based, no Joule heating) and a majority gate for logics has been already demonstrated.[8]

V.2.4.3. Concept 3: Neuromorphic computing

a- Table of concept 3 Neuromorphic computing

DRAFT	Medium term: 5+	Long term: 10+
Neuromorphic computing		
a) Key research questions or issues		
• Neuromorphic computing mimics the operation of natural neurons. • Not necessarily based on von Neumann nor Boolean architectures. • One of the key issues is to understand the information processing of biological entities. • At the device level this means combining analog, or multi-level, and digital	X	X

[7] http://magnetism.eu/88-the-spintronicfactory-stf-.htm
[8] T. Fischer et al., Appl. Phys. Lett. **110** (2017) 152401.

information processing, combining memory and switches to realise synapses and produce the corresponding algorithms and circuit architectures to make use of the circuitry.		
b) Potential for application or Application needs and Impact for Europe		
• Pattern recognition including image processing, audio processing, tactile processing, olfactory processing, multisensory integration, EEG and MEG signal processing, medical monitoring (ECG, blood pressure…), brain-computer interfaces, robotics and motor control, financial markets etc. • High potential for next generation production, services and also safety and security. • Main activities in development of neuromorphic applications are currently developed outside **Europe (including Google, Facebook, Baidu and Amazon, IBM, Microsoft and Apple).** • Artificial intelligence- and IoT-related approaches to efficient next generation production offer new possibilities to European industry.	X X	X
c) Technology and design challenges		
• Dedicated hardware realizations. • New devices/circuits which combine memory and decision making, are mixed analog and digital and can communicate with the digital world are needed. • The circuits will be in most cases dedicated to specific tasks, and algorithms and interfacing with generic data processing need development. • Algorithms for HPC environment	X X X	X X
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• The most relevant issues are power consumption and speed, integration and compatibility with CMOS platform and connectivity. • Supervised or unsupervised learning. • FoMs are case dependent.	X X	X
e) Other issues and challenges, and interaction with other Tasks/WPs.		
• Materials and technology development need resources • The most efficient approaches rely on hardware dedicated to neuromorphic computing, • Emulation using HPC, algorithms and interfacing to big data and user interfaces require R&D. • Links to WP5 System Design and Heterogeneous Integration and WP6 Equipment and Manufacturing Science are relevant	X X X	X X

b- Competitive situation for concept 3 Neuromorphic computing

Outside Europe the main players are large companies, including both micro/nanoelectronics, e.g., IBM, Microsoft and Apple, and companies providing services and applications like Google, Facebook, Amazon and Baidu. While the micro/nanoelectronics companies develop dedicated devices and circuits for neural networks, the service providers exploit HPC. It seems that in Europe the majority of the work on neuromorphic computing is carried out within the Human Brain flagship project. While FPGAs provide a relatively straightforward route to hardware realisation, PCMs have promise to ultra-low power operation and set/reset switching has been demonstrated at μA current level and consuming only ~μW programming power.[9]

c- Recommendations for concept 3 Neuromorphic computing

Neuromorphic computing can benefit from the investments to HPC in Europe. For IoT applications, sensing and automotive industry, development of case specific fast and low power hardware together with the

[9] F. Xiong et al., Science **332** (2011) 568.

software and interfaces to digital world could turn out to become a new avenue to the European electronics, materials and equipment industry.

V.2. 4.4. Concept 4: Thermal, Brownian and nanomechanical computing

a- Table of concept 4 Thermal, Brownian and nanomechanical computing

DRAFT	Medium term: 5+	Long term: 10+
Thermal, Brownian and nanomechanical computing		
a) Key research questions or issues		
• Potential for energy conversion in the nano-scale near-field radiative heat not yet tested, except in realisations of surface-phonon polaritons but not in a sufficiently wide range of technological-relevant materials.		X
• Surface-phonon polaritons shown to transmit thermal energy over 100 um's on the surface.	X	
• To what type of interfaces does the concept of surface-phonon polaritons apply?		
• What are the boundaries and implications of signals performing a random search, in Brownian computing, looking for a way out in a maze of a circuit determined by topology?	X	
• What are the boundaries and implications of disorder-induced Anderson localization in the context of Brownian computating??		X
• Brownian computing has demonstrated the use of fluctuations in circuits based on SETs, through a random search mechanism, in addition to counting, testing of conditional statement, memory and arbitration of shared resources. Can an alternative to SETs be found?		X
• How large must the thermal driving field (driven fluctuations) be compared to the signal level?		
• How to define an operational local temperature in the nano-scale under non-linear conditions?	X	
• How does entropy change with varying distance between nanogaps and how important is it?	X	
• Potential to reach THz in NEMs-based computing with low power operation.	X	
• Potentially ultra-sensitive NEMs-based sensors.	X	
b) Potential for application or Application needs and Impact for Europe		
• Surface-phonon polaritons applied to enhance efficiency of thermal photovoltaics, magnetic switching and phase changes.	X	
• Design of future computers and neural networks.		X
• Potential to lower power consumption by harvesting fluctuations.	X	
• Brownian motion is used in less complicated device and to obtain universality.		X
• Harvest fluctuations instead of fighting them for computing (entropy-based computing?)		X
• NEMs-based concept could deliver cooling solutions by enhancing efficiency via driving the TE generator.	X	
• Integration with spintronics.		X
c) Technology and design challenges		
• Can we attempt evanescent wave engineering?		X
• What are the tolerances of thermal energy and fluctuation-based components and circuits?		
• Other schemes to apply the concepts of NEMs-generated		

thermoelectricity? • How to reach the ground state to move to quantum computation? • Scalability? • Need for ultra-clean devices. • Control of nano scale motion. • Do we have a better chance with hybrid computation using one or more of these approaches?	X	X
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• Orders of magnitude demonstration in power consumption. • Switching times • Energy as information (magnitude, frequency, …)		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
WP 6 Manufacture & Equipment and WP 5 Design and architectures		

b- Competitive situation for concept 4 Thermal, Brownian and nanomechanical computing

Europe has probably the strongest but dispersed community in nano-scale thermal transport, near-field radiation and Brownian motion, together with a very strong theoretical community on statistical physics. The NEMs and quantum NEMS community is still small, in particular the latter). It also has a leading community in the experimental front, developing new methods of measurements and tools for fabrication. The consolidation of the community is poor and is an obvious weakness.

c- Recommendations for for concept 4 Thermal, Brownian and nanomechanical computing

In heat transport in the nano-scale, NEMS and Brownian computing, the role of entropy must be taken into account vis-à-vis a measurand (energy? temperature?). Likewise the community needs to become one that can discuss and make progress and advocate its case.

Industry needs to be convinced of the value that this community can bring, especially in low power in the near future and in sub k_BT information processes in the long term.

V.2.4.5 Concept 5: Steep-slope devices for emerging energy efficient computation paradigms

a- Table of concept 5 Steep-slope devices

Tunnel FETs		
a) Key research questions/issues	Medium term: 5+	Long term: 10+
- What performance (I_{on}, I_{off}, g_m, SS, switching speed) can be achieved in different materials and geometries? - Channel length scalability is likely worse than for MOSFETs, how will this impact applicability for future nodes? - Will we be able to bring trap level densities (Dit, TAT,..) low enough for BTBT to dominate in entire swing region. - Origin of trap mechanisms, extrinsic like D_{it} in gate stack or intrinsic related to doping tails or material composition, and to which extent can they be controlled. - Investigations of variability and reliability of	- Recent devices show performance with sub-thermionic SS over 2-3 decades of current, but performance still needs to be improved in terms of higher I_{60} and operation frequency. - Tunnel FETs are mostly limited by trap mechanisms not BTBT. Predictions how that at least $D_{it}<5x10^{12}$ cm^{-2} must be achieved, which is challenging to reliably achieve in heterostructure systems.	- Long-term scalability for TFETs could be an issue, if gate lengths cannot be scaled because of direct source-to-drain tunneling and need for underlapped regions. Traditional scaling should be re-defined in 2D/2D Tunnel FET architectures. - Performance/speed trade-off compared to other advanced devices (NWs, 2D)

TFETs is still very limited. - Boosting of Tunnel FET by disruptive solutions: phase change materials and negative capacitance	- How good must TFETs be to bring an advantage? Just a few percent improvement in SS, will not justify substantial technology changes. - Tunnel FETs should complement advanced CMOS platforms, for smart co-design: more energy efficient multi-core in hybrid CMOS-Tunnel FET design. - Technology boosters such as negative capacitance and phase change materials in the source of tunnel FET will improve their characteristics	- The goal is to achieve Complementary Tunnel FETs with Vth ~0.1V and Vdd ~0.2-0.3V and Ion ~200-500uA/um. - Beyond traditional logic design with Tunnel FETs, such as neuromorphic ICs.
- b) Potential for application or Application needs and Impact for Europe	-	
- TFETs are not high speed devices (comparatively), so target applications should exploit low I_{off}. - Very strong European efforts on TFET both in terms of device technology and simulation. - A high potential of Tunnel FETs concerns the analog gain at low current/voltage and their thermal stability	- IoT and other applications targeting lower frequency ranges < 500MHz-1GHz, but where active and passive power consumption is essential. - Potentially hybrid technologies mixing TFETs and conventional devices - Low power analog ICs with high temperature stability - Tunnel FEt sensors and new readout interfaces for sub-100nA current levels	- Heterogeneous systems. Complex III-Vs required for TFETs → potential for co-integration with active photonics, sensing and RF technologies. - Exploiting temperature independence of TFETs (once trap issues are solved), applications with greater temperature span.
c) Technology and design challenges		
- Non-standard Si CMOS, requires an ecosystem for III-V capability and integration opportunities. - Complementary tunnel FET in other than Si technologies are technologically very challenging. - No design infrastructure for TFETs. - Reliable TCAD, compact models and design tools which accurately capture behavior and does not require extensive tuning are needed to enable VLSI TFET designs. - Demonstration of vdW Tunnel FET in 2D/2D embodiments for sensing and analog functions	- Demonstration of sufficiently good p-and n-TFETs in independent technologies. - Demonstration of working devices based on other concepts EHBTFET, superlattice FET, resonant TFET, 2D/2D tunnel FETs - Strong coupling to other technology developments, if III-V MOSFETs do not make it for 7 or 5nm nodes, TFETs most likely will not either. - vdW 2D TFETs, does this technology offer advantages over compound semiconductor technology?	- Current best devices are either based on exotic air-bridge/MBE structures or vertical NWs which rely on processing tuned to specific material combinations. For TFETs to become mainstream mature technologies (lateral or vertical) must be developed which allow for complementary TFET circuits. - High-performance complementary TFET technologies in foundry environment. - 2D/2D Tunnel FETs in BEOL embodiments for smart sensing
- d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time.		

- I_{off}, I_{60}, I_{on}, SS_{ave}, g_m, - Temperature sensitivity included as metric/evalaution - Common definition of metrics for comparison of different sources and technologies. - I_{60} is an excellent FoM which has been pioneered by simulation. Will become relevant when experimental devices get better. - Abolish the use of SS_{min} – meaningless number	- Target I_{60} close to 100uA/um combined with SS_{ave} < 60mV/dec.	- Metrics will be application specific - Target I_{60}=500uA/um combined with SS_{ave} < 50mV/dec. - Need to demonstrate reasonable dynamic performance, ~1GHz operation
- e) Other issues and challenges, and interaction with other Tasks/WPs.		
- Electrostatics more important than for MOSFETs → need for confined geometries - Potential high process variability and sensitivity to process variations; robust design for Tunnel FETs.	- Simple correlation of material parameters (μ, m_{eff}, E_G..) to device models incorporating heterostructures. - Control of variability	- High-performance TFETs will need III-V → potential traction with integrated photonics. - Analog ICs and sensors based on Ge/SOI Tunnel FETs or on 2D/2D Tunnel FETs in BEOL

b- Competitive situation of concept 5 Steep-slope devices

TFETs are not presently high-speed logic devices, so target applications should exploit low Ioff for very low power applications. The possible applications scenarios are: (i) more energy efficient hybrid CMOS-Tunnel FET cores for digital computation, (ii) energy efficient neuromorphic design with Tunnel FETs, and, (iii) use of Tunnel FET for low energy computation, analog and sensing applications in the IoT field.

c- Recommendations for concept 5 Steep-slope devices

- Demonstrate TFETs with combined performance superior to MOSFETs at <0.3V
- Develop understanding of the impact of traps and develop design and technology mitigation strategies.
- Study, optimize and implement more technology boosters for TFETs such as negative capacitance and phase change materials for enhanced performance.
- Develop compact models and design tools including hetero-junctions and III-Vs
- Investigate hybrid CMOS-TFET core design
- Evaluate performance beyond DC-IV: LG scalability, speed, noise, variability, reliability
- Establish foundry-level scalable complementary TFET platforms, preferably hybrid CMOS
- Explore TFETs for analog and sensing, with potential integration of 2D/2D architectures in BEOL.

V. 2.5 Synergies with other topics

The production processes and processing equipment of nanoelectronic circuits have been developed to the ultimate level at the sub-□m dimensions with hundreds of lithography steps on 300-450 mm wafers. In many ways, the majority of the Beyond CMOS devices could benefit from the existing technology. The palette of materials will be broader, however, the compatibility of the new materials with current processes is likely to be manageable. While in first approximation no mayor barriers are foreseen, and the potential for equipment and processes of some emergent technologies looks feasible, this aspect has to be further discussed in collaboration with the WP6 Equipment and Manufacturing Science.

The majority of the new computing paradigms are based on non-von Neumann architectures. The design of the circuits, their architectures and connectivity to the CMOS platform, internet, telecom, etc., have to be standardised and this has a close connection to the activities in WP5 Design and Architectures. In addition, non-Boolean operation, e.g., analog and multi-level, poses a challenge to the development of algorithms.

Although for the realisation of most of the Beyond CMOS technology candidates, realisation of information processing apparata is a long-term target, many of them can already provide new possibilities for efficient and fast sensors. For example, 2-D TMDCs are promising materials for tunnel FETs and, in addition, they have potential in optoelectronics as emitters[10] or ultra-fast detectors.[11] In molecular electronics, connecting the molecules has turned out to be very challenging. Nevertheless, molecules can self-assemble and the assemblies can be used, for example, as photochromic[12] or redox switches.[13] In addition, the very small size of molecules enables the exploitation of quantum effects at room temperature.

V. 2.6 Recommendations for Beyond CMOS research

A thread running through most of the alternative computing approaches is the need to understand at conceptual, experimental and technological levels the thermal properties of materials and interfaces involved. This is currently a handicap ("show stopper") in the form of heat dissipation in almost all current and emerging technologies. Thus, *a shift of paradigm in the perception of the thermal management challenge is needed*. Europe has the potential to lead in this field and, consequently, to remove this roadblock.
In silicon CMOS technology the heat dissipation challenge has led to "dark silicon", use of multi-core units and to saturation of the operation frequency to a few GHz range, hindering the full exploitation of the potential of CMOS circuitry. In the long term, thermal issues can be transferred to Brownian or entropy computing and used either on their own or in a hybrid approach with other state variables. Capitalising on the wave nature of thermal vibrations is very challenging but it offers a potential alternative to very low power information processing. Nevertheless, at the moment embryonic efforts in this direction are few and far between pursued by fragmented communities, each excellent in their own right.

In the near term, neuromorphic computation holds a high promise in applications such as the IoT and big data. The field is making strong progress in algorithms and, to a lesser extent in hardware realisations. There are several technology candidates and the planned FET CSA may well accelerate progress in the Human Brain flagship, in ICT LEIT projects and future constellations. Nevertheless, *a directed program towards neuromorphic hardware development in Europe is recommended*.

Si-based quantum photonics must be an integral part of the Quantum Technology flagship, building on the European leadership in the field, already breaking frontiers in chip-level integration and competing globally in innovations, for example, with nanophotonics-based components such as single photon detectors based on superconducting nanowires.

Regarding spintronics, memory cells are already in the market, and spin/charge-based devices, such as spin torque and spin Hall devices, are being developed. Moreover, there is also potential to create neuromorphic circuits using spintronics. Magnons or spin-waves provide an interesting possibility for ultra-low power and very fast devices, and some logic elements, like majority gates, have already been demonstrated. Therefore, *coordinated efforts in magnonics are recommended*.

[10] F. Withers et al., Nature Materials 14 (2015) 301–306.
[11] L. Waldecker et al., Phys. Rev. Lett. 119 (2017) 036803.
[12] J. S. van der Molen et al., Nano Lett. 9 (2009) 76–80.
[13] J. Liao et al., Chem. Soc. Rev. 44 (2015) 999-1014.

The range of materials under investigation within alternative computing paradigms goes well beyond silicon, e.g., in quantum (nano)photonics, neuromorphic computing and spintronics. Steep slope devices are no exception. Thus, *advances are urgently needed with technological figures of merit in mind of several non-silicon based materials*, ranging from scalable material production technologies, through wafer-scale nanofabrication with innovative tools and last but not least, a combined effort from the start with the design and architecture community.

V. 3 Advanced Logic and Connectivity (WP3)

V. 3.1 Nanoscale FETs (T3.1)

V.3.1.1 Executive summary

The historical trend in micro/nano-electronics over the last 40 years has been to increase both speed and density by scaling down the size of electronic devices, together with reduced energy dissipation per binary transition, and to develop many novel functionalities for future electronic systems. We are facing today dramatic challenges for More Moore and More than Moore applications: substantial increase of energy consumption and heating which can jeopardize future IC integration and performance, reduced performance due to limitation in traditional high conductivity metal/low k dielectric interconnects, limit of optical lithography, heterogeneous integration of new functionalities for future nanosystems, etc.
Therefore many breakthroughs, disruptive technologies, novel materials, and innovative devices are needed in the next two decades.
With respect to the substantial reduction of the static and dynamic power of future high performance/ultra low power terascale integration and autonomous nanosystems, new materials, ultimate processing technologies and novel device architectures (FDSOI, FiNFET, Nanowire FET, Non-charge-based Memories, 3D integration) are mandatory for different applications using ultimate CMOS, as well as new circuit design techniques, architectures and embedded software.
This section will focus on the main trends, challenges, limits and possible solutions for future high performance and ultralow power nanoscale devices in the CMOS arena.

V. 3.1.2 Relevance and competitive value

What are the advantages of the chosen technologies (concepts) compared to others?

During decades, Moore's law was the main driver of the CMOS world, and most of the electronic industrywere scaling the CMOS area by a factor 2 every 2 years. At the 32/28nm node, the industry introduced the first CMOS revolution by leaving the classical bulk CMOS integration to shift to thin-film devices for improved electrostatic control.
In this way, STMicroelectronics introduced the 28FDSOI, and companies like INTEL, Samsung and TSMC have shifted to FinFET technologies and are continuing down to the 10 and 7nm node. In this context, the CMOS world is facing a second revolution, as the famous Moore's law slows downs because cost and complexity of scaling are increasing faster than economic advantages. The technology-push approach that has driven semiconductor evolution is slowing down, while the market is shifting to a more application-driven approach. This implies that technology differentiation is becoming again a critical issue for semiconductor actors.

V. 3.1.3 Vision

For future, reliable, high performance and /or low power ICs and systems, new materials (strained semiconductors, SiGe, Ge, III-V, 2D, 1D), ultimate processing technologies and novel device architectures (FDSOI, FinFET, Nanowire FET, Non-charge-based Memories, 3D integration) are required.
In the field of alternative memories, PCRAM, RRAM or MRAM will be useful for pushing the limit of integration and performance beyond those afforded by present Non-Volatile, DRAM and SRAM memories.
3D sequential processes could also be used for the integration of these future high performance sustainable, secure, ubiquitous and pervasive systems, which will be of high added value for many applications in the field of detection and communication of health problems, environmental quality and security, secure transport, building and industrial monitoring, entertainment, education, etc.

V. 3.1.4 Scope and ambition

In this mid-term Roadmap, we have chosen some core technologies that we think are the most promising for many future applications in order to overcome the number of challenges we are facing for future ICs, in particular:

-High performance
-Low/very low static and dynamic power consumption
-Device scaling in the range
-Low variability
-Affordable cost

Considering these challenges, the following nanodevices and technologies have been considered as very relevant for future Nanoscale FETs:

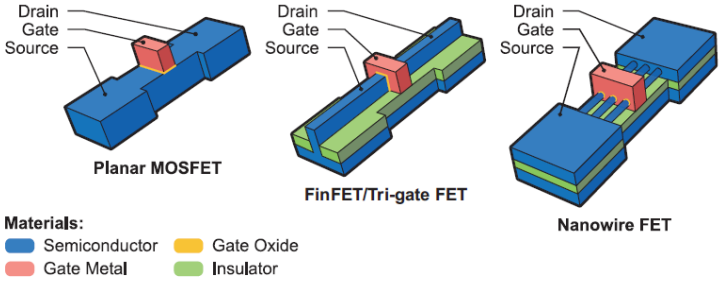
-FD (Fully Depleted) SOI (Silicon-On-Insulator) MOSFET: for low power applications and low variability
-FinFET (or Trigate FET): for high performance and/or low power applications
-Nanowire FET: for high performance and low power applications and ultimate integration
-Non-charge-based/Resistive Memories: to replace charge-based memories using PCRAM (Phase Change RAM), RRAM (Resistive RAM using a nanofilament), or MRAM (Magnetic RAM, especially STT/Spin Transfer Torque MRAM)
-Sequential 3D integration: for increasing device integration (transistors, memories, sensors, etc.) using 3D stacking
-The roadmap also covers the future modelling and characterization tools needed for developing these future devices and technologies.

V. 3.1.5 Main Concepts

V.3.1.5.1. Concept 1: Nanowires (Main contributor Lars-Erik Wernersson, Lund University)

The evolution of MOSFETs is shown in the figure below, starting from plane device to FinFET, ending by Nanowire FET, which could be the best device due to the following advantages:

-Advantageous carrier transport with optimized volume inversion: high transconductance gm and driving current Ion
-Wrap-gate geometry and small nanowire diameter: large number of electrons, low output conductance gd, reduced short channel effects DIBL (Drain Induced Barrier Lowering) and charge sharing, low Ioff.



Evolution of MOSFETs from planar structure to nanowire

a- Table of concept 1 Nanowires

Concepts/Technologies	Medium term: 5+	Long term: 10+
i) Nanowires		
a) Key research questions/issues		
- What performance (I_{on}, I_{off}, g_m, f_t/f_{max}, NF) can be achieved in different materials and geometries? - How can different materials/geometries be manufactured at large scale? - Evaluation of interface and dielectric quality from HCI and PBTI measurements - Investigations of variability for 10 nm nanowire diameter/gate length transistors - Circuit/technology co-design in 3D transistor architectures	-Available data suggests that the best performance (lowest I_{off}, highest I_{on}, highest g_m, etc) is obtained for Si, Ge, and III-V nanowires. Hybrid III-V/SiGe channel technology has been demonstrated as well as III-V gate stacks with $D_{it}<10^{12}$ cm^{-2}. Transistor data is available for < 10-15 nm In(GaAs) diameter.	-Current status includes first demonstrations of SRAM cells and first nanowire amplifiers designed in complex 3D geometries. A maturing technology will enable circuit implementation -With current efforts on TMD materials synthesis, it is likely that the technology will mature and contribute to the roadmap - CNT show promise in stacked memories
b) Potential for application or Application needs and Impact for Europe		
-Extend the roadmap for CMOS scaling based on improved electrostatic control and increased drive current -Meeting the low-power demand for IoT applications -Enhance the CMOS RF-properties by (III-V) materials integration -Increase performance in mixed-domain by increase in f_t/f_{max} -Provide opportunity for efficient mmWave front-ends combined with high-speed digital logic -Electrostatic control provided by nanowires/nanosheets critical for TFET implementation	-Tailoring of Si and Ge nanowire transistors to meet the demands of IoT. -Introduction of hybrid III-V/Si(Ge) and/or all-III-V technology for high-performance applications (both RF/mmWave and mixed-mode)	-Integration of high-speed logic and high-performance RF front-ends using III-V technology combined with CMOS and possible TFETs
c) Technology and design challenges		
- Challenges in terms of 3D processing in complex geometries at 10 nm L_g - Evaluation and reduction of parasitics in 3D transistors at 10 nm L_g - Understanding and reduction of thermal effects in 3D transistors at 10 nm L_g (heating, reliability …) - Strain engineering (processing, characterization etc) at the 10 nm length scale - 3D vertical transistor stacking to reduce area (vertical/lateral channels) - Strategies for co-integration of various types of transistors (Si, Ge, III-V, CNT) in manufacturable CMOS processes - Transistor and circuit co-design and optimization in complex 3D structures	-Maturing of the process technology for Si, Ge and III-V nanowires to meet the requirements of IoT and high-performance applications -First demonstration of nanowire circuits with competitive/high performance	-Circuit layout in complex 3D architectures with minimized parasitics -Improved materials and process control of 2D materials

d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
- I_{on}, I_{off}, g_m, f_t/f_{max}, NF	Rapid development with current status: Ion 650 µA/µm (normalized to periphery) , > 3mS/µm gm (normalized to periphery) , <1nA/µm Ioff , > 500 GHz fmax	Further improvement in fmax and processing stability
e) Other issues and challenges, and interaction with other Tasks/WPs.		
- Nanowire transistors provide the electrostatic control required for TFETs - The electrostatic control in nanowires and sheets will allow for reduction of off-state leakage to meet IoT requirements - The high g_m and self-gain make nanowire transistors promising for millimeter wave applications (connectivity) -A selection between nanowires and FinFETs is likely	The technology development will follow points a-c	The technology development will follow points a-c

b- Competitive situation of Concept 1 Nanowires

Nanowire FET can be considered as the best FETs for the ultimate integration of CMOS devices with the best performance and lowest power consumption for the 0X technology nodes.

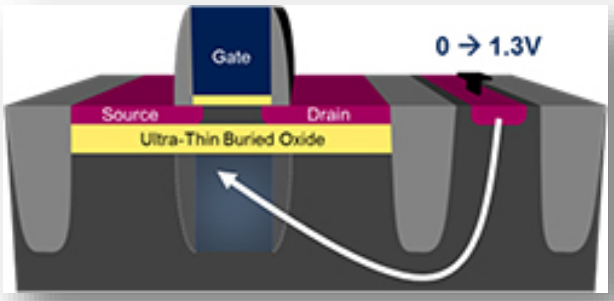
c- Recommendations for Concept 1 Nanowires

- Identify the best material and geometry options for logics (high-speed as well as low-power)
- Develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar)
- Develop transistor/circuit co-design strategies for mixed and mmW applications
- Consider the 3D aspects of processing (stacking, vertical integrations etc)
- The electrostatics and heterostructure design options provided are beneficial for TFETs

V.3.1.5.2. Concept 2: FDSOI (Main contributor Stephane Monfray, ST)

Fully Depleted Silicon On Insulator, or FD-SOI, is a planar process technology that relies on two primary innovations. First, an ultra-thin layer of insulator, called the buried oxide, is positioned on top of the base silicon. Then, a very thin silicon film implements the transistor channel. Thanks to its thinness, there is no need to dope the channel, thus making the transistor Fully Depleted. The combination of these two innovations is called “ultra-thin body and buried oxide Fully Depleted SOI” or UTBB-FD-SOI. FD-SOI technology enables control of the behavior of transistors not only through the gate, but also by polarizing the substrate underneath the device, similarly to the body bias available in Bulk technology.

As the slowing of Moore’s law signals the beginning of “Smart Everything”, each FDSOI process node can be a long lasting technology with differentiated options (RF, Mixed signal, Ultra Low Power, Embedded Memories, sensors…). The challenges and needs will be mainly focused on their ultra-low power possibilities to reduce as much as possible the supply voltage and improve the energy efficiency.



source: www.st.com

Fully Depleted Silicon-On-Insulator MOSFET

a- Table of concept 2 FDSOI

	Medium term: 5+	Long term: 10+
Concept 2: FDSOI		
a) Key research questions or issues		
Improving performances for sub-14nm nodes (strain technologies for Higher drive current)	Introduction of dual stressors on sSOI wafers	More efficient dual stressors on sSOI wafers
Structure evolution (Si & BOX thickness reduction challenges) for electrostatic control for sub 14nm node	Tsi<6nm Tbox<15nm	Tsi<5nm Tbox<10nm
Evolution of planar FDSOI to multi-gate structure (nano-sheet) with at least 2 conductive channels	Development of planar nanosheet devices (2 channels)	More than 3 channels (multi stacks)
Design evolutions exploiting back biasing techniques	ULP IoT dedicated design Vd<0,5V	ULP IoT dedicated design Vd<0,4V
Evolution of FDSOI platform to new materials (GeOI, III-V OI) and sequential 3D integration	sSOI, SiGeOI with high Ge content, sequential 3D	sequential 3D sSOI / GeOI / III-V-OI for RF
FDSOI Logic & embedded flash memories for micro-controller applications / Automotive applications	Development of embedded flash memories (PCRAM, …)	New flash memories, innovative selector device
Electrical characterization of small scale devices (transport, capacitances, local strain impact…)	New techniques for short devices transport characterization	Evolution to Ballistic transport
b) Potential for application or Application needs and Impact for Europe		
low power applications	Consumer, IoT, Automotive…	Automotive smart sensors / imaging computing
Ultra-Low Power devices for IoT (Vdd<0,4V)	Application to wearable devices	Application to medical devices
Harsh environment resistant devices	Spatial applications	Spatial applications
FDSOI Logic & embedded flash memories for micro-controller applications / Automotive applications	Automotive, IoT	Automotive, IoT
FDSOI development for Analog and RF applications and integration with bipolar devices for high speed devices	High speed Datacom	High speed Datacom
Application of FDSOI for Innovative sensors (use of FDSOI design for sensing)	Concept of new sensors with FDSOI (Imaging, pH sensing, gas sensing…)	Applications to integrated and low power Gas sensing, biosensing, Autonomous Imaging
Beyond CMOS devices co-integration w/ CMOS (Quantum devices – eg: Qbit)	Development of Quantum devices	Development of Quantum systems
FDSOI for neuromorphic circuits design challenges	3D integration for neuromorphic designs	3D integration for neuromorphic designs
c) Technology and design challenges		
Integration of Strain SOI substrates: processing of tensile strain for NMOS & compressive strain for PMOS	Local strain N & P MOS	Local strain N & P MOS
Compatibility with flash memories process (as eg in BEOL)	Reliable and energy efficient embedded memory	Reliable and energy efficient embedded memory
FDSOI design for ultra-low power (Vdd<0,4V)	Subthreshold circuits	Circuits with sub-60mV/dec devices

Evolution of FDSOI co-integrated with Tunnel FET option	Development of solutions for sub-60mV/dec devices	Development of solutions for sub-60mV/dec devices
Thermal management/self-heating mitigation with 3D integration	Passive Local cooling solution	Low cost Passive Local cooling solution
Integration with new materials (SiGe, High Ge content) and future III-V materials (logic applications)	High Ge conc. SiGeOI	3D III-V OI circuits
New material for differentiator: III-V OI for photonic	Development of Co-integration of CMOS with Si- photonic	Development of Co-integration of CMOS with Si- photonic
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
Ieff/Ioff	Ieff 470/420 µA/µm @10nA/µm Ioff	Differentiation through options
Variability (Avt)	<1mV.µm	<0.8mV.µm
Vdd (logic)	<0,75V	<0,6V
Subthreshold slope	<70mV/dec	<65mV/dec Introduction of sub-60mV/dec technologies
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Link with WP2: enabler for neuromorphic computing/quantum computing Link with WP4: sensors+ cmos co-integration enabler Link with WP5: need for understanding system level benefit of 3D sequential options Link with WP6: development of strain silicon layers, low T processes, wafer bonding for new material on insulator, low temperature epi, gate stack materials/interfaces development for low T for 3D technologies and new materials integration		

b- Competitive situation for Concept 2 FDSOI

FD SOI MOSFET can be considered as the best FETs using planar devices for low power applications, harsh environments (radiation, temperature), and are also very interesting for analog and RF applications.

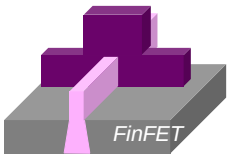
c- Recommendations for Concept 2 FDSOI

From technological point of view, performances can be boosted also with breakthrough approaches like sSOI, monolithic 3D integration (e.g 28nm/28nm) or new materials without device scaling. From device architecture point of view, FDSOI technology can suit 14nm & 10nm nodes and can be replaced by FinFET or Nanowires for 7nm and below.

-Develop differentiated options (RF, Embedded Memories, Imaging or molecules sensors) on FDSOI (applications for automotive, IoT, smart sensors…)
-Develop ULP design (Vd<0,4V) for IoT market (wearable, medical…)
-FDSOI and 3D integration can respond to future neuromorphic and quantum computing approaches

V.3.1.5.3 Concept 3: FinFET (Main contributor Anda Mocuta, IMEC)

FinFETs are presently the most advanced nanodevices especially for high performance applications. They are using a trigate structure for improving the driving current and the control of electrostatic effects, as show below:



FinFET realized on bulk Si substrate

a- Table of concept 3 FinFET

iii) FINFETs	Medium term: 5+	Long term: 10+
a) Key research questions/issues		
- subthreshold slope control to less than 70mV/dec at very short gate length (<14nm) - improved device performance (Ion/Ieff at given Ioff) while scaling the gate length and pitch - control of parasitic capacitances at scaled dimensions - Variability control at very scaled dimensions	- innovation needs to continue in the following areas: contact resistivity, conformal doping, dopant activation above solid solubility limit, low k or air spacer; HKMG scaling and multi-Vt; high mobility channels; channel strain enhancement; integration of taller fins; - understand under what conditions nanowires will outperform finfets; - Co-integration with other device architectures or between 2 channel materials - 3Dsequential integration with other devices	- finfet is becoming a mature device architecture, on the longer term all optimization knobs may be already understood. - 3Dsequential integration with other devices
b) Potential for application or Application needs and Impact for Europe		
- current workhorse device for Si CMOS technologies - current best option for high performance space - currently can cover part of the low power/low cost space - can be considered for quantum computing as qbits - Specialty sensors		
c) Technology and design challenges		
- No single device/material able to replace Si CMOS; Co-integration of finfet with other device architectures or between different channel materials will be key - Improve finfet analog performance	- develop finfets that can be processed at low T; - develop finfets that can withstand a long thermal cycle for 3D seq integration; - develop integration flows for multiple channel materials and strain(e.g. Si, SiGe, Ge, III-V on Si or SRB)	- develop co-integration schemes between finFETs and nanowires/nanosheets
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
- I_{on}, I_{eff}, CV/I,	20% improvement/2-3yrs	20% improvement/2-3yrs

- Subthreshold slope	SS<80mV/dec	SS<80mV/dec
- min achievable $I_{off,}$, GIDL	<10pA/um	<10pA/um
- $A_{vt,}$	<1mV.um	<0.8mV.um
e) Other issues and challenges, and interaction with other Tasks/WPs.		
- manufacturing processes and integration will become very complex; working with increased aspect ratios will be key - system level studies to decide what are the best devices to be co-integrated and in what way, for a given application	Manufacturing processes to be developed are same as in a)and c)	Manufacturing processes to be developed are same as in a)and c)

b- Competitive situation for Concept 3 FinFET

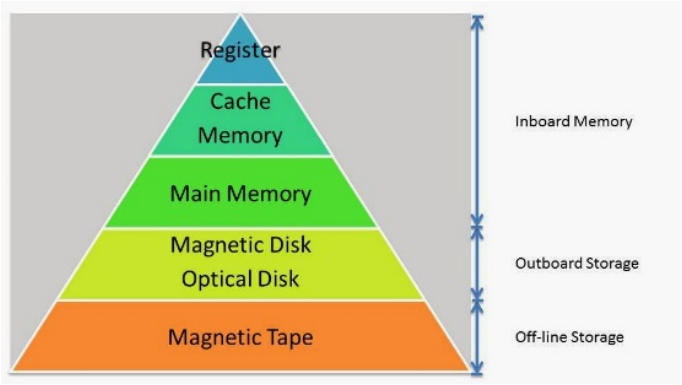
FinFET is the current workhorse device for advanced Si CMOS technologies and is current best option for the high performance space. It can also cover a part of the low power/low cost space.

c- Recommendations for Concept 3 FinFET

- Develop co-integration of different channel materials
- Develop low thermal cycle finFETs for sequential integration
- Develop low contact resistivity and high strain solutions
- Improve finFET analog performance
- Develop finFETs as devices for quantum computing

V.3.1.5.4 Concept 4: Memories (Main contributor Carlo Cagli, CEA-LETI)

Today, stand-alone memory is a pure 3D NAND-Flash. Emerging NVM aims at SCM/Storage Class Memories (memory between DRAM and storage) and embedded memories for automotive or IoT. New disruptive applications like neuromorphic are also becoming important. Therefore, in this domain we focus on non-charge-based memories (PCRAM, RRAM or MRAM) which could satisfy the performance needed for many future applications.



Different types of Memories

a- Table of concept 4 Memories

iv) Emerging memories for storage class memory, IoT and embedded (µC) application	Medium term: 5+ Identification of a "winning" technology and definition of required specs. Analysis of real application domain No soft errors required (but possible ECC) Endurance > 10^{11} Retention hours—days for power loss in PC Current <100µA (at 1-2V) Speed <1-10µs	Long term: 10+ Proof of concept with identified specs
a) Key research questions/issues		
OxRAM: HRS distribution reduction Operation energy reduction	Cell reduction and/or encapsulation techniques can be beneficial and need to be investigated. New materials? HfO2 or Ta2O5… other candidates? If at 5 year OxRAM don't answer to this question, they will probably disappear	HRS distributions controlled. This can happen in 2 ways: 1. On known materials like HfO2, working on scaling, encapsulation, programming techniques, CF confinement; or 2. Changing material. This way seems less likely, because HRS spread looks to be intrinsic in the CF-like switching
CBRAM: Increase of endurance Increase of data retention	Specimens are on the market! New generation required and waited. Can CBRAM meet specs for SCM?	CBRAM has to improve data retention, to meet Flash standards (85C 10y) or 125C 10y for automotive. Endurance is less stringent for most applications, but 10^5 will be required.
MRAM: How to integrate complex magnetic stack?	Main issues related to integration and COST. Some samples are available (mainly Everspin). Fab integration demonstration required. New tools required for integration (large Capex). Specs are ok.	Integration of MRAM process in foundries need to be assessed. Reduction of programming current required (10-100pJ/bit can be a reasonable figure).
PCRAM: How to reduce erase current? How to increase data retention?	Material research, architecture research PCRAM is also candidate to SCM, and to replace flash for embedded applications (ST). 28nm integration has to be achieved.	PCRAM has to demonstrate integration in <<28nm.
FeRAM (FeFET) Increase of ⍰Vth	Mostly for embedded application at scaled node. One main actor (GF and Namlab) First demonstration available. At 5 years a commercial generation 1 required. Research on HfO2 dopant needed to increase coercive field→Vth shift	Difficult to establish: FeFET is a very recent device.

b) Potential for application or Application needs and Impact for Europe		…
Embedded: integration at scaled node <28nm scaled SoC automotive application(but spec needs to be demonstrated) IoT Security applications (embedded security) SCM: Applications on PC, tablet, phones, consumer markets High speed computation Fast boot Recovery after power loss Computing in memory	Identification of the technology to be adopted: PCM, MRAM, OxRAM Specs are required!! Applications need to be clarified and identified Embedded memory at 40nm, with reduced consumption Need to prove that specs are achievable. Need to identify the potential of SCM Same as embedded + need to scale as much as possible. 28nm compulsory	Scaling limit has to be identified Lowering potential is imperative By 2025 memory at 28nm with low power consumption, also intended for computing Identification of technology to be used First demonstrators must appear Sub 10nm required
	…	…
c) Technology and design challenges	…	…
MRAM	Scalability is main challenge. 14nm can be reached with material engineering.	Below 14 nm, a new cell structure is required. Increasing the number of interfaces to stabilize the magnetic polarization.
OxRAM and CBRAM	Need to confine CF. work on the cell encapsulation and interfaces. New designs on system level can open new (niche) market. Ex: IoT (this can be a mainstream), neuromorphic, TCAM, NV-DRAM, memory computation… However, crossbar will be necessary for density→ need for BEOL access diode	Difficult to say, OxRAM has big challenges in the 5 years horizons already
PCM	Need for cell thermal confinement→ GST etching required. 2 research axes: 1. Materials improvement for quicker write/erase and 2. Improvement for higher thermal stability (for embedded applications, 150C	Scalability at 1x nodes with thermal confinement looks as a main challenge.

	automotive + 260C 2’ for soldering reflow)	
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time) FoM are known already and relatively quantified for the applications		…
SCM: High endurance Low voltage	10^{10}-10^{12} Forming voltage is the main issue. 1V-2V required	Generally speaking SCM applications require a complete review of memory architectures. Potentially, core structure needs to change to take advantage of SCM memory. Universal memory? If a universal memory is found, the entire memory hierarchy will be replaced, but this is extremely unlikely in 10y.
Embedded: Scalability Low voltage and current High retention	Erase current<100µA Retention as flash requirements (soldering reflow is also to be considered)	
IoT: like embedded, with special care of low energy	Very low energy <50µA?? no specs available	
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Interaction with WP3, 4, 5 and 6		

b- Competitive situation for Concept 4 Memories

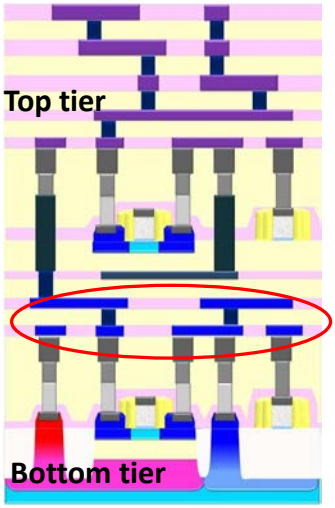
Non-charged-based Memories (PCRAM, MRAM, RRAM) can potentially overcome many technology limitations of traditional charge-based memories and could be used for many applications (e.g. Embedded and SCM/Storage Class Memories).

c- Recommendations for Concept 4 Memories

- OxRAM: HRS broadening is the Challenge. New materials, new programming challenges are required
- PCM: process improvements necessary for GST patterning
- MRAM: scalability is the issue. This requires new material enabling horizontal scaling

V.3.1.5.5 Concept 5: 3D sequential integration (Main contributor Claire Fenouillet, CEA-LETI)

3D sequential integration is an alternative to conventional device scaling. Compared to TSV-based 3D ICs, 3D sequential process flow offers the possibility to stack devices with a lithographic alignment precision (few nm) enabling via density > 100 million/mm^2 between transistors tiers (for 14nm design rules). It's also possible to merge several technologies and materials. The typical structure is shown below:



3D sequential integration of various devices

a- Table of concept 5 3D sequential integration

v) Sequential 3D	Medium term: 5+	Long term/ 10+
a) Key research questions or issues		
Which application will benefit from very high density interconnections?	For IoT: intelligent local processing of the data to decrease the bandwith of data transmission. Neuromorphic architectures	
How to enable ultra-fine grain interconnections between layers?	CoolCube and sequential integration	Active 3D interconnection (programmable), DNA based interconnection for ultra-high density non bi-directionnal interconnection (to enable more close neighbours)
Thermally stable metallization, with low resistance	Interconnect metallization materials and associated diffusion barrier materials which provide low resistance and required stability throughout the temperature bonding cycles.	Co, silicided intercos
Reliability for low T gate stacks	Reliability in low temperature gate last integration	
Low thermal cycle device performance	Full low temperature CMOS transistors @ 500°C with good gate stack reliability	
Test methodology	For top and bottom characterization	
b) Potential for application or Application needs and Impact for Europe	…	…
CMOS-on CMOS for area scaling	SRAM memory block to block	Enabler for in memory computing architecture and neuromorphic
Imagers co-integrated with Logic	3D pixels for smart pixels (digital computing won't be at the local scale) Local memory storing	Smart pixels with local computing capabilities (each pixel will benefit from its local computing unit)
Computation immersed in memory		
Sensors on CMOS for IOT	NEMS, bolometers with the local analog parts with better performance than ASIC and better cost than co-integration	Multisensing platform
Beyond CMOS devices co-integration w/ CMOS	TFET, 2D TMDs, graphene	Qubit addressing
c) Technology and design challenges	…	…
Design tools optimized for Sequential 3D not available	Use of 2D existing tools to provide partially optimized (fold or shrunk techniques) 3D place and route tools.	Actual 3D place and route tools with 3D optimization at the logic gate scale.
Reducing parasitics in each implementation	Wire length decrease	Material optimization

Thermal management/selfheating mitigation	Layout optimization	Layout + heat spreaders + thermoelectric cooling, energy harvesters, new interconnection materials
Manufacturing challenges as in a) above	Same performance, same yield as 2D integration	Yield on multi-Tiers
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Top level device performance and reliability	Similar to 2D	…
Contamination management	In industrial fab with W or Cu interconnect	
System level performance vs 2D or 3DTSV	Same as 2D, or 3DTSV	> than 2D, or 3DTSV
System level area vs. 2D or 3DTSV	Same as 2D, or 3DTSV	< than 2D, or 3DTSV
System level cost comparison vs. 2D or 3DTSV including yield	Same as 2D, or 3DTSV	< than 2D, or 3DTSV
Multi-tier stacking	2 tiers	More than 2 tiers
e) Other issues and challenges, and interaction with other Tasks/WPs.	…	…
Link with WP2: enabler for neuromorphic computing/quantum computing Link with WP4: sensors+ cmos co-integration enabler Link with WP5: need for understanding system level benefit of 3D sequential options Link with WP6: development of low resistance, thermally stable BEOL materials; low T processes: wafer bonding, epi, gate stack materials/interfaces development for low T.		

b- Competitive situation for concept 5 3D sequential integration

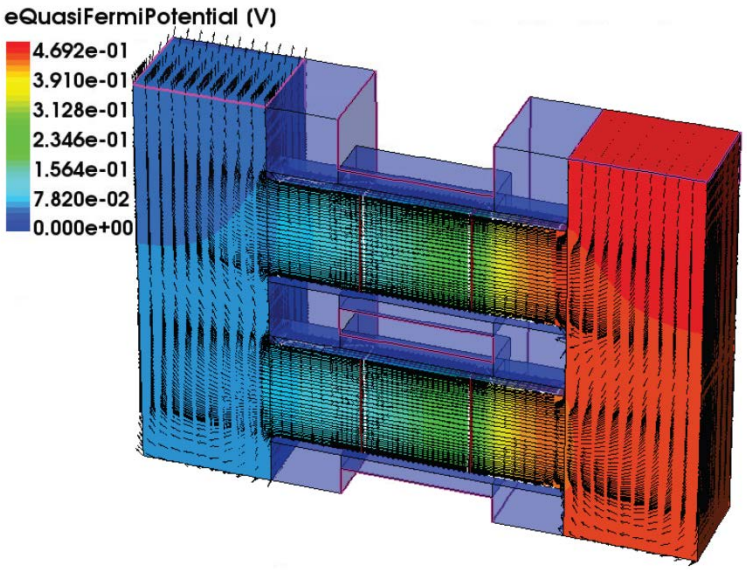
3D sequential integration is a very interesting approach for the following developments: CMOS-on CMOS for area scaling, Imagers co-integrated with Logic, Computation immersed in memory, Sensors on CMOS for IoT, Beyond CMOS devices co-integration w/ CMOS.

c- Recommendations for concept 5 3D sequential integration

- To define which applications will benefit from very high density interconnections (IOT, neuromorphic…)
- Development of a 3D place and route tool
- 3D sequential can combine any CMOS from bulk planar to Finfet or FDSOI…
- FDSOI and 3D integration can respond to future neuromorphic and quantum computing approaches

V.3.1.5.6. Concept 6: Modelling/Simulations Tools (Main contributor Luca Selmi, University of Udine/IUNET)

Modelling and Simulation tools are needed for the proof of concept of new devices, benchmarking and screening of technology options, and assessment up to circuit level (DTCO). They are also very important in order to assist interpretation of experimental data and extraction of the physically meaningful parameters. They should be predictive of trends and give actual absolute average values and variability.



Simulation of electron quasi-Fermi potential and the current vector in a FinFET

a- Table of concept 6 Modelling/Simulations Tools

	Medium term: 5+	Long term: 10+
vi) Modelling and Simulation		
a) Key research questions/issues		
Modelling full band structure of confined (2D, 1D) materials of interest to enable electrostatics and transport studies	- DFT, TB, KP, EPM methods and related NP-EMA parameterizations of most promising materials	DFT, TB, KP, EPM methods and related NP-EMA parameterizations of most promising materials
Models suited to steer the selection of device architectures and of channel materials (FDSOI, FinFET, UTBB DG, GAA, NW, NSH, stacked NW, etc.) - Static performance (Ion, Ioff, SS, DIBL, VT, gm, Avi, etc.) - Dynamic performance (C_{ij}, T_{sw}, τ_{FO4}, f_T, f_{max}, etc.)	- quantum electrostatics models in 2.5D and 3D - Multi-valley Multi Sub-band models of layered structures including wave-function penetration - Semi-classical and quantum transport coupled electro-thermal models (including all relevant scattering mechanisms) - Almost arbitrary geometry, material ($sSi_xGe_{(1-x)}$, GeSn, III-V), orientation and strain combinations	For winning solutions - Extension to transient time-dependent and time-harmonic small signal solutions - Inclusion in TCAD
Models of novel steep-slope device concepts for ULP electronics integrating new materials and suited for the selection of most promising options - Attention to leakage phenomena	- Heterojunction tunnel FETs - Ferro- and Piezo FETs - 2D materials FETs - Calibration to experiments	For most promising solutions - Non-ideal effects (traps, etc.) - Extension to transient time-dependent and time-harmonic small signal solutions - Inclusion in TCAD
Models for 3D vertical transistor stacking and related parasitics (resistances and capacitances)	Multiscale approaches combining accurate physical description of the channel and access regions with large scale DD models for parasitics (change of carrier gas dimensionality, ultra-small contacts, etc.)	
Simulation of variability, fluctuations, impact of traps and defects in nanoscale devices in Silicon and in new channel/dielectric materials	- Atomistic descriptions of gate dielectrics, interfaces, barriers, defects, traps, surfaces and link to continuum models for selected devices/materials - Statistical models for most promising devices	Progress toward full atomistic descriptions of nanoscale devices (DFT, TB, etc.)
Reliability modeling in new material systems (HCI, BTI, …)	Identification of degradation mechanisms and degradation models	Implementation of degradation models in design tools
Process modeling for new materials, support to DTCO	Requirements will be application specific	Requirements will be application specific
b) Potential for application or Application needs and Impact for Europe	…	…
Accelerate development and strengthen competitive advantage	…	…

in the field of ULP technologies		
Modeling and simulation SMEs in Europe form a small but healthy ecosystem (GSS, GlobalTCAD, TiberTCAD, NextNano, Quantavis, QuantumWise, MDlab, etc.)	Potential for further growth (atomistic, multiscale, reliability, …)	Consolidation of the M&S SME sector ?
"Modeling Technology" transfer from academia to industry Knowledge transfer to large research laboratories and industry	Integration of advanced research tools in general purpose TCAD platforms	- Ability to attract bright minds to the field of nanoelectronics M&S - Ability to maintain high quality education in applied math and physics subjects
c) Technology and design challenges		
Model verification and experimental calibration at different levels of physical detail		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
Physical device dimensions and computational dimensionality of manageable problems (e.g.: length, cross section, volume, no. of materials, regions, atoms, number of eigenstates, number of particles, wall clock time, CPU time)	Steadily getting better because of improvements in computing resources and efficiency of simulation methods	Steadily getting better because of improvements in computing resources and efficiency of simulation methods
Ability to incorporate all relevant physics	FoMs will be technology dependent	FoMs will be technology dependent
Ability to achieve the degree of accuracy required by applications (device design, benchmarking of technologies, etc.)	FoMs will depend on degree of technology maturity, application and type of device	FoMs will depend on degree of technology maturity, application and type of device
Computational resources accessible to academic, research institute and industrial environments	Improved because of evolution in conventional computing technology and related costs	Distributed scientific computation?
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Memory modelling	…	…
Automotive and Energy: Verified and calibrated models down to TCAD level for large bandgap materials (e.g. SiC, GaN, etc.)	TCAD compact models for material properties and physical processes	Widespread use of TCAD in design of electron devices for the applications
Sensors: dependable simulation of analyte diffusion and transduction processes including statistical aspects	- Solid/liquid electrolyte materials and interface models available in multiscale-multiphysics and TCAD simulation tools - Coupled analyte diffusion / transport modeling	- Models for functionalization layers responsible of selectivity - Models for analytes - Broader usage of commercial and ad-hoc simulation tools of transduction processes - Achieve simulations "predictive" of trends

		observed in actual devices and suited to interpret the measured statistics

b- Competitive situation for concept 6 Modelling/Simulations Tools

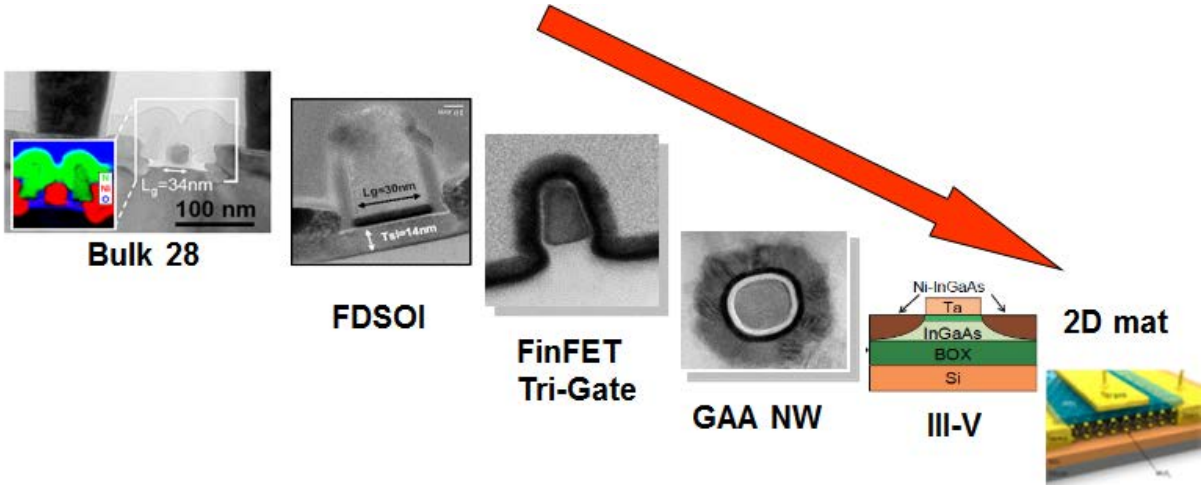
The modelling and simulation tools are of fundamental interest in order to speed-up technological optimization and reduce the cost of technology development. European teams have a very strong expertise in this field.

c- Recommendations concept 6 Modelling/Simulations Tools

- Promote dedicated M&S projects in application areas of interest for the European nanoelectronics community (ULP electronics, power devices, nano-bio sensing, neuromorphic memory, quantum computing, etc…)
- Identify M&S needs well in advance, systematically devote adequate share of resources, also by embedding modeling in all technology projects
- Privilege approaches that account for arbitrary geometry and all relevant physics, e.g. multi-scale, valley, subband, electrostatics of layered structures with wavefunction penetration, transport models comprehensive of tunneling and all relevant scattering mechanisms (remote-X, SR).

V.3.1.5.7 Concept 7: Characterization Tools (Main contributor Gérard Ghibaudo, CNRS/Grenoble INP)

CMOS technologies evolve from bulk to FDSOI/FinFET and Nanowires due to improved electrostatic control, better scalability and lower variability, but increasing issues of transport and interfaces in Ultrathin Bodies and new materials. Therefore, reliable characterization methods have to be developed for the next generation of nanoscale devices.



Evolution of Transistor architectures and Channel materials for ultimate MOSFET integration

a- Table of concept 7 Characterization Tools

	Medium term: 5+	Long term: 10+
vii) Key Challenges in Electrical Characterization		
i) Nanowires		
• Specific test structures with multifingers necessary for increase device area especially for vertical NW with short channel features.	X	X
• In III-V gate stack, issue with border trap characterization by CV & Gw techniques on large area, LF noise proves efficient even on small area devices…	XX	X
• III-V channel transport properties: Hall effect test structure for free carrier density assessment vs total carrier density from CV data, Hall mobility vs effective mobility, low temperature studies for scattering mechanisms identification…	XX	
• Similar methods should apply to 2D materials with critical issues on interface (LF noise, CV & Gw techniques, current DLTS, Fast IV for hysteresis analysis…). Any specificity for 2D materials should be pointed out.		X
ii) FDSOI/FinFET		
• For electrical characterization, it should be mentioned that most of existing I-V and C-V measurement tools have good enough resolution and accuracy for DC and low frequency range. RF test equipment currently available in industrial and academic labs are also of sufficient accuracy up to 100GHz frequencies for S parameter measurements and subsequent data de-embedding exploitation.	X	X
• Stack parameter extraction and associated wafer scale variation: Challenge due to multiple layers combining front gate dielectric, channel, BOX and ground plane, assessment of work function for front and back gates, discriminate charge and dipole contribution in front HK dielectric, Solutions: confront TCAD simulation results and statistical CV data on large area MOSFET at wafer scale, use of specific CV test structures with variable EOT over wafer (beveled HK thickness)…	X	
• Ferrolectric and negative capacitance MOSFET: challenge in polarisation assessment using specific test structure (conducting layer in between Cox and Cfe capacitance, cf Rusu 2012) or using standard Sawyer-Tower circuit providing polarization vs field characteristics, associated strain measurements should be desirable for piezo-Ferro materials…	XX	X

• Transport properties (mobility, velocity) and parameter extraction in channel of nano MOSFETs: Challenge due to parameter extraction (channel vs access), finding scattering mechanisms and ballistic contribution, solution by RF split CV, magnetoresistance measurements, low temperature characterization…Improved parameter extraction are needed for Rsd assessment, especially if they depend on gate voltage (Rtot vs L method, Y function method, dRtot/dL method…). Need for appropriate parameter extraction methods adapted to low voltage operation with Vdd close to threshold voltage (Vdd<0.4V). Confrontation to TCAD simulation results will also be worthwhile for validating extraction methodologies.	X	
• Intrinsic and parasitic Capacitances of nano MOSFETs: Challenge due to small capacitance values, solutions: use of multifinger MOSFET structures, use of RF CV technique based on S parameter measurements…	X	
• Strain/stress in nano MOSFETs: Challenge due to nanoscale probing along the channel for correlation to mobility enhancement using holographic TEM, HRTEM, NBED, PED, CBED techniques…	X	
• Interface quality and reliability related to initial and stress induced traps: Challenge due to small area of nano MOSFETs, device-to-device stochastic variations, solutions: use of multifinger MOSFET structures, use of dedicated techniques applicable to small area such as LF noise, AC transconductance, drain current DLTS,… requirement for statistical measurements…	X	
• Variability in nano MOSFETs: Challenge due to requirement for statistical measurements, discrimination of local vs global variability sources, time dependent instability and dynamic variability measurements at µs to ns time scale, solutions: use of specific methodologies based on DC drain current variance analysis vs bias, use of addressable array structures for enhanced statistics, use of ultra-fast I-V measurements with specific test structures …	X	
• Self heating effect (SHE): Challenge due self heating arising from BOX, need for test structures for measuring channel temperature, discrimination of SHE impact on reliability…	X	
iii) TFET		
• Proper parameter extraction methodology needed due to special BBT operation, assessment of local drain current variability needed, impact of interface quality and junction doping/gap profile on BBT, correlation to physical characterization….	XX	X
• A special attention should be paid to determine whether carrier injection on either side of the device occurs via band-to-band tunneling or single carrier tunneling through a Schottky barrier. This can be achieved by analyzing the Id-Vd output characteristics under	XX	X

forward and reverse operation. • Better assesment of trap assisted tunneling in TFET operation.	XX	X
iv) FinFET		
Idem FDSOI with specific multifinger test structure needed.	X	
v) Memories		
Specific challenges in characterization: ultra-fast tool for programming and reading, LF noise and RTN, cycle-to-cycle and device-to-device variability, physical characterization of filamentary nature by local AFM probe for OXRAM/CBRAM, data retention after thermal acceleration test for emerging memories…	X	
vi) 3D sequential integration		
Idem FDSOI with also Specific challenges in characterization: differentiate top vs bottom layer devices in terms of transport, interface and variability properties…	X	

b- Competitive situation for concept 7 Characterization Tools

The characterization tools are of fundamental interests for technological optimization. European labs have a very strong expertise in this field.

c- Recommendations for concept 7 Characterization Tools

-CV/capacitance-voltage measurements are still feasible but specific test structures are needed (multi fingers or RFCV) on FDSOI, FinFET, Nanowires…
-MOSFET parameter extraction requires the development of new methods and on new 2D materials, III-V, Ge,… The source-drain resistance Rsd is a key parameter
-Mobility and transport parameters are measurable on standard MOSFETs down to very small Lg but the magneto-resistance is very useful and should be developed
-Traps and interface quality can be assessed even on very small area devices and methods using LFN/low frequency noise or RTN/random telegraph noise are becoming very useful (C-V, CP/charge pumping are area limited unless multi finger is used)
-Stochastic Variability becomes critical and must be measured in static and in dynamic modes => problems for non mature technologies but also for TFET, FeFET….

V.3.1.6 Synergies with other topics

Important links of WP3/Nanoscale FETs with WPs 2, 4, 5 and 6.

V. 3.1.7 Recommendations for Task 3.1 Nanoscale FET

-For Nanowires, identify the best material and geometry options for logics (high-speed as well as low-power), develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar), and consider the 3D aspects of processing

-For FD SOI, develop differentiated options (RF, Embedded Memories, Imaging or molecules sensors) on FDSOI (applications for automotive, IoT, smart sensors…), ULP design (Vd<0,4V) for IoT market (wearable, medical…), and 3D integration for future neuromorphic and quantum computing approaches

-For FinFET, develop co-integration of different channel materials, low contact resistivity and high strain solutions, improve finFET analog performance

-For non-charge-based Memories, overcome the HRS broadening for OxRAM, improve the process for GST patterning for PCRAM, develop new materials enabling horizontal scaling

-For 3D sequential integration, define which applications will benefit from very high density interconnections (IOT, neuromorphic…), and develop a 3D place and route tool

-For Modelling/Simulation and Characterization, develop new tools taking into account all the new materials, technologies and device architectures in order speed-up technology optimization and reduce the cost of technology development.

V. 3.2 Connectivity (T3.2)

V. 3.2.1 Executive summary

The connectivity functions are everywhere, making the link between all other electronic functions. From the sensors and actuators to the processors and microcontrollers, from the sensor nodes to the gateways, from the gateways to the cells from the cells to the data centres, and all over the world. Inside each of

these units, the connectivity links the computers to the memories, the core of multicores in High performance computing applications, and the peripheral devices to the central computing units.

The connectivity functions can be differentiated depending on the range and the nature. The nature of such function are wireless (in radio frequency mmW, THz bands, or visible light), or wireline (in copper or optical fiber). The range of such functions can be sorted out depending on the distance, the ultra-short range, is in the µm to cm distance; the short range is under 100m, while the long range covers distances over 100m.

Presently the largest connectivity market activity is dedicated to data communications, especially for cellular (WAN), WLAN, WPAN, NFC, and incoming WSN and IoT communications. Then we can distinguish 2 other market areas, especially in Europe, even if they use, or are be connected to the first one: the automotive market which is at the beginning of the autonomous vehicle revolution, and the "health & security" market which will transform drastically our way of life in the next decades.

In the data communication field, we can distinguish three main families using the link distance criteria, the outdoor and cellular, for example 5G and future generations, the indoor communication mainly represented today by the WiFi links, and a third which is not visible to the consumer, which can be called the In Devices one, or the communication between dies and packages in an equipment.

V. 3.2.2 Relevance and competitive value

If we look at the expected evolution of the technologies, the improvements are primarily seen at the functional device level, such as Power Amplifiers, Low noise Amplifiers, Antennas in Wireless field, or Modulator Drivers, Laser Drivers, Trans Impedance Amplifiers, Modulator, Laser Diodes, and PIN diodes in Wireline field, we have to implement for the different transceivers. In this domain, the More Than More axe is privileged, (actives, NEMs and MEMs, and passives components), and the multi-physics assembly can bring advantages versus present solutions.
On the other hand, we can notice that for all transceivers, we have common functions including the Phase Frequency generation, Local Oscillators in Wireless field, Phase Frequency Lock Loop and Clock Recovery in Wireline field. For these functions the expectation is mainly the same whichever the selected communication link. In this domain, the More Than More axe is also privileged, (actives, NEMs and MEMs, and passives components). As previously, the multi-physics assembly can bring advantages versus present solutions.
Concerning the signal modulations and demodulations, the improvement comes primarily from the design, whether the functions are done in an analog approach or a digital one. Then, depending on the approach, the technology expectations are different. In an analog approach, the active More Than More axe is privileged, and, in a digital or "digital like" approach, the More Moore will bring the cost and the efficiency.

How to evaluate the Figure of Merit of a function?
This question is one of the main issues we face in Connectivity, as it is very difficult to compare wireless or wireline solutions. The proposed approach, which is under discussion with NEREID experts, is the following:
Before adopting a particular solution, an industrial concern needs to evaluate the efficiency of a given function versus the cost of this function.
Starting from this ratio, we can try to define what the efficiency of a connectivity function is:
The efficiency could be the data rate multiplied by the range moderated by the error rate and divided by the power consumption.
We can call this efficiency the *Technical Efficiency FOM*.
Next we determine what the cost of such a function is:
The cost is very complex to estimate, as we don't have the correct information unless we are in volume production. As an estimate, it could be composed of the fabrication cost (initial cost), depending on the technology cost, the packaging cost, the test cost, and the exploitation cost. This will be called the *Economic FOM*.

The proposed formulae for the technical efficiency FOM is the following one:

FOM = (Datarate(Gbs)×$Distance^2(m)$×1/BER)/(Psupply(W))

Concerning the cost of the function, the T32 NEREID experts need more discussions in order to propose an Economic FOM.

V. 3.2.3 Vision

The connectivity challenges are not limited to the physical specifications, but also to the privacy of exchange data, the security of a communication and the safety of the consequence of the exchanged data. We will try to explain in few sentences these different challenges:

-The Physical quantities for the next 5 years:

- Traffic multiplied by 10 000
- Energy per Bit divided by 1000
- Capacity per area multiplied by 10 or connection density per Km² multiplied by 10
- Mobility up to 500Km/h
- Data Rate average per connection 100Mbs
- Data Rate peak per connection 10Gbs
- Latency less than 1ms
- Spectrum efficiency multiplied by 3
- Connected devices multiplied by 100 (without IoT connection).
- IoT connections more than 100 / room

-Privacy and security:

- No RF interception of the ultra-short range Communications.
- Multi-Frequency, Multi-Mode dynamic Coding for wireless communications.
- …

-Safety:

- Redundancy of the communications
- Safe from hacking threats.
- …

V. 3.2.4 Scope and ambition

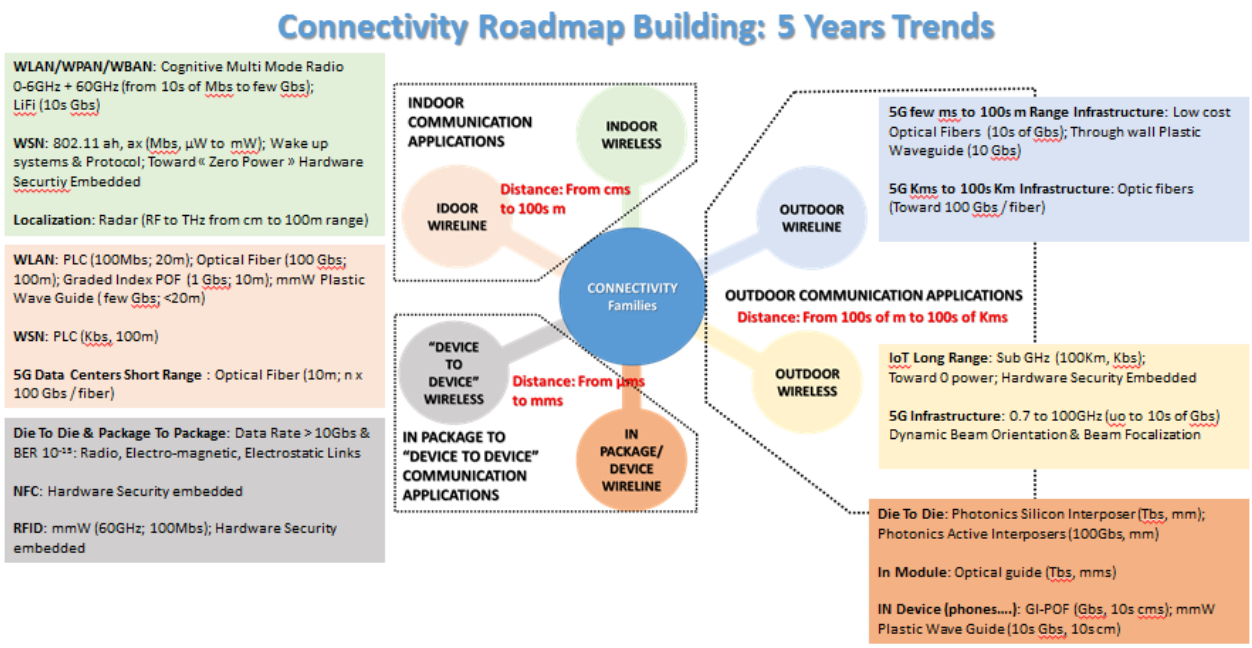
The Connectivity roadmap will present the medium and long term applications and their impact for each communication range sorted by category, and then will present the technology and design challenges to target these applications. At the end of the table the FOM formulae is given, and will be evaluated in the second part of the project.

V. 3.2.5 Main Concepts

The next figure presents the concepts applied to the 5 years roadmap. At the centre of the figure the connectivity families are sorted out taking into account the distance and the nature of the links. Two main natures are defined, either the link is guided, by extension we speak about Wireline, or the link is in the air, and then we speak about Wireless. Three distance ranges separate the applications. If the distance is very short, then we speak about In Package and Device to Device communications; if the distance is in the centimetre metre to hundreds of metres range, we can put this category as the Indoor communications, and finally, from hundreds of metres to Kilometres we speak about Outdoor applications.

Sorting out the connectivity, we can define 6 different concepts, which will be presented in the next tables:

- The Outdoor Wireless Applications
- The Outdoor Wireline Applications
- The Indoor Wireless Applications
- The Indoor Wireline Applications
- The Device to Device Wireless Applications
- The In Package/Device Photonics Wireline Applications



Connectivity families, and their main 5 years objectives.

V.3.2.5.1. Concept 1: The Outdoor Wireless Applications

a- Table of concept 1 The Outdoor Wireless Applications

Concepts/Technologies	Medium term: 5+	Long term: 10+
Concept 1: OUTDOOR WIRELESS APPLICATIONS		
a) Key research questions or issues		
- IoT Long Range	Sub GHz (100Km, Kbs) Ultra low power (<mW)	Sub GHz (100Km, Kbs) Zero power (<100µW) Hardware security embedded
- Cellular Up & Dwn Links	0.7 to 100GHz (10 Gbs) With dynamic Beam Orientation	Up to THz (10s of Gbs) With Dynamic Beam Orientation
- Fix Mini Cell to Mini Cell & Fix Mini Cell to Cell Backhauling	mmW to THz bands (10s of Gbs) with Beam Focusing	mmW to THz bands (100 Gbs) with Beam Forming
- Mobile Mini Cell to Mobile Mini Cell; Mobile Mini Cell to Cell Backhauling	mmW bands (10Gbs) with Dynamic Beam Orientation	mmW bands (10s of Gbs) with Dynamic Beam Orientation
b) Potential for application or Application needs and Impact for Europe		
5G+ Network:	Big Data, Cloudification: European solution for European Business and population.	Full Distributed Cloud; Ad-hoc / opportunistic; local cloud (clustering); multi-cloud: European Independence.
Environmental survey:	Forests, water, snow …. Surveys: Better European Environment control.	Global multi physics environment survey: Better disaster prevention.
Autonomous objects:	Driving aid, drones automation…: Lifes saved; injured number reduction; travel time reduction; CO2 emission reduction.	Dynamic automated data driven decision & vehicle action: Safe transport system. Low resource consumption transport system.
c) Technology and design challenges		
Power Amplifier Technology challenges		
Fmax:	More than 0.5 THz	More than 1THz
Current density:	More than 0.1A over wide gate area respecting Fmax.	More than 0.1A over wide gate area respecting Fmax.
Voltage breakdown:	More than 5V	More than 5V
Linearity:	High	Very High
Re-Configurability: Power Switch Transistors	Ron-Coff < 100fs	Ron-Coff < 30fs
Selectivity: Passives	High Q	Very High Q
Integration: Passives & Packages	Partially integrated in RDL	All integrated in the RDL level
Ultra-low capacitor ESD	Up to 30GHz	Up to 100GHz
Power Amplifier Design challenges		
Wide Band	XX	XXX
PAE	XX	XXX
mmW to THz	X	XXX
Phase shifting	X	XXX
Switch Band	XX	XXX
RF and mmW ESD management	X	XX
RF and mmW BIST	X	XX

RF and mmW Built In Self Control	X	XX
<u>Modulator – De-Modulator Technology challenges</u>		
Re-Configurability: Multi-mode Multi frequencies transceivers:		
FT:		
Variability:	More than 0.5THz	More than 1 THz
Components density:	Allowing Design controlled	Allowing Design controlled
Switches Transistors:	High (under 15nm gate)	Very High (under 10nm gate)
Vdd:	Ron-Coff < 50fs	Ron-Coff < 10fs
Ioff:	Under 0.6V	Under 0.4 V
	Low.	Very Low.
Linearity:		
Selectivity: Passive	Very High	Extremely High
Capacitor density: Linear capacitor.	High Q	Very High Q
ESD at high frequency and low voltage	High density per µm²	Very High density per µm²
	X	XX
<u>Modulator – De-Modulator Design challenges</u>		
Wide Band and High Dynamic ADCs at Low Power.		
Design by Mathematics and Digital approach for	X	X
Analog functions	X	XXX
Reconfigurability to Cognitive Radio	X	XX
mmW power consumption reduction	X	XX
Systematic BIST	XX	XXX
Built In Self Control	X	XX
<u>LNAs Technology Challenges:</u>		
NFmin:		
Linearity:		
Re-Configurability:	Less than 1dB @ 100GHz	Less than 1dB @ 200GHz
Selectivity: Passives	High	Very High
Ultra-low Noise ESD	Ron-Coff < 100fs	Ron-Coff < 30fs
	High Q	Very High Q
<u>LNAs Design Challenges:</u>	Up to 30GHz	Up to 100GHz
Full Duplex Transceiver: TX isolation		
Wide Band LNA		
mmW to THz	More than 90dB @ 6GHz	More than 90dB @ 100GHz
Frequency Tuning	XX	XXX
Switch Band	X	XX
Noise cancellation	X	XX
RF and mmW BIST	XX	XXX
RF and mmW Build In Self Control	X	XX
	X	XX
<u>Phase Frequency Generation Technology Challenges:</u>		
1/F noise: Cut Frequency		
Fmax:		
Selectivity: Passives and resonators	100s of Hz @ 6 GHz	100s of Hz @ 100 GHz
Stability:	More than 0.5 THz	More Than 1THz

Tuning range: Re-Configurability: Switch transistors FT: Voltage breakdown: Capacitor density: Linear Capacitor Phase noise reduction White noise reduction VCO FOM <u>Phase Frequency Generation Design Challenges:</u> Frequency Agility ADPLL Jitter noise reduction Reconfigurability Tunability <u>Antennas Technology Challenges:</u> Dielectric Resonator Antennas Lenses Plastic antennas Polarization Efficiency Gain/ Antenna element <u>Antennas Design Challenges</u>: Antennas Array: Mixed Array and Lenses: Beam Forming: Dynamic orientation. Tunability: Switched Bands:	High Q in GHz range Equivalent to Quartz but in GHz range 15% Min Ron-Coff < 50fs More than 0.5 THz More than 2V High density per µm² X X 190 dBc/Hz/mW @6GHz X XX X XX X Low cost material @10GHz Low cost mmW Lenses X X High More than 0dBi XX X XX 20% XX	High Q in 10s of GHz range Equivalent to Quartz but in 10s of GHz range 30% Min Ron-Coff < 10fs More Than 1THz More Than 2V Very High density per µm² XX XX 195 dBc/Hz/mW @6GHz XX XXX XX XXX XX Low cost material @100GHz Low cost sub-THz Lenses XX XX Very High More than 3dBi XXX XX XXX 40% XXX
d) Definition of FoMs (quantitative or qualitative) or planned evolution		
FOM=(Data_rate(Gbs)×$D^2(m)$×1/BER)/(Psupply(W)) IoT Long Range FOM: Cellular Up & Dwn Links FOM: Fix Backhauling FOM: Mobile Backhauling FOM:	**These FOMs will be estimated in the Second part of NEREID Project**.	
e) Other issues and challenges, and interaction with other Tasks/WPs.		

b- Competitive situation for Concept1 The Outdoor Wireless Applications

The Long Range IoT applications market is in rapid expansion, and many standards are yet proposed in or outside of the 5GPPP association, such as Sigfox, LoRa outside, LTE-M inside. Concerning the 5G

wireless applications, the Cells to Cells communications are in competition with the wireline ones. There should be a balance between the wireless and the wireline market for these applications, depending on the cell characteristics, with small and pico-cells base stations using wireless, while big base stations will continue to use wireline. The last 5G link between the mobile and the base market is in very high growth rate, as the number of users, and the bandwidth per user will increase rapidly in the next years.

c- Recommendations for Concept1 - The Outdoor Wireless Applications

In this concept, we will have two different technology needs, the one for IoT long range is oriented to the Ultra-Low power requirements, and the integration of all the functions in one node; while the 5G wireless applications need high speed, high power, high bandwidth, and millimeter wave (mmW), which means that technologies which will serve such applications are high end technologies.

V.3.2.5.2 Concept 2: The Outdoor Wireline Applications

a- Table of concept 2 The Outdoor Wireline Applications

Concepts/Technologies	Medium term: 5+	Long term: 10+
Concept 2: OUTDOOR WIRELINE APPLICATIONS		
a) Key research questions or issues		
Cellular Base Station to Base Station	Optical fibers: 100 Gbs / fiber	Optic (n x 100 Gbs / fiber)?
Fix Mini Cell to Mini Cell, Fix Mini Cell to Cell Base Station	Low cost Optical Fibers (10s of Gbs); Through wall Plastic Waveguide (10 Gbs)	Low cost Optical Fibers (100 of Gbs); Through wall Plastic Waveguide (10s of Gbs)
Cell Base Station to Data Centers & Data Centers Long Range	Optical Fibers: 100 Gbs / fiber	Optical fibers: n x 100 Gbs / fiber
Long haul	Optical fibers: 40 Gbs / fiber	Optical Fibers: 100 Gbs / fiber
b) Potential for application or Application needs and Impact for Europe		
5G+ Network & 5G+ Servers: WWAN: FTTx:	Big Data, Cloudification: European solution for European Business and population Global Network: Web 3.0 Sub-Urban Network deployment: More Citizen will have RAN 2.0 access	Full Distributed Cloud; Ad-hoc / opportunistic; local cloud (clustering); multi-cloud: European Independence Global Network: Web 4.0 Local Rural network deployment: Increasing the citizen number accessing to RAN 3.0.
c) Technology and design challenges		
Optical Modulator or Laser Driver technology challenges FT: Voltage breakdown: Linearity:	 More than 0.5 THz More than 2V	 More than 1 THz More than 2V

Re-Configurability:	High Voltage linearity Ron-Coff < 100fs	High voltage linearity Ron-Coff < 30fs
<u>Optical Modulator Or Laser Driver Design challenges</u>		
Multilevel Modulations.		
Pre-emphasis capability	X	XX
Power consumed reduction	X	XX
	XX	XXX
<u>Modulations and Demodulation technology challenges:</u>		
Re-Configurability : Multimode		
FT:		
Components density:	More than 0.5 THz	More than 1 THz
Switch transistors:	High (under 15nm gate)	High (under 10nm gate)
Vdd:	Ron-Coff < 50fs	Ron-Coff < 10fs
Ioff:	Less than 0.6V	Less than 0.4V
	Low	Very Low
<u>Modulations and Demodulation Design challenges:</u>		
Multilevel Modulations.		
Power consumed reduction	X	XX
Equalization, Post emphasis	XX	XXX
CDR low power	X	XX
Low jitter	X	XX
	X	XX
<u>Trans Impedance Amplifiers Technology challenges:</u>		
Current noise density:		
FT:	Low	Very Low
Re-Configurability:	More than 0.5 THz	More than 1 THz
Linearity:	Ron-Coff < 50fs	Ron-Coff < 10fs
Wide Band	High current linearity	Very high current linearity
	Wide	Very Wide
<u>Trans Impedance Amplifier Design Challenges</u>:		
Highly linear TIA		
High Dynamic range (Optical offset compensation)	XX	XXX
	XX	XXX
<u>Frequency Generation And Clock Recovery Technology challenges</u>:		
Fmax:		
Stability:	More than 0.5 THz	More than 1 THz
Tuning range:	High	Very High
Re-Configurability: Switch transistors	30% Min	50% Min
FT:	Ron-Coff < 50fs	Ron-Coff < 10fs
Voltage breakdown:	More than 0.5 THz	More than 1 THz
Capacitor density: Linear Capacitor	More than 0.7V	More than 0.5V
	High density per µm²	High density per µm²
<u>Frequency Generation And Clock Recovery Design challenges</u>		
Digital approach	XX	XXX
Ultra-Low Jitter	X	XX
Stability	X	XX
Low Power High speed	X	XX
<u>Photodiode technology challenges:</u>		
Responsivity		

Input capacitor Black current 3D assembly <u>Laser Challenges</u>: Cost Radiated Temperature Size <u>Optical Modulators technology challenges:</u> Extinction ratio Actuation	0.85 Few 10s fF Very low High efficiency Low (few $) Low (less than 30 °C) Small package 6dB 2V range actuation	0.95 Few fF Extremely Low Very High efficiency Very low (few 10s of cents) Very low (less than 10°C) Very small (package) 12dB 1V range actuation.
d) Definition of FoMs (quantitative or qualitative) or planned evolution		
FOM=(Data_rate(Gbs)×$D^2(m)$×1/BER)/(Psupply(W)) Cellular Base Station to Base Station FOM: Fix Mini Cell to Mini Cell, Fix Mini Cell to Cell Base Station FOM: Cell Base Station to Data Centers & Data Centers Long Range FOM: Long haul FOM:	**These FOMs will be estimated in the Second part of NEREID Project**.	
e) Other issues and challenges, and interaction with other Tasks/WPs.		

b- Competitive situation of concept 2 - The Outdoor Wireline Applications

The 5G wireline applications, from the Cells to Cells communications to long Haul communications are partially in competition with the wireless ones, for their “short range” part. In this range there should be a balance between the wireless and the wireline market for these applications, depending on the cell characteristics, small and pico-cells base stations will use wireless, while big base station will continue to use wireline. Concerning the other aspects of wireline communications there is no other competitive solutions today.

c- Recommendations of concept 2 - The Outdoor Wireline Applications

The 5G wireline applications need high speed, high power, high bandwidth, and Photonics, this means that technologies which will serve such applications are high end technologies.

V.3.2.5.2. Concept 3: Indoor Wireless Applications

a- Table of concept 3 Indoor Wireless Applications

Concepts/Technologies	Medium term: 5+	Long term: 10+
Concept 3: INDOOR WIRELESS APPLICATIONS		
a) Key research questions or issues		
- WLAN/WPAN/WBAN - WSN - Localization	Cognitive Multi Mode Radio 0-6GHz and 60GHz band; LiFi (10s Gbs); P2P over 100GHz bands; New sub-THz band Cooperative sensing, cooperative radio; Towards « Zero Power » Hardware Securtiy embedded. Radar (RF to THz); UWB ; Ultrasound; Impulse light	Cognitive Multi Mode WLAN over 100GHz; LiFi (100s Gbs); P2P in sub-THz band « Recycling material » for radio « Zero power node »; Security / Safety / Privacy Embedded. Multi physics fusion
b) Potential for application or Application needs and Impact for Europe		
Fitness: Healthcare: Home safety & security Public space safety & security Factory 4.0 Autonomous objects	Performance sensing & benchmarks: Consumer Market E-Monitoring: Ageing people maintained at home. E-Survey: Domestic accidents and burglaries prevention E-Survey: aggressions, theft, terrorist actions prevention. Machine automation: reduction of human intervention in the production process. Mono-function autonomous machine: Reducing laborious tasks at home.	Enhanced human performances: Consumer Market E-Hospital: Specialist intervention through the Net. Data Analysis and decision making. Autonomous Home protection: Data Analysis and decision making Autonomous Public Protection: Multi source data analysis and decision making. Factory 4.0: No Human intervention. CPS: First generation of multi functions robots.
c) Technology and design challenges		
<u>Power Amplifier Technology challenges</u> Fmax: Voltage breakdown: Linearity: Re-Configurability: Power Switch Transistors	More than 0.5 THz More than 2V High Ron-Coff < 100fs	More than 1THz More than 2V Very High Ron-Coff < 30fs

Selectivity: Passives	High Q	Very High Q
<u>Power Amplifier Design challenges</u>		
Wide Band	XX	XXX
PAE	XX	XXX
mmW to THz	X	XXX
Phase shifting	X	XXX
Switch Band	XX	XXX
<u>Modulator – De-Modulator Technology challenges</u>		
Time and Frequency domain Approach:		
FT:		
Variability:	More than 0.5THz	More than 1 THz
Components density:	Allowing Design controlled	Allowing Design controlled
Switches Transistors:	High (under 15nm gate)	Very High (under 10nm gate)
Vdd:	Ron-Coff < 50fs	Ron-Coff < 10fs
Ioff:	Under 0.6V	Under 0.4 V
	Low.	Very Low.
Current Inversion Analog Approach:		
FT:		More than 1 THz
Variability:	More than 0.5 THz	Very low in weak inversion
Linearity:	Very low in weak inversion	High
Selectivity: Passive	High	Very High Q
Capacitor density: Linear capacitor.	High Q	Very High density per μm^2
	High density per μm^2	
<u>Modulator – De-Modulator Design challenges</u>		
Design by Mathematics and Digital approach for		X
Analog functions	X	XXX
Reconfigurability to Cognitive Radio	X	XXX
Weak inversion design	XX	XXX
RF & mmW in die	XX	
<u>LNAs Technology Challenges:</u>		
NFmin:		Less than 1dB @ 200GHz
Linearity:	Less than 1dB @ 100GHz	Very High
Re-Configurability:	High	Ron-Coff < 30fs
Selectivity: Passives	Ron-Coff < 100fs	Very High Q
	High Q	
<u>LNAs Design Challenges:</u>		
Full Duplex Transceiver: TX isolation		More than 90dB @ 100GHz
Wide Band LNA	More than 90dB @ 6GHz	XXX
mmW to THz	XX	XX
Frequency Tuning	X	XX
Switch Band	X	XXX
Noise cancellation	XX	XX
	X	
<u>Phase Frequency Generation Technology Challenges:</u>		
1/F noise: Cut Frequency		10s of Hz
Fmax:	100s of Hz	More Than 1THz
Selectivity: Passives and resonators	More than 0.5 THz	High Q in 10s of GHz range
Stability:	High Q in GHz range	Equivalent to Quartz but in

Tuning range: Re-Configurability: Switch transistors FT: Voltage breakdown: Capacitor density: Linear Capacitor <u>Phase Frequency Generation Design Challenges:</u> Frequency Agility ADPLL Phase noise reduction White noise reduction Reconfigurability Tunability <u>Antennas Technology Challenges:</u> Antenna on die with Semi-conductor substrate: Antenna in Package on Organic substrate: Antenna in a Module on ceramic substrate: Antenna on Other Metamaterial: <u>Antennas Design Challenges</u>: Antennas Array: Antenna with reflectors Beam Forming: Dynamic orientation. Tunability: Switched Bands:	Equivalent to Quartz but in GHz range 15% Min Ron-Coff < 50fs More than 0.5 THz More than 2V High density per µm² X XX X X XX X 0dBi gain and □/n design approach Low cost mmW Low cost mmW Low cost mmW XX X XX 20% XX	10s of GHz range 30% Min Ron-Coff < 10fs More Than 1THz More Than 2V Very High density per µm² XX XXX XX XX XXX XX 0dBi gain and □/2n design approach Low cost sub-THz Low cost sub-THz Low cost sub-THz XXX XX XXX 40% XXX
d) Definition of FoMs (quantitative or qualitative) or planned evolution		
FOM=(Data_rate(Gbs)×$D^2(m)$×1/BER)/(Psupply(W)) WLAN FOM: WPAN FOM: WBAN FOM: WSN FOM: Localization FOM:	**These FOMs will be estimated in the Second part of NEREID Project.**	
e) Other issues and challenges, and interaction with other Tasks/WPs.		

b- Competitive situation of concept 3 - Indoor Wireless Applications

The Indoor wireless applications, from WBAN to WLAN through WSN are very open, with a huge standards competition currently ongoing, and the winning standards are not yet known. Whatever the outcome, all of these applications need more or less similar technology capabilities in the end.

c- Recommendations of concept 3 - Indoor Wireless Applications

From the WSN to the WLAN, all these applications require Energy efficiency and are oriented towards the Low power to Ultra-Low power technologies. Ultimately, they will integrate all the functions in a System-On-Chip approach.

V.3.2.5.3. Concept 4: Indoor Wireline Applications

a- Table of concept 4 Indoor Wireline Applications

Concepts/Technologies	Medium term: 5+	Long term: 10+
Concept 4: INDOOR WIRELINE APPLICATIONS		
a) Key research questions or issues		
- WLAN - WSN - Data Centers Short Range	Copper (Low power HDR); PLC (100Mbs; 20m); Optical Fiber (100 Gbs; 100m); GI-POF (1 Gbs; 10m); mmW Plastic Wave Guide (few Gbs; <20m) **will be completed in the Second part of NEREID Project** Copper (1m; 10s of Gbs) ; Optical Fiber (10m; n x 100 Gbs / fiber); GI-POF (1m; 1Gbs) mmW PWG(1m; 10Gbs)	Copper (ULP HDR); PLC (n x 100Mbs; 20m); Optical Fiber (100s of Gbs; 100m); GI-POF (10 Gbs; 10m); mmW PWG (n x 10Gbs; <20m) will be completed in the Second part of NEREID Project Copper (1m; 100Gbs) ; Optical Fiber (10m; 1Tbs / fiber); GI-POF (1m; 10 Gbs) THz PWG (1m; 10s of Gbs)
b) Potential for application or Application needs and Impact for Europe		
Home Automation: Factory Automation: 5G+ Data Center:	Multi physics Network: Reducing time transfer for data at home. Multi physics Network: Reducing time transfer for data in Factory Very high speed Network: for short range transfer.	Multi physics Network: Reducing decision making at home. Multi physics Network: for Factory 4.0 Very high speed Network: for RAN 3.0
c) Technology and design challenges		
Optical Modulator Or Coper line Driver technology challenges FT: Voltage breakdown: Linearity:	 More than 0.5 THz More than 2V High Voltage linearity	 More than 1 THz More than 2V High voltage linearity

Re-Configurability:	Ron-Coff < 100fs	Ron-Coff < 30fs
<u>Optical Modulator Or Coper line Driver Design challenges</u>		
Multilevel Modulations.	X	XX
Pre-emphasis capability	X	XX
Power consumed reduction	XX	XXX
<u>Modulations and Demodulation technology challenges:</u>		
Re-Configurability : Multimode		
FT:	More than 0.5 THz	More than 1 THz
Components density:	High (under 15nm gate)	High (under 10nm gate)
Switch transistors:	Ron-Coff < 50fs	Ron-Coff < 10fs
Vdd:	Less than 0.6V	Less than 0.4V
Ioff:	Low	Very Low
<u>Modulations and Demodulation Design challenges:</u>		
Multilevel Modulations.	X	XX
Power consumed reduction	XX	XXX
Equalization, Post emphasis	X	XX
CDR low power	X	XX
Low jitter	X	XX
<u>Trans Impedance Amplifiers Technology challenges:</u>		
Current noise density:	Low	Very Low
FT:	More than 0.5 THz	More than 1 THz
Re-Configurability:	Ron-Coff < 50fs	Ron-Coff < 10fs
Linearity:	High current linearity	Very high current linearity
Wide Band	Wide	Very Wide
<u>Trans Impedance Amplifier Design Challenges</u>:		
Highly linear TIA	XX	XXX
High Dynamic range (Optical offset compensation)	XX	XXX
<u>Frequency Generation And Clock Recovery Technology challenges</u>:		
Fmax:	More than 0.5 THz	More than 1 THz
Stability:	High	Very High
Tuning range:	30% Min	50% Min
Re-Configurability: Switch transistors	Ron-Coff < 50fs	Ron-Coff < 10fs
FT:	More than 0.5 THz	More than 1 THz
Voltage breakdown:	More than 0.7V	More than 0.5V
Capacitor density: Linear Capacitor	High density per μm^2	High density per μm^2
<u>Frequency Generation And Clock Recovery Design challenges</u>		
Digital approach	XX	XXX
Ultra-Low Jitter	X	XX
Stability	X	XX
Low Power High speed	X	XX
<u>Photodiode technology challenges:</u>		0.95
		Few fF

Responsivity Input capacitor Black current 3D assembly Laser Challenges: Cost Radiated Temperature Size Optical Modulators technology challenges: Extinction ratio Actuation	0.85 Few 10s fF Very low High efficiency Low (few 10s of cents) Low (less than 10 °C) Small (Over die integration) 6dB 2V range actuation	Extremely Low Very High efficiency Very low (few cents range) Very low (less than 5°C) Very small (over die integration) 12dB 1V range actuation.
d) Definition of FoMs (quantitative or qualitative) or planned evolution		
FOM=(Data_rate(Gbs)×$D^2(m)$×1/BER)/(Psupply(W)) WLAN FOM: WSN FOM: Data Centers Short Range FOM:	**These FOMs will be estimated in the Second part of NEREID Project.**	
e) Other issues and challenges, and interaction with other Tasks/WPs.		

b- Competitive situation of concept 4 - Indoor Wireline Applications

The indoor wireline applications are niche markets, they can't compete with wireless in 95% of the use cases. Sometimes they may be needed to do through wall high data rate communications or to use existing power line networks.

c- Recommendations of concept 4 - Indoor Wireline Applications

Depending on the nature of these links, they will need low cost existing technology, with high voltage capability, or high end technologies with integrated photonics components.

V.3.2.5.4 . Concept 5: Device To Device Wireless Application

a- Table of concept 5 Device To Device Wireless Application

Concepts/Technologies	Medium term: 5+	Long term: 10+
Concept 5: DEVICE TO DEVICE WIRELESS APPLICATIONS		
a) Key research questions or issues		
- Die To Die & Package To Package	Data Rate > 10Gbs; BER 10-15	Data Rate > 100Gbs; BER 10-18

- NFC - RFID	RF (13MHz; 1Mbs); Hardware Security Embedded RF (13MHz; 100Kbs); RF (2.4GHz; 10Mbs); mmW (60GHz; 100Mbs) Hardware Security Embedded	Security / Privacy Embedded Security / Safety / Privacy Embedded
b) Potential for application or Application needs and Impact for Europe		
High data rate non-contact transfer Non-contact Safe Data transfer: Traceability and identification:	Multi-media transfer: Consumer market. Money transfer: Security of the operation. Goods and animals: safe and secure	Data-Base transfer: Consumer market. Personal and confidential data transfer: Safe and secure. People: Privacy.
c) Technology and design challenges		
Power Amplifier Technology challenges Fmax: Voltage breakdown: Re-Configurability: Power Switch Transistors Power Amplifier Design challenges mmW to THz Switch Band Modulator – De-Modulator Technology challenges Digital Approach: FT: Variability: Components density: Switches Transistors: Vdd: Ioff: Modulator – De-Modulator Design challenges Design by Mathematics and Digital approach for Analog functions Reconfigurability LNAs Technology Challenges: NFmin: Re-Configurability: LNAs Design Challenges: mmW to THz Switch Band Phase Frequency Generation Technology Challenges:	will be completed in the Second part of NEREID Project	will be completed in the Second part of NEREID Project

1/F noise: Cut Frequency Fmax: Tuning range: Re-Configurability: Switch transistors FT: Capacitor density: Linear Capacitor <u>Phase Frequency Generation Design Challenges:</u> ADPLL Reconfigurability <u>Antennas Technology Challenges:</u> Antenna on die with Semi-conductor substrate: Antenna in Package on Organic substrate: <u>Antennas Design Challenges</u>: Antenna with reflectors Switched Bands:		
d) Definition of FoMs (quantitative or qualitative) or planned evolution		
FOM=(Data_rate(Gbs)×$D^2(m)$×1/BER)/(Psupply(W)) Die To Die & Package To Package FOM: NFC FOM: RFID FOM:	**These FOMs will be estimated in the Second part of NEREID Project.**	
e) Other issues and challenges, and interaction with other Tasks/WPs.		

b- Competitive situation of concept 5 - Device To Device Wireless Application

RFID and NFC are the main drivers of such markets, the positive growth will continue and will be reinforced, with the demands for identification, food security, safe and secured bank data transfers, and so on. The first application, concerning in package communication, doesn't require any new product on the market, and could be a niche market within 5 years.

c- Recommendations of concept 5 - Device To Device Wireless Application

RFID and NFC applications need Energy efficiency and are oriented to Ultra-Low power requirements, they will integrate all the functions including security in a SOC approach. The last die to die and in package applications require in addition high bandwidth, and high frequency to mmW capabilities.

V.3.2.5.5. Concept 6: In Package/Device Photonics Wireline Applications

a- Table of concept 6 In Package/Device Photonics Wireline Applications

Concepts/Technologies	Medium term: 5+	Long term: 10+
Concept 6: IN PACKAGE/DEVICE PHOTONICS		

WIRELINE APPLICATIONS		
a) Key research questions or issues		
- Die 2 Die	Copper links (100 Gbs, 100s um); Photonics Silicon Interposer (1 Tbs, 10s mms); Active Interposers (100Gbs, mm) Flip chipped + Copper (100 Gbs , mm)	Photonic Silicon Interposer more than 2 Tbs over 10s mm Active Interposers (1Tbs, mm)
- Module 2 Module	Optical Waveguide (Tbs, 10s cm), Multifiber connectors, passive alignment	Toward 10 Tbs over cm
- Active cable	Optical guide/Fiber (toward 2Tbs, 10s m); Copper (100 Gbs, 10s cms); GI-POF (10Gbs, 10s cms); mmW Plastic Wave Guide (10s Gbs, 10s cm)	Toward 10 Tbs over 10s cms
b) Potential for application or Application needs and Impact for Europe	Big Data HPC	
HPC: 5G+ Data-center Intelligent transport; Entertainment; Factory 4.0…	Multicore Processor: European Independence. Big data Data transfer	Cognitive computing: European Independence. Big Data Data transfer
c) Technology and design challenges	…	…
Optical Modulator or laser driver technology challenges FT: Voltage breakdown: Linearity: Re-Configurability: Optical Modulator or laser Design challenges Multilevel Modulations. Pre-emphasis capability Power consumed reduction Modulations and Demodulation technology challenges: Re-Configurability : Multimode FT: Components density: Switch transistors: Vdd: Ioff: Modulations and Demodulation Design challenges: Multilevel Modulations.	 More than 0.5 THz More than 2V High Voltage linearity Ron-Coff < 100fs X X XX More than 0.5THz High (under 15nm gate) Ron-Coff < 50fs Less than 0.6V Low	 More than 1 THz More than 2V High voltage linearity Ron-Coff < 30fs XX XX XXX More than 1THz High (under 10nm gate) Ron-Coff < 10fs Less than 0.4V Very Low

Power consumed reduction Equalization, Post emphasis CDR low power Low jitter <u>Trans Impedance Amplifiers Technology challenges:</u> Current noise density: FT: Re-Configurability: Linearity: Wide band <u>Trans Impedance Amplifier Design Challenges</u>: Highly linear TIA High Dynamic range (Optical offset compensation) <u>Frequency Generation And Clock Recovery Technology challenges</u>: Fmax: Stability: Tuning range: Re-Configurability: Switch transistors FT: Voltage breakdown: Capacitor density: Linear Capacitor <u>Frequency Generation And Clock Recovery Design challenges</u> Digital approach Ultra-Low Jitter Stability Low Power High speed <u>Photodiode technology challenges:</u> Responsivity Input capacitor Black current 3D assembly <u>Laser Challenges</u>: Integration in Photonic Silicon <u>Optical Modulators technology challenges:</u> Extinction ratio Actuation <u>Optical Switches Challenge</u>:	X XX XX XX XX Low More than 0.5 THz Ron-Coff < 50fs High current linearity Wide XX XX More than 0.5 THz High 30% Min Ron-Coff < 50fs More than 0.5 THz More than 0.7V High density per µm² XX X X X 0.85 Few 10s fF Very low High efficiency III-V/Si 6dB Less than 2V range actuation Research	XX XXX XXX XXX XXX Very Low More than 1 THz Ron-Coff < 10fs Very high current linearity Very Wide XXX XXX More than 1 THz Very High 50% Min Ron-Coff < 10fs More than 1 THz More than 0.5V High density per µm² XXX XX XX XX 0.95 Few fF Extremely Low Very High efficiency Ge Laser and other Si compatible 12dB In 1V range actuation. Development
d) Definition of FoMs (quantitative or qualitative)		

or planned evolution		
FOM=(Data_rate(Gbs)×$D^2(m)$×1/BER)/(Psupply(W)) Die 2 Die FOM: Module 2 Module FOM: Device 2 Device FOM:	**These FOMs will be estimated in the Second part of NEREID Project**.	
e) Other issues and challenges, and interaction with other Tasks/WPs.		

b- Competitive situation of concept 6 - In Package/Device Photonics Wireline Applications

Photonics communications are the main promising technique to implement high speed networks in a package. The roadmap is clear and defined. We can't speak about High Performance Computing without such connectivity.

c- Recommendations of concept 6 - In Package/Device Photonics Wireline Applications

The photonics communications need high speed, medium power, high bandwidth, and Photonics components, this means that technologies which will serve such applications are high end technologies.

V.3.2.6 Main recommendations

Main recommendations for the Task

- Evaluation of the Connectivity FOM for each concept
- Reinforce the Indoor Short range Roadmap.
- Refine the technology request for each application.
- Define a complete Market analysis for each concept.

Main recommendations for technology research:

Antennas & Passives:
On demand Re-configurable and tunable Antennas and Passives, very compact and massive MIMO antennas, with beamforming systems and very high antennas' directivity for all the used band, 0-6GHz and mmW. Work may address metamaterials, NEMs, MEMs and integrated passives technologies, packaging and modules, design, systems and microsystems.

Transceivers & Front End Radio:
High Data Rate:
Up to 100GHz and up to THz Transceivers, stable and accurate local oscillators, and antennas' interfaces targeting high and agile spectrum usage, with wider communication bands, allowing Full-duplex communications and solving Interference management, with on demand new PHY waveforms generation. Work may address New generation of nm CMOS, beyond CMOS, and mixed Silicon-III-V technologies, NEMs, MEMs, and new physics devices, combined with new design methodologies, modelisation and wireless long range, short range or wave guided systems.

Low Power Radio:
Ultra-low power transceivers for WSN and IoT Networks, with µW consumed power objectives. Work may address Wake-Up Radio, Ultra-stable ultra-low power time reference, charge transfer, or time-frequency

modelisation and design methodologies, CMOS, Beyond CMOS, NEMs MEMs, and new physics devices, wireless, including ultrasonic, or silk guided systems.

Wireline:

Low cost 1300nm and 1500nm laser sources, optic modulators, LEDs, and PIN diodes, with their electrical interfaces, drivers and Trans impedance receivers, for modulations giving 400Gbs to Tbs. Work may address photonics integrated components, including laser and VCSELs, copper wireline interfaces, 3D packaging methodology, Multiphysics modelisation and simulations, CMOS beyond CMOS, and low cost exotic More than Moore processes.

V. 4 Functional Diversification (WP4)

V. 4.1 Smart Sensors (T4.1)

V. 4.1.1 Executive summary

Global challenges for today's technology concern more sustainable, ICT-enabled strategies for *healthcare, energy and environment.* The role of edge-of-the cloud devices and of the generated big data are expected to drive the creation of new ecosystems and include 11% of the world economy by 2030.

The technology-Market developments[14] moved from a Processing Information "Moore" age (from the 80's to 2010) to a present Sensing Interaction in the "More than Moore" age (from 2010 to 2030, exploiting mobile computing and communication technologies) and, the expectations for the future are about an Actuating Transformation "Beyond Moore" age (beyond 2030, with smart cities, smart home and autonomous vehicles and Industry 4.0 driving the application scenarios). This means that the technology is moving from simple sensing to *smart sensing* in almost every object, enabling new classes of services and applications.

The exercise of performing a European smart sensor roadmap is broad, complex and diversified because sensing technologies are very diverse and not driven just by scaling and costs, such was the case of CMOS. The exponential growth of the importance of smart sensors was first pointed out in Europe and worldwide by the FET Flagship initiative Guardian Angels for a Smarter Life in 2011, a project that proposed roadmaps for energy efficient smart sensors in a perspective of 10 years. Only later some industries came with roadmaps for the so called 'Trillion of sensors planet'. This means that Europe played a pioneering role in understanding and predicting the importance of smart sensors to support edge of the cloud applications in the future economy.

Among many domains for smart sensor applications, NEREID has chosen to focus on two main fields: (i) *healthcare* and (ii) *automotive*, as application drivers. These two fields have a high relevance for European industry and research.

In the healthcare sector European countries are coming second after US, while in automotive, Europe dominates the autonomous vehicle market. Moreover, the European leadership in automotive is expected to be reinforced in the coming 5-10 years thanks to the presence of major technology manufacturers, early commercialization of automated vehicles and public organizations supporting the advancement of these vehicles[15]. In addition, most of the sensors types and challenges outside these fields are similar and relevant for industrial segments such as consumer electronics (MEMS accelerometers, magnetic, chemical and gyroscopes), industrial (image sensors), infrastructures (air quality gas sensors) and defense (LiDAR sensors).

[14] Sensors for Wearable Electronics & Mobile Healthcare 2015 Report by Yole Development.

[15] ADAS (Advanced Driver Assistance System) by systems and sensors, Global Opportunity Analysis and Industry Forecast, 2013 – 2020, May 2015, (www.alliedmarketresearch.com).

Overall, connected objects (as part of Internet of Things, IoT), big data, software and algorithms, zero-power or self-powered sensors, sensor fusion, wireless sensor networks and system-in-package are all important topics for a more complete sensor roadmap.

V.4.1.2 Relevance and competitive value

The European automotive industry includes many world leaders and Europe is expected to lead the future autonomous cars market with the Advanced Driver Assistance Systems (ADAS) which predicts a worldwide market of 60 B$ by 20203. On the other hand, European medical industry has a competitive position within the global market. European medical diagnostics and wearable market is the second highest revenue generator, owing to well-penetrated healthcare system and favorable regulatory policies2.

Automotive sensors are involved in major automotive scenarios involving less energy consumption (fuel-efficient and hybrid electric vehicles), *less pollution* (reduction for carbon footprint with stringent government laws and regulations towards vehicular emission) and *improved safety and security* of passengers (with autonomous cars and regulations to avoid road accidents). Progress in these domains is expected to boost the market growth and open new opportunities in the field of automotive sensors.

Improvements in healthcare sensor technology and required infrastructure will accelerate the extension and increase of its scientific excellence and competitiveness, which enable a cost effective fully sustainable health-care system with truly personalized medicine, prevention and wellness for European citizens. This certainly will drive an economic benefit of healthcare costs.

This favorable position for European high added value medical and automotive smart sensors and systems (proposed by ECSEL[16]) needs to be maintained and supported by massive investments of resources against the very competitive Asia-Pacific markets and other emerging countries. At the same time, these investments could activate a strong emergence of startups, the creation of bridges that improve the synergies between the excellences of European technology offer (that it is often sold abroad) and the European Industry (that buys their components from abroad) by forming a new sustainable ecosystem of European industries with high innovation content.

Societal benefits

Energy and environment, as mentioned above, are two present global challenges. *The road transport research in Europe (ERTRAC) supported by EU policies have set out key ambitions[17]: (1) The European road transport sector should be 50% more efficient by 2030, (2) CO_2 emissions will reduce significantly (80% cars, 40% trucks) and new fuels will enter the market, and (3) transport schedules (mobility) will be 50% more reliable and traffic safety will improve significantly (reducing road accidents around 60% by 2030).* Fuel-efficient hybrid electric vehicles are one of the paths to reduce the carbon footprint and the energy needs of society (if the energy is generated by renewable sources). Autonomous cars appear to improve x10 the safety of passengers and pedestrians while reducing fuel consumption by 10% and cost insurance by 30%[3].

In addition, there is an increase in the incidence of chronic diseases (cancer, cardiovascular diseases, diabetes) or of those coming from viral and bacterial infections (gastrointestinal, respiratory, sexually transmitted diseases, STDs or tuberculosis TBC). In 2011, approximately 5 million deaths occurred due to these diseases (AIDS, malaria & TBC). Awareness of health detrimental factors like obesity is rising as well as the population ageing (by 2025 more than 20% of Europeans will be 65 or older[1]). According to WHO (World Health Organization), cancer caused 8.8 million deaths in 2015, and is expected to reach 11 million by 2030[18]. The increase in these diseases will raise the demand for diagnostic devices (activity trackers,

[16] Smart Health, Smart Production, Smart Society (www.ecselju.eu/web/index.php).
[17] European Roadmap Safe Road Transport, ERTRAC, June 2011 (www.ertrac.org).
[18] Fact sheets and World Cancer Report 2014 (www.who.int).

body monitors and multi-parameter real-time sensing) and for most of them, a low-cost, portable and fast diagnostic solution does not exist in the market yet. They could also serve to detect the incidence of health hazards caused by pollution. These emerging medical devices will allow improving healthcare facilities (patient monitoring techniques from a distant location), treating these diseases in the emerging nations and simplifying the acceptance of personalized more-efficient medicine.

V. 4.1.3 Vision

The Bosch scientist's vision for Automotive 2030+ foresee that the needs for cars in urban areas will also change. The cars makers have to re-think their business model and it will go mostly in the direction of "mobility-as-a-service" where the providers will offer electrical vehicles, car sharing, etc. All this is oriented to the "Last-Mile" micro-mobility as an attractive niche market where the car is intended to be used only for the last mile after public transportation (train, plane, etc.) because the classical motorized individual traffic will reach its peak. Future automotive sensors will serve as important drivers for the reduction of fuel consumption and car emissions, and to improve safety and security of the driver and other vulnerable road users. These governments and users awareness in addition to the coming regulations will massively transform the automotive industry with a rapid market penetration of smart sensors and a mass adoption of Advanced Driver Assistance Systems (ADAS) amongst customers. Autonomous cars and drowsiness detection are two of the ultimate applications. It is predicted that the number of sensors per car will increase from 10 to 300 in the next 10 years.

The future of medical sensors is related to edge of the cloud applications serving personalized and preventive healthcare approaches combined with healthy lifestyle electronic managers. New generations of non-invasive biological monitoring with embedded powering and sensing, multi-parameter sensing platforms, sensor fusion, wireless sensors networks (WSN), zero-power technological platforms or self-powered sensors, big data, energy-efficient data processing in cloud computing, etc. will predictably edge to the billion or trillion planet sensors of connected devices.

V. 4.1.4 Scope and ambition

These roadmap sections will cover medical and automotive applications and some specific selected sensors/categories as follows:

Automotive:

- Sensor's for car internal system performance: Motion, Pressure and Position sensor
- Advance Driver Assistance System (ADAS): Image, LiDAR and Infrared sensors
- Environmental monitoring: Gas and Particulate Matter sensors

Medical:

- Physiological signal monitoring
- Implantable sensors
- Molecular diagnostics

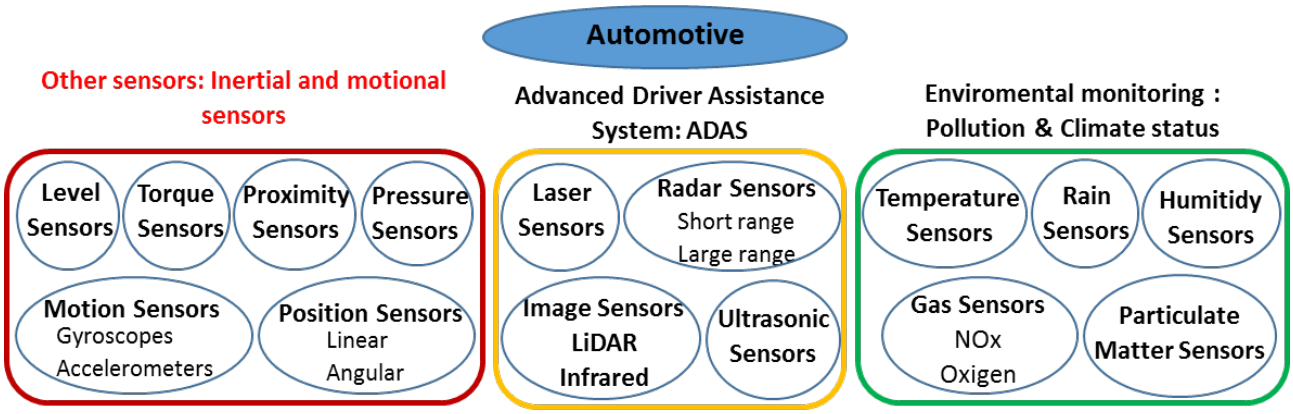
Other sensor applications from other sectors are not specifically covered here. However, most of the sensors types and challenges covered in this document are similar and relevant for other industrial segments such as consumer electronics (MEMS accelerometers, magnetic, chemical and gyroscopes), industrial (image sensors), infrastructures (air quality gas sensors) and defense (LiDAR sensors).

V. 4.1.5 Main Concepts

A **smart sensor** is an electronic component that enables better control and monitoring of different operations, such as sensing physical inputs and produces a response by generating an output on a display or transmitting information in an electronic form for further processing using signal conditioning, embedded algorithms, and digital interfaces.

Sensors for Automotive applications

Automotive sensors are being widely used in four key applications; chassis, powertrains, body electronics and safety & security. Powertrain is the most popular application as sensors play an imperative role in improving fuel efficiency and reducing emissions. Most of the sensors used in automotive are categorized below:



Common requirements for the sensor technologies in the automotive industry are:

- All the features (i.e., high resolution and contrast for a camera) guided by safety rules
- Capability to filter, process and evaluate big data, data safety and privacy
- Transferability to all vehicle types
- Robustness in all weather conditions
- Stability in large temperature ranges
- Redundancy for failsafe operation
- Long life-time, low power and low cost
- Capacity for data storage and a sufficient computing power
- Miniaturization
- High quality standards and performance optimization (resolution, form factor, etc.)

Sensors for navigation and car's basic system performance

MEMS devices are extensively used in cars for air bag sensors, electronic stability control, tire pressure monitoring, fuel injector pressure sensors, roll over detection sensors, vehicle dynamic control VDC sensors, throttle position sensors and other safety features.

Motion sensors serve to detect or track movements (in linear or rotational direction, namely accelerometer and gyroscope respectively) by monitoring a change in velocity or orientation of an object. There is an increased demand of accelerometers, gyroscopes and magnetometers. MEMS-based sensors have smallest form factor, which is a major reason for their faster adoption.

Optical position sensor detects the position of the targeted object. It detects changes in vehicle positions and provides parking assistance. In addition, these sensors ensure driver safety, thus releasing airbag depending on the position of the driver. A growth in adoption of these sensors is expected due to the increase demand of automobile safety and the rise of wearable medical devices adoption. Owing to their compact size, reliability, and low power consumption, high-performance and cost-efficiency of these sensors are widely adopted and rising its use in consumer electronics.

Proximity sensors are integrated in systems to detect the presence of an object of interest within the vicinity of the sensor. The function is featured with non-contact detection ensuring a high degree of reliability and durability of sensor.

Displacement sensors measure the displacement of object of interest from one point to another. There is a growing popularity towards contact less sensing applications and the interest of automobile manufacturers towards the integration of sensor technology in automotive security and infotainment systems, as for parking sensor system. Other non-automotive applications are ground proximity warning system, anti-aircraft warfare, roller coasters, conveyor systems, vibration monitoring systems, assembly line testing, mobile devices, etc.

V.4.1.5.1 Concept 1: Motion Sensors

a- Table of concept 1 Motion Sensors

	Medium term: 5+	Long term: 10+
Concept 1: Motion Sensors		
a) Key research questions or issues		
Accelerometers	XXX	XXX
Gyroscopes	XXX	XXX
b) Potential for application or Application needs and Impact for Europe	…	…
Roll over detection for airbag	XXX	XXX
Dead reckoning	XX	XXX
Anti-theft	X	XX
Pre-sage system	XX	XX
Black box	X	XXX
Infotainment	XX	XX
c) Technology and design challenges	…	…
MEMS	XXX	XXX
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Acceleration	+/- 2 g range	
Form factor/miniaturization	Important for bionics	
Power consumption	< 1 µW	
Price	< 1 $	
Output data range	1 kHz	
Resolution	>8 bit	>10 bit
Non linearity	XXX	XXX
Bias stability	XX	XX
Full range	X	X
Lifetime	5 years	10 years
Packaging	XXX	XXX

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period.

b- Competitive situation for Concept 1 Motion Sensors

MEMS devices primarily drive the automotive sensor market. Accelerometer and Gyroscope market is projected to reach $5 billion by 2022[19]. Parking sensor systems based on proximity and displacement sensors hold at present the maximum revenue share. Motion sensors are used in fully autonomous vehicles, in air bags, for voice-controlled equipment or across medical and healthcare sector (e.g. designing implantable medical devices) are expected to witness future growth opportunities in the European sensor market. On the other hand, accelerometer and gyroscope have become an integral part of all consumer electronic devices, although the MEMS market in mobile/portable applications grows more slowly than in previous years[19].

c- Recommendations for Concept 1 Motion Sensors

Low accuracy of motion sensors restrains the market growth. Increase in automation for vehicles and low power consumption & small size are anticipated to provide numerous opportunities in the future. In addition, MEMS average selling price for consumer applications has fallen below $1, meaning that the use of sensors such as MEMS microphones, inertial, pressure and gas sensors in mobile phones has very low margins today. More lucrative industries or larger volumes are needed to boost MEMS market (automobile, defense & aeronautics, medical and industrial). The internet of Things (IoT) is still a niche market and wearable electronics applications look very promising although volumes are not very high yet. Medical and automotive applications still offer pockets of growth and profitability as well as new opportunities. At present, the car industry uses on average 20 MEMS per car and autonomous cars will offer more possibilities for MEMS technologies.

V.4.1.5.2 Concept 2: Pressure Sensors

Pressure sensor detects, measures, and transmits the information, which helps in analyzing the performance of a device. It monitors and controls the pressure of gases and liquids; and measures different types of pressures such as absolute, vacuum, gauge, and differential pressure

Pressure sensors are the key components in reducing emissions and fuel consumption in emission control sensors, so as to decrease the air pollution. In addition, they are deployed for various safety concerns of passengers, such as Tire Pressure Monitoring Systems (TPMS), Advanced Driver Assistance Systems (ADAS), and Manifold Absolute Pressure Sensors (MAP). It also helps in deployment of air bags, throttle position, weight, sensing of passengers and Engine Gas Recirculation (EGR).

a- Table of concept 2 Pressure Sensors

	Medium term: 5+	Long term: 10+
Concept 2 : Pressure Sensors		
a) Key research questions or issues		
Pressure sensors for automotive	XX	XXX
Pressure sensors for medical applications	XXX	XXX
b) Potential for application or Application needs and Impact for Europe	…	…
Automotive		
Tire Pressure Monitoring System	XXX	XXX
Air Bag deployment	XX	XXX
Electronic Engine Control	XX	XX
Side Crash detection	R&D and DP	Market Introduction

[19] Accelerometer & Gyroscope Market (…) and Industry Vertical (Consumer Electronics, Automotive, Aerospace & Defense, Industrial, and Healthcare) - Global Opportunity Analysis and Industry Forecast, 2014 – 2022, February 2017, (www.alliedmarketresearch.com).

Pedestrian impact detection	DP and RS	Market Introduction
Seat Comfort System	R&D	Market Introduction
Idle stop	XX	XX
Fuel Vapor	XX	XX
Barometric Air Pressure (BAP)	XXX	XX
Medical		
Blood pressure measurement	XXX	XX
Bladder examination	XXX	XXX
Tactile sensors for fall detection	XX	XXX
Mass balance (to detect nanoparticles/atoms)	X	XX
c) Technology and design challenges	…	…
Piezoresistive		…
Capacitive (MEMS)		
Optical		
Electromagnetic		
Resonant Solid state		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Barometric Pressure Sensor – Wearable devices	….	…
Pressure level precision	0.005 hPa	0.001 hPa
Pressure relative accuracy	0.06 hPa	0.001 hPa
Temperature accuracy	0.5 °C	0.1 °C
Pressure temperature accuracy	0.5 Pa/K	0.1 Pa/K
Measurement time	3 ms	< ms
Power consumption (average/Standby current)	1 μA	< 100 nA
Supply voltage	1.2 – 3.6 V	< 1 V
Package dimension	2 x 2.5 x 1 mm	XXX
Output power	8 dBm	
RF Transmitter/LC receiver	400 MHz/ 300 KHz	
Robustness (-20, 200°C), Lifetime, Stability	XXX	XXX
Robustness (-20, 200°C), Lifetime, Stability	XXX	XXX

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period, R&D: research and development, DP: Demonstration and Prototype, RS: Regulations and Standards.

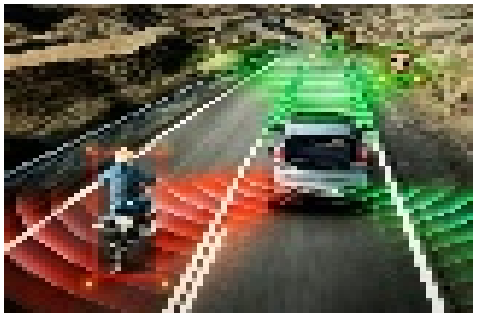
b- Competitive situation for Concept 2 Pressure Sensors

The global pressure sensors application market is dominated by the automotive applications segment and, with the medical sector, hold more than half of the total share. In addition, autonomous cars and the increase in demand of pressure sensors in medical applications will benefit automotive and medical manufactures to boost their market growth and increase their market share in the short-middle term (3-5 years).

c- Recommendations for Concept 2 Pressure Sensors

Industrial and defence markets provide growing opportunities for high-end and high-margin devices such as inertial and pressure sensors. For consumer industry with smart phones and wearables has in turn pushed for smaller dies for integration in thinner handsets, reducing prices and shrinking margins. A shared manufacture infrastructure cost with other applications (e.g. between automotive and consumer), improved processes that further lower cost (like CMOS MEMS) or the creation of new devices with added value (e.g. software embedded within the sensor to deliver higher level functions) are some ways to limit the MEMS market regression.

V.4.1.5.3 Concept 3: Advanced drive assistance systems (ADAS): *sensors for autonomous cars*



Autonomous cars (driverless or self-driving car) are automated cars, which feature all the major competencies of traditional cars. There is a major interest from technology providers to develop safer and more efficient transportation systems due to the increase of road accidents. Thus, a majority of the manufacturers have indicated a keen interest in developing, manufacturing and commercializing driverless cars in the coming years. In a first phase towards fully autonomous vehicles, ADAS facilitates safe driving and warns the driver if the system detects risks from the surrounding objects. Deployment of ADAS in vehicles serves to enhance comfort along with a rise in government regulations for ensuring safety on road. Main sensor types in ADAS systems are image devices (cameras, infrared and LiDAR sensors), radar sensors (short and large range), laser and ultrasonic sensors. Main ADAS systems based on those sensors are displayed below (apart from other dynamic systems as Tire pressure monitoring, adaptive front lighting or drowsiness monitor).

The different ADAS functions are split in mandatory for safe driving reasons, standards for effortless driving and differentiation for a *new driving experience*. However, such functions will be constantly upgrading and what today is installed in a premium class car, in the future it will be in the comfort class.

Vehicle cameras or image devices are mounted in and around a vehicle to provide real-time imaging and video recording of the inside and outside surroundings of the vehicle. These image devices offer various advantages such as 180-degree view of path for drivers, night vision, evidence in case of accident, and others. Advancement and fusion of technologies and equipment are likely to transform and increase the camera efficiency. It is categorized by 3D cameras (for gesture recognition, presence detection and driver monitoring), vision cameras (blind-spot side view, rear parking assistance, accident recorder, stereo cameras with direction and distance for LDWS and traffic sign recognition), LiDAR (light detection and ranging) sensors (for 3D mapping of surroundings) and night vision cameras (for pedestrian and animal detection).

Image sensors detect images and convey information to a central monitoring system. Their use in autonomous cars is expected to increase exponentially. Image sensors are classified into charge-coupled device (CCD) and complementary metal - oxide semiconductor (CMOS). Other applications are in medical imaging for 3D scanning, 3D rendering, image reconstruction or 3D modeling gesture recognition apart from traditional digital camera and camera modules consumer markets.

Light Detection and Ranging (LiDAR) is a dynamically emerging technology which is used over conventional surveying methods to make the examination, detection and 3D mapping of geospatial surfaces easier and to provide highly accurate data (improved resolution and data processing) in a shorter time than conventional methods. A LiDAR forms the image of the environment by shining a laser on it and capturing the reflected light to compute distances. Novel LiDAR technology is micro-size, all silicon and low-cost, which allows its use for all kind of new applications as for autonomous driving. However, LiDAR systems are still more expensive than other technologies as radars due to the large number of components required: laser scanners, position and navigation system, high-resolution 3D cameras, photodetectors and MEMS.

Infrared detectors are used to detect infrared radiation, to measure heat and detect motion. Infrared detectors convert infrared radiation into electrical signals and are used in defense systems, medical and automotive applications among others (as non-contact temperature sensing, infrared gas analysis, flame detection, temperature control systems, detection of human presence, and infrared spectroscopy).

Recent developments have manufactured highly sensitive infrared detectors at affordable prices. They are compact in size and have the ability to detect infrared light from long distances. However, they detect infrared images based on the temperature variations of objects (no discrimination of objects with a very similar temperature range). Their main present challenges are the higher cost (due to the required additional semiconductor components for increased sensitivity, the cooling techniques and the installation) and the inaccuracy in certain conditions (clean environment without dust and low humidity are required)

a- Table of concept 3 Images Devices for autonomous cars

	Medium term: 5+	Long term: 10+
Concept 3 Imaging Devices for autonomous cars		
a) Key research questions or issues		
Image Sensors	XXX	XXX
LiDAR	XX	XXX
Infrared Sensors	XX	XX
b) Potential for application or Application needs and Impact for Europe	…	…
Image Sensors		
Adaptive Cruise Control (ACC)	Standard function	Mandatory function
Lane departure Warning System (LDWS)	Standard function	Mandatory function
Park Assistance (PA)	Standard function	Mandatory function
Collision warning	Market Introduction	Premium class
Dynamic lighting	R&D and RS	Market introduction
Pedestrian detection	DP and RS	Market introduction
Traffic signal recognition	R&D and RS	DP
LiDAR		
Automatic emergency braking (AEB)	RS and DP	Market Introduction
3D Mapping of surrounding	Market introduction	Premium class
Infrared Sensors		
Night vision camera	Premium class	Standard function
Pedestrian/Animal detection	DP and RS	Market introduction
c) Technology and design challenges	…	…
Image Sensors	…	…
Charge-coupled device (CCD)	XXX	XXX
Complementary metal - oxide semiconductor (CMOS)	XXX	XXX
Single-phonon avalanche diode (SPAD)	XX	XXX
3D hybrid stack backside illumination (BSI)	X	XX
LiDAR Component		
Laser scanner	XX	XXX
Position and navigation systems (GPS/GNSS)	XX	XX
3D cameras (as before)	XXX	XXX
Photodetectors (solid-state as Si avalanche photodiode)	XX	XXX
MEMS	XXX	XXX
Infrared Sensors		
Pyroelectric	XX	XX
Thermopiles	XX	XX
Thermodiodes	XX	XX
Microbolometers	XXX	XXX
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Common ADAS FoMs		
Feet-off	XX	XXX

Hands-off	X	XX
Eyes-off	O	XX
Mind-off	O	O
Multifunction camera	XX	XXX
Sensor fusion	XX	XXX
(3D) Image Sensors		
Sensitivity	XX	XXX (important for medical imaging)
Price	3$	1$
N° of sensors/car	5	10
Autofocus (AF)	XX	XXX
Optical Image Stabilization (OIS)	XX	XXX
Dual camera technology	XX	XXX
Time of flight (ToF)	XX	XXX
Structure light (SL)	XX	XX
3D Sensing cameras/4D	X	XX
Saturation Signal	X	XX
Dark signal	X	XX
Resolution (pixel, p)	XX	XXX
Pixel size/Number	X	X
Read noise	XX	XX
Detection Range (m)	1-50 m	1-70 m
Field of view	60 °	180 °
Chip/Image size	XX	XX
LiDAR		
Resolution	XX	XXX
Price	< 250 $	< 100 $
N° of sensors/car	1	2
Power consumption		
Detection Range	1-100 m	1-250 m
Accuracy	< 2 cm	< 0.1 cm
Scanning angle	270 °	360°
Angular accuracy	5-10 °	2-5°
Scanning time	Few seconds	Ms
Time of flight (ToF)	XX	XXX
Infrared Sensors – Night vision camera		
Camera resolution	XX	XXX
Price	< 1000 $	< 500 $
N° of sensors/car	1	3
Power consumption		
Detection Range (NIR/LWIR)	150/ 400 m	200/ 500 m
NETD (f/1; 300k; 50 Hz)		
Frame rate	XXX	XXX
Size/weight	XX	XXX
Common features		
Failsafe	XXX	XXX
Robustness (operating temperature -20°C – 60°C)	XXX	XXX
Reliability - Lifetime	10 years	15 years

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period, R&D: research and development, DP: Demonstration and Prototype, RS: Regulations and Standards.

b- Competitive situation on concept 3 Images Devices for autonomous cars

In addition to the exponential increase in the use of image devices predicted for autonomous cars applications, there is a continuous market in mobile applications and an increased demand for better and sophisticated healthcare facilities, advanced resolution and visualization of accurate test diagnosis. Thus, 3D healthcare industry is anticipated to witness high adoption of 3D imaging and dominate the global market share by 2022. The CMOS image sensor (CIS) market with new functions and industries (medical, security, industrial, etc.) could reach $18.8B by 2021. European key players include Infineon Technologies, STMicroelectronics and Siemens Healthcare among others.

c- Recommendations on concept 3 Images Devices for autonomous cars

Competition in image sensors will remain relatively open and can become a market opportunity for Europe as long as the growth pattern is maintained and key technology changes occur almost every other year. The ADAS trend is further increasing pressure on vendors to provide sensors beyond their current technical capabilities. Image analysis is the new frontier and early usage of artificial intelligence for many different industries. Finally, technologies as time of flight (ToF) is bringing device miniaturization and structured light (SL) is resulting in high-resolution mapping at reasonable cost. For the case of infrared imagers, the high cost of the technology has restrained the use of microbolometer to niche/medium volume applications but this is changing which will allow the way to consumer applications.

V.4.1.5.4 Concept 4: Radar Sensors

Radar sensors provide long- and mid-range functionality, which allow automotive systems to monitor the environment around the vehicle to help prevent collisions. A radar is an object-detection system where the radio waves are used to determine the range, angle or velocity of objects. They are less affected by adverse weather conditions and pollution (as compared to infrared detectors) and can provide 360° sensing.

a- Table of concept 4 for Radar Sensors

	Medium term: 5+	Long term: 10+
Concept 4: Radar Sensors (Long range/ medium-short range)		
a) Key research questions or issues		
Long Range Radar (LRR)	XXX	XXX
Medium/Short Range Radar	XX	XX
b) Potential for application or Application needs and Impact for Europe	…	…
Long Range Radar		
Adaptive Cruise Control (ACC)	Standard function	Mandatory function
Emergency Brake Assistance (EBA)	RS and DP	Market Introduction
Collision avoidance or Mitigation (CM)	Market Introduction	Premium class
Pedestrian Detection	DP and RS	Market introduction
Short/Medium Range Radar		
Rear Collision warning	Market Introduction	Premium class
Blind Spot Detection (BSD)	RS and DP	In Market
Cross Traffic Alert	R&D and RS	DP
Lane change assist (LCA)	R&D and RS	DP
c) Technology and design challenges	…	…
Silicon	XXX	XXX
Silicon Germanium	XX	XXX
d) Definition of FoMs (quantitative or qualitative) or planned evolution	…	…

(based on SoA @ 2017 and evolution vs time)		
Long range Radar		
Distance of object recognition	250 m	
Price	100 $	50 $
N° of sensors/car	1	2
Frequencies	79-81 GHz	
Short range Radar		
Distance of object recognition	0.2-30 m	
Price	30 $	10 $
N° of sensors/car	4	6
Frequencies	24-77 GHz	
Common Radar sensors features		
Failsafe	XXX	XXX
Efficiency	XX	XX
Noise level	X	X
Robustness (-40 °C to 125 °C)	XXX	XXX
Reliability - Lifetime	10 years	15 years
Packaging	X	X

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period, R&D: research and development, DP: Demonstration and Prototype, RS: Regulations and Standards.

b- Competitive situation

There are regular upgrades in the ADAS technology, which facilitate competitiveness in the market. In addition, the increasing awareness on safety and safety regulation in parallel with an increasing demand for driving comfort and multifunctional systems helps to keep the market growing. In the following figures, the sensor modules and functions for autonomous cars and market share are depicted (Yole development reports2).

Key players in Europe include automotive suppliers as Robert Bosch GmbH, NXP or Infineon and manufacturers as Peugeot-Citroen SA, Jaguar Cars limited and Fiat-FCA among others.

c- Recommendations

The general challenges from the automotive markets cover the technology and packaging, a full eco-system ("from transistor to housing") which includes multi-domain co-design (chip, package, system) and reliability (see WP5 Roadmap too). In addition, the necessary building blocks for monitoring an autonomous car includes not only sensors but also software, Electronic Control Unit (ECU), data management, GPS and connectivity which require interaction among WPs.

Pollution/Air quality monitoring based on gas sensors

V.4.1.5.5. Pollution/Air quality monitoring based on gas sensors

Pollutants released from vehicles (automobiles and powered vehicles, industries, power plants diesel generators, etc.) into the environment can be controlled by setting up emission standards, which dictate the limits of pollutants such as CO_2, NO_x and SO_x. Low emission vehicles are fully electrical or hybrid, which involves a combination of traditional engines (Internal Combustion Engines), and electric vehicles in order to reduce both pollution (low emission batteries) and the dependence on oil.

In addition, **Gas sensors** and **Particulate Matter detection** are very demanding for other applications especially to measure the Indoor/outdoor Air Quality and see the influence on our health (in combination with physiological signals monitoring). A common air quality index exists in Europe CAQI[20] based in three major pollutants: particulate matter (PM10), nitrogen dioxide (NO_2) and ground-level ozone (O_3). When data also available three additional pollutants are also taken into account: particulate matter PM2.5, carbon monoxide (CO) and sulfur dioxide (SO_2).

The Figures of Merit (FoM) from the following table has been considered for the most demanding applications, such as portable gas sensors where the size, form factor and power consumption are crucial FoMs which would not be the case for the gas sensors on cars.

a- Table of concept 5 for Pollution/Air quality monitoring

		Medium term: 5+	Long term: 10+
Concept 5: Environmental monitoring			
a) Key research questions or issues			
Gas Sensors		XXX	XXX
Particulate Matter Detection		XX	XXX
b) Potential for application or Application needs and Impact for Europe			
Gas Sensors			
CO, SO_2, NO_2, O_3 (IAQ: indoor/outdoor, vehicle emissions)		R&D, RS and DP	Market introduction
Automotive fuel cell			
Blood alcohol content (BAC)		Market Introduction	
Medical diagnostic (Asthma or odor detection)			
Toxic, explosive, fire or injurious gases (industrial, infrastructure)		R&D, RS and DP	Market introduction
Particulate Matter Detection			
PM2.5		R&D, RS and DP	Market Introduction
PM 10		R&D, RS and DP	Market Introduction
c) Technology and design challenges (TRL)			
Metal oxide semiconductor (MOS)			
Pros	*Cons*	*Target gases and/or application field*	
▪ Low cost ▪ High sensitivity (but poor at room T°) ▪ Wide range of gases	▪ High T° operation ▪ Long recovery time ▪ Structural instability ▪ High power consumption	Industrial application and civil use	
Nanometal oxides – Resistive MOX-CMOS			
Pros	*Cons*	*Target gases and/or application field*	
▪ Longest lifetime 5-10 years ▪ Fast Stabilization time	▪ Large size ▪ High cost ▪ High power consumption ▪ Need of calibration		
MEMS Micro-hotplates MOS		First products in Market	High volume market?
Pros	*Cons*	*Target gases and/or application field*	
▪ Small footprint ▪ Low cost ▪ Ultra-low power consumption	▪ Limited by sensitivity	Mobile market	
Electrochemical Sensors		In Market	In Market
▪ Large size (2 cm), limited lifetime (< 2 years), mature			

[20] http://www.airqualitynow.eu

Solid-state CMOS imagers		DP	Market Intro?
▪ High power consumption~50 mWatt, poor sensitivity			
Polymer sensing layers (possible with MEMS resonating layers)		R&D	R&D
Pros	*Cons*	*Target gases and/or application field*	
▪ High sensitivity at room T° ▪ Short response times ▪ Low energy consumption ▪ Low cost	▪ Long-time instability ▪ Irreversibility ▪ Poor selectivity	Portable applications Indoor air monitoring Workplace like chemical industries	
Carbon-based (SW-CNTs)		R&D and DP	Market Intro ?
Pros	*Cons*	*Target gases and/or application field*	
▪ Ultra-sensitive ▪ Great adsorptive capacity ▪ Short response times ▪ Low cost, weight and simple ▪ Large surface/volume ration ▪ Good corrosion resistance	▪ Lack of CNT growth control ▪ Variability ▪ Hysteresis ▪ Low TRL	Detection of partial discharge (PD)	
Moisture Absorbing Material			
▪ Low cost and suitable for mass production (+)		Humidity monitoring	
Spectroscopy		Few in market	
Pros	*Cons*	*Target gases and/or application field*	
▪ High sensitivity, selectivity and stability ▪ Long lifetime ▪ Short response time	▪ High cost	Enable on-line real time detection	
Optical IR sensors (non-dispersive IR: pulsed emitter and detectors)		In Market	In Market
Pros	*Cons*	*Target gases and/or application field*	
▪ Highest accuracy ▪ High sensitivity, selectivity and stability ▪ Longest lifetime ▪ Enable miniaturization (MEMS)	▪ Large size (not for mobiles) ▪ High power consumption (~150 mWatt) ▪ High cost ▪ Inaccuracy in certain conditions	Remote air quality monitoring Gas leak detection systems with high accuracy and safety High-end market applications	
Chromatography			
▪ High sensitivity but high cost and size		Typical laboratory analysis	
Quantum dots, nanotubes and nanowires		R&D	R&D
▪ Low TRL, Integration challenges			
c) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)			
Gas sensors Technical Requirements		….	…
Sensitivity (high ppb, medium/low ppm)		**< 100 ppm**	< 10 ppm
Response Time		<0.1 s	ms
Sensor element power consumption		< 200 nW	<50 nW
Energy consumption (including the read-out circuitry)		< 100 μW	< 10 μWatt
Adsorptive capacity			
Sample rate (fs= 2x B bandwidth)		**>0.1 KS/s**	>1 KS/s
Input full scale (FS)			
Normalized output signal (NS)			1%
Resolution (Effective number of bits ENOB, N)		**8**	10
Energy entire sensor readout		**<100 fJ**	<10 fJ
Particulate PM 2.5 Technical requirements			
Sensitivity (high ppb, medium/low ppm)		50 μg/m³	1 μg/m³
Response Time		5 min	1 min
Sensor element power consumption		< 100 μWatt	< 10 μW
Sample rate (fs= 2x B bandwidth)		**>0.1 KS/s**	>1 KS/s
Input full scale (FS)			

Normalized output signal		1%
Resolution (Effective number of bits ENOB, N)	1	2
Other requirements		
Selectivity	XX	XX
Reversibility		
Stability (accuracy)	XXX	XXX
Auto calibration	XX	XXX
Reliability - Lifetime	5 years	10 years
Package Size (for mobile application)	< 3 cm^2	< 1 cm^2
Form factor	XXX	XXX
Integration (hybrid, 3D, on flex)	XX	XXX
Wireless/Wired connectivity	X	XXX
Robustness (harsh environment)	XX	XX
Business Requirements		
Price	2 $	< 1$
Volume (low, medium, high)	High	high
Market (emerging, niche, growing, mature)	Emerging	Growing

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period, R&D: research and development, DP: Demonstration and Prototype, RS: Regulations and Standards.

b- Competitive situation

The growing awareness of air pollution will be driving the demand for gas sensors. The environmental gas sensor market is expected to grow over $3 billion by 20272121 including indoor, portable and fixed outdoor air quality as shown in the figure below. The gas sensor market is dominated by US, Europe occupies a second position and the Asia-Pacific region is expected to grow at the highest CAGR margin (the bubbles sizes in the figure below represent the market size of the individual countries).

c- Recommendations

- Emission standards that dictate the limits of pollutants such as CO2, NOX and SOX, released from vehicles and industries into the environment, need to be established.
- Low emission vehicles such as hybrids, which involve a combination of traditional engines and electric propulsion will further reduce the pollution (low emission batteries) and the dependence on oil.

Sensors for medical and healthcare applications

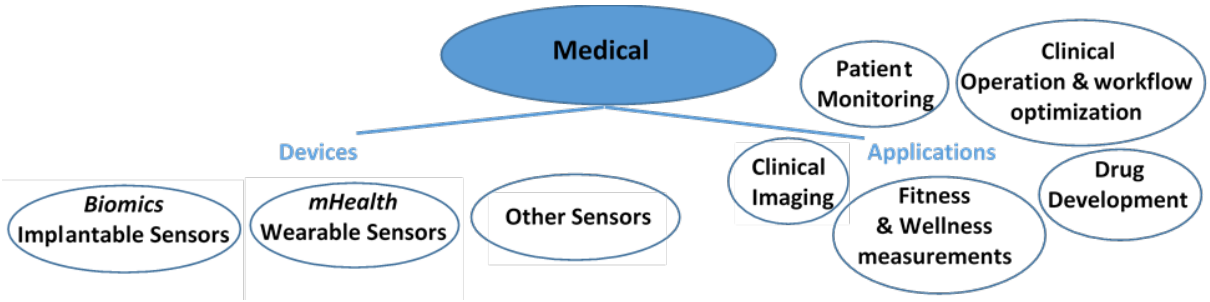
Recent research trends in IoT-based health include network architectures and platforms, new services and applications, interoperability, and security aspects[22]. In addition, policies and guidelines are needed for deploying the IoT technology in the medical field. The domain of smart health is developing very fast. The potential of the sensors technologies for healthcare originates in the expectations to have them in the future as key components of the healthcare cycle[23].

Sensors for medical and healthcare applications are categorized here as: *implantable*, *wearable*, and *other sensors*. Some of their main applications are patient monitoring, clinical operation and workflow optimization, clinical imaging, fitness and wellness monitoring, and drug development. The end-users for such applications includes healthcare providers, patients and active people, healthcare payers, research laboratories of pharma, biotech companies and government authority.

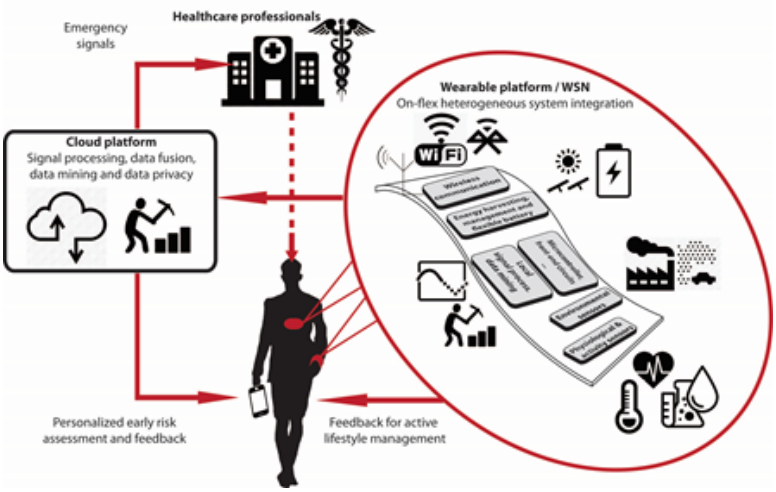
[21] Enviromental Gas Sensors 2017-2027, IdTechEx, (http://idtechex.com/research/reports/enviromental-gas-sensors-2017-2027-000-500.asp).

[22] S.M. Islam et al., *The Internet of Things for Health Care: A Comprehensive Survey*, IEEE Access, volume 3, 2015, pp. 678-708.

[23] A.M. Ionescu, presentation of CONVERGENCE Flag-Era project, Riga, 2017.



The figure below depicts the concept proposed by the European Convergence Flag-Era project for an energy efficient wearable platform with *embedded wireless low power bio- and environmental sensors* and energy management for preventive life-style and healthcare, including feedback loops, and data processing locally and in the cloud.



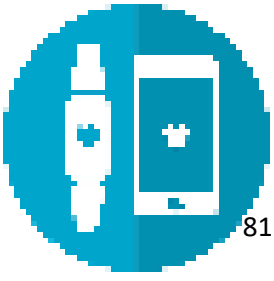
The main challenges for medical sensors are to have a good signal quality that filters motion artifacts from the medical grades sensing; frictionless technology with the right form factor and ideally non-contact sensing; autonomy or ultra-low-power designs; clinical validation where large scale of clinical studies/trials are required; and user adoption with the implies personalized algorithms and feedback.

In the automotive and other industries, additional common requirements for sensors are:

- Safety/security
- Miniaturization, weight
- Biocompatibility, manufacturability and cost
- Computing capacity and power
- Packaging and reliability
- Various sensing functionalities (genes, ADN, proteins, chemical species, position and orientation, interaction with ultrasound, with light, 3D surfaces, healthy or pathologic cells)
- Actuation: micro-pumps (drug delivery, micro-nano fluidics for biological samples analysis), movements (micro-robots, nano-particles), surgical tool control
- Energy harvesting and storage
- Biocompatibility and biodegradability

V.4.1.5.6. Concept 6: Physiological Signal Monitoring

Wearable devices (including mobile-based medical devices), provide real-time information such as heartbeat monitoring, cholesterol levels, calorie intake, quality, and quantity of sleep (apnea), oxygen levels, blood pressure, etc. Such biometric sensors embedded in clothing are called *smart textile*.



There is a strong demand nowadays for the monitoring of the physiological signals to enhance the well-being through healthier life-style, to prevent cardiovascular accidents or dehydration while doing fitness and to improve the management of chronic/acute diseases. It can serve for diagnostic, monitoring, treatment and prevention of cardiovascular, diabetes, respiratory and neurological diseases or for wellness & healthcare system strengthened solutions. Cardiovascular diseases would expect to generate the highest revenue among them.

Medical grade wearable sensors can be inserted in headphones or glasses, carried on the wrist (bands or watches) or on the body (hats, socks or shoes) and as neck wear. Their use is expected to increase in the healthcare sector thanks to increasing trend towards IoT and owing to evolution in circuit miniaturization, low power microcontrollers, front-end amplification, and wireless data transmission. In digital health monitoring systems, wearable sensors facilitate continuous physiological access and reduce manual intervention.

Wearables are intended to be non-invasive and they can provide the monitoring of multiple parameters as

- Hemodynamic Monitoring Devices
    - Blood Glucose
    - Cholesterol
    - Blood Gas & Electrolyte Analyzers/Monitors
    - Blood Pressure
- Neuromonitoring Devices
    - Electroencephalograph (EEG) Devices
    - Magnetoencephalograph (MEG) Devices
    - Intracranial Pressure Monitors (ICP)
    - Transcranial Dopplers (TCD)
    - Cerebral Oximeters
- Cardiac Monitoring Devices
    - Electrocardiogram (ECG) Devices
    - Implantable Loop Recorders (ILR)
    - Cardiac Output Monitoring (COM) Devices
    - Event Monitors
- Fetal & Neonatal Monitoring Devices
    - Ultrasound
    - Electronic Fetal Monitoring devices (EFM)
    - Fetal Doppler
- Respiratory Monitoring Devices
    - Capnographs
    - Anesthesia Monitors
    - Spirometers
    - Pulse Oximeters
    - Sleep Apnea Monitoring Devices
- Weight Monitoring Devices
- Temperature Monitoring Devices

These sensors are more and more often combined in multiparameter monitoring devices and sometimes used to monitor remotely the patient for better and less invasive diagnostic as for: CRD (Cardiac rhythm disorder), CHF (Congestive health failure), ADD (Attention deficit disorder), ASD (Autism spectrum disorder), obstructive sleep apnea, TBI (Traumatic brain injury), dehydration, etc. However, as important as the data are the algorithms to analyze and interpret the information more efficiently, requiring personalization to the patient, similar to the delivered treatment. In addition, there is an essential role of clinical partners to drive applications, systems requirements and definitions of validation tests.

Physiological sensors serve also to detect the incidence of health hazards caused by pollution (**air quality monitoring** described later) and rising concerns about health and well-being. Moreover, the need for easy and convenient patient monitoring techniques from a distant location could fill this existing application gap.

a- Table of concept 6 Physiological Signal Monitoring

	Medium term: 5+	Long term: 10+
Concept 6: Physiological Signal Monitoring		
a) Key research questions or issues		
Patient based devices	XXX	XXX
Hospital based devices	XX	XXX
Driver impairment Monitoring	X	XX
b) Potential for application or Application needs and Impact for Europe		
Patient based		
Blood glucose meter	XX	XX
Cardio meter (real time by a health patch)	XXX	XXX
BP monitor	XX	XXX
EEG monitoring for epilepsy for childrens	XX	XXX
Activity monitor – Actimetry	XXX	XXX
Fitness monitor (skin temperature, conductance, humidity, 3D accelerometer, ambient temperature with 100 h autonomy)	XX	XXX
Smart multifocal contact less for presbyopia	X	XX
Energy expenditure monitor (EE)	XX	XXX
Stress monitor	X	XXX
Hospital based		
Blood pressure meters & monitor (ECG, PPG)	XXX	XXX
Vital signal monitoring	XX	XXX
Apnea & sleep monitor (including EEG, EOG, EMG)	XX	XXX
Pulse oximetry (neurological monitoring device)	XX	XXX
Congestive heart failure (tracking fluids instead of a thorax radiography required)	XX	XXX
Chronic obstructive pulmonary disease	X	XX
Pregnancy contraction monitoring	X	X
Dialysis	XX	XXX
Driver Impairment Monitoring		
Alcohol-locking system	X	XX
Drowsiness mitigation systems	X	XXX
Driver inattention	X	XXX
c) Technology and design challenges	…	…
Ions and/or biomarkers sensors	XX	XXX
Temperature sensors	X	X
Pressure sensors	XX	XXX
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Sensor element power consumption	< 200 nW	<50 nW
Sensing time	1 min	
Resolution	>8 bit	>10 bit
Non-invasive	XXX	XXX
Multisensing	Activity parameters + a few biomarkers + air quality monitoring	Full activity and energy expenditure + Tens to hundreds of biomarkers + full environmental monitoring (air quality, allergens, pollens, etc.) + feedback for behavior engineering

Price	Low cost medical patches (~1-5 Euros) depending con complexity Smart sensing modules in wrist based devices (~10's Euros)	Paid by subscription services
PCR-free	?	Yes
Portability	Yes	Yes, full flexible embedding
Lifetime	Days to months	Months to years
e) Other issues and challenges, and interaction with other Tasks/WPs.	…	…
Certification and validation test procedure	Yes	Yes
Autocalibration	Yes	Yes

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period.

b- Competitive situation on Concept 6 Physiological Signal Monitoring

The top impacting factors for mHealth market are the cost and convenience (for the patient, the hospital, etc.). The technological innovations and integration of wireless technology in medical device is influencing faster adoption. The affordability of smartphones, government initiatives and increasing lifestyle diseases are secondary factors while the weak reimbursement coverage and the technological awareness among ageing population are not any more relevant in the medical industry. One of the key players in Europe is Philips Healthcare, but there are many European SME's and spinoffs in the medical sector than needs a further support to enter in the global market.

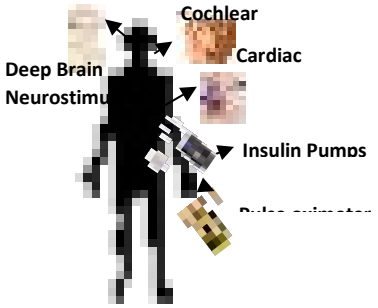
c- Recommendations on Concept 6 Physiological Signal Monitoring

Medical devices development including market introduction is very difficult nowadays, related to the long and tedious development stage, followed by the high cost of clinical validations, and the difficult process of CE labelling / FDA approval in case of novel device concepts (non-standard validation tests). As a consequence, the total device development period ranges typical from 10 to 15 years, and is very expensive, often unaffordable for standard SMEs and spinoff companies. The creation of a *European excellence consulting and advising clinical validation center* would support the development of novel medical devices and reduce the time to market for them. For example, it would be very useful to standardize some metrology or validation tests for the hermeticity of advanced device package methods (i.e. based on polymers combined with ceramic diffusion barriers). Issues are also seen with respect to security and privacy of patients having e.g. implants with remote control. The availability of guidelines regarding prevention of hacking would be an important help for European institutes and companies developing smart implantable devices.

V.4.1.5.7. Concept 7: Implantable sensors: Bionics

Bionics also known as biomedical implants are artificial additions to the body. These artificial implants mimic the function of the lost or non-functional natural organ such as limb or eye. Rise in geriatric population results in the upsurge in number of incidence of chronic diseases such as hearing and vision loss, cardiac disorders and neural disorders, with an important decrease in quality of life and dramatic increase in medical costs as consequence. In parallel, increase in technological advancements such as most recent pacemakers or cochlear implants (with speech recognition features), led to higher adoption of medical

bionics. However, high cost of these medical devices and corresponding medical treatment, as well as the stringent approval processes for medical devices are severe challenges, which hinder the market growth.



There are various domains for which the use of implantable sensors is considered very interesting (non-exhaustive list): vision (e.g. bionic eye), ear (e.g. cochlear or auditory brainstem implants), orthopedic (e.g. electrical bone growth stimulators), cardiac (e.g. pacemaker, artificial heart or heart valves, ventricular assist device), neural/brain (e.g. neurostimulators), etc. Not only medical implants but also devices in very close contact with body tissue are considered, such as smart contact lenses to restore vision.

Sensor devices used for medical implantations are based on a wide variety of technologies and working principles. In addition, some of them have been already described in other applications or concepts (such as the accelerometers). The implantable sensors roadmap table intends to cover the specificities, figures of merit, design challenges and key research issues common to most of known bionics. No specific application is selected in this concept.

a- Table of concept 7 Implantable sensors: Bionics

	Medium term: 5+	Long term: 10+
Concept 7: Bionics: implantable sensors		
a) Key research questions or issues		
Specificities of implantable sensors (figures of merit bellow)	Very critical to the final performance	
Validation tests and certifications (not defined by medical directives yet)	Difficult, expensive and time consuming	Certifications & validation tests defined by medical directives
b) Potential for application or Application needs and Impact for Europe		
Vision	XXX	XX
Ear	XX	XX
Orthopedic	XX	XX
Cardiac	XXX	XX
Neural/brain	XXX	XXX
c) Technology and design challenges		
Novel hermetic package technologies based on flexible polymers (for miniaturization and biomimetic devices)	R&D phase	Packaging solutions available
Wireless power supply (difficult when the sensor is deep in the body)	Induction allows only for implant depth of a few cm. Ultrasound and energy scavenging for deep implantation is in research phase	Power solutions for >10cm implantation depth available
Long-term sensor sensitivity and stability	5 years (A.D)	10-20 years (A.D.)
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Form factor/size	Small, flexible, biomimetic	Small, flexible, stretchable, biomimetic
Biocompatibility	Yes	Yes
Biostability	Yes	Yes
Battery size	Small, flexible	No battery?
Tissue heating	Critical (related to the	Controlled

	power consumption)	
Lifetime determine by the long-term sensitivity in order to avoid explantation	A.D. Not relevant for drug releasing devices	10-20 years (A.D.)
Autonomous sensors		
Energy harvesting	Early research, only very limited energy can be harvested	R&D, only limited energy harvested but OK for devices with ultra-low power consumption
Remote/wireless power transmission	Few cm implantation depth using induction.	For >10cm implantation depth alternative power transmission methods such as ultrasound
Wireless communication and device control	Low data rate/ device control	
Price (determined by local government, not by medical device manufacturer. Reimbursement by health insurance is important issue.)	Not very critical since the entire process is very expensive. (e.g. surgery, follow up in intensive care unit, etc.)	

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first in this time scale, A.D: This metric is application dependent.

b- Competitive situation on Concept 7 Implantable sensors: Bionics

Europe is well positioned for the medical market, as most of these sensor applications require extremely high reliability (failsafe devices) and a very accurate fabrication because the quality of the final product is very important. Although the cost of the final device is not unimportant, 'cheap fabrication' is not the rule, since quality and reliability is of utmost importance. The development of a medical implant is very difficult, since many scientific domains have to be combined. Highly educated scientists of many disciplines have to collaborate to fabricate a device with required quality, safety, and efficacy. Europe is ideally suited to perform such scientific work, since highly educated personnel is available, and since the cost requirements for an implanted medical device or more relaxed compared to quality requirements. An example of this fruitful multidisciplinary research is the recent application of motion sensors across the medical & healthcare sector, resulting in an interesting opportunity for future growth in the European sensor market as well as medical device market.

c- Recommendations on Concept 7 Implantable sensors: Bionics

The recommendations applied in concept 6 remain valid for this section.

V.4.1.5.8. Concept 8: Molecular Diagnostics

Molecular diagnostics technique is used to detect specific sequences in DNA or RNA, including single nucleotide polymorphism (SNP), deletions, rearrangements, insertions and for analyzing biological markers at the molecular level, such as genome and proteome; for diagnosis of the various infectious diseases, cancer, and other diseases/disorders; and to check the risk of genetic predisposition for a disease. Infectious disease diagnostic is an important application gap, owing to the increase in the number of patients suffering from viral and bacterial infections worldwide such as Human Immunodeficiency Virus (HIV), Hepatitis C virus (HCV), Human Papillomavirus (HPV), Chlamydia trachomatis/ Neisseria gonorrhoeae (CT/NG). Fast, simple and low-cost infection

diagnostics directly at the patient bedside remains an unmet need in the health-care diagnostics market. Currently, rapid tests are available only for the simplest biological parameters (e.g. C-reactive protein, procalcitonin). For complex and life-threatening infectious illnesses however, reliable diagnostics can take place only through laborious and time-consuming procedures with the participation of a central laboratory employing qualified specialists.

The molecular diagnostic technology is categorized into polymerase chain reaction (PCR), hybridization, DNA sequencing, microarray, isothermal nucleic acid amplification technology (INAAT), and others (electrophoresis, mass spectroscopy, and flow cytometry). PCR contributed to the highest share in 2016, owing to the increase in usage in proteomics and genomics, which is highly cost-effective. Based on application, it is divided into infectious diseases, oncology, genetic testing, blood screening, and others (microbiology, neurological diseases, and cardiovascular diseases). End-users are hospitals, reference laboratories, blood banks, home health agencies and nursing homes.

The label free detection method is used for detecting biomolecules and their interactions. It is divided into cellular dielectric spectroscopy, bio-layer interferometry, surface plasmon resonance, optical waveguide grating technology and others. Within the products, there are biosensor chips and microplates. Specific applications related to label free detection are binding thermodynamics, binding kinetics, hit confirmation, lead generation and endogenous receptor detection.

a- Table of concept 8 Molecular Diagnostics

	Medium term: 5+	Long term: 10+
Concept 8: Molecular Diagnostic		
a) Key research questions or issues		
Lab-on-a-chip	XX	XXX
b) Potential for application or Application needs and Impact for Europe	…	…
Infectious disease, cancer and other disorders medical diagnostic	XXX	XXX
DNA probe/target recognition	XX	XXX
Single particle or virus detection	XX	XXX
Counting of particles/Particle trajectory tracking/Imaging	X	XX
Biological markers analyzer (e.g. acetone in breath for diabetes)	XX	XXX
m-RNA in blood (for cancerous tumours treatment efficiency)	XX	XXX
c) Technology and design challenges		
CMOS Capacitive Sensor	DP	Market intro?
Label-free based on FET SC NW	R&D	DP
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
Number of parallel diagnostics	XX	XXX
Sensitivity/detection limit	XX	X
Price	XXX	XXX
PCR-free		Yes
Portability	XX	XXX
Power consumption/autonomy	XX	XX
Lifetime	XX	XX

Note; XXX: Critical, high priority or more probably to come first, XX: Less critical, middle priority or less probable to come first, X: no critical, lower priority or unprovable to achieve it in this time-period, R&D: research and development, DP: Demonstration and Prototype, RS: Regulations and Standards

b- Competitive situation on Concept 8 Molecular Diagnostics

Key player in the biomolecule diagnostic market includes Novartis AG, Siemens Healthcare GmbH, Roche Diagnostics and Bayer Healthcare among others.

c- Recommendations on Concept 8 Molecular Diagnostics

It addresses the need for better diagnostics and targeted therapeutic tools for physicians, athletes or patients (as dose reminder).

V. 4.1.6 Synergies with other topics

The synergies of all the concepts and interactions with other workpackages are common for all the described concepts and are summarized below.

- **Connected objects and Internet of things (IoT) – Task 3.2 Connectivity.**

The connectivity technology is 2G, 3G, and 4G/LTE and can be integrated, embedded for navigation, telematics or infotainment applications. Fast connection to the wireless network and advanced infotainment systems are the two most prominent features. Connected cars facilitate connectivity on wheels offering comfort, performance, safety, and security combined with powerful network technology. In addition, this enables interconnectivity between two connected cars as the Machine-to-Machine (M2M) connectivity platform and numerous sensors and processors located in the car can provide accurate and real-time information to the driver.

Internet of things (IoT) is basically the networking of smart electronic devices or things to transmit data signals. It includes the devices, system & software and services. IoT technology will revolutionize the traditional paper-based healthcare treatment through simplifying access of real-time patient data and remote patient monitoring due to the growing demand for cost-effective treatment and disease management. This includes also the healthcare information technology (IT) infrastructure that intends to act as a bridge between all the medical entities and minimizes manual errors. Increasing exposure to smartphones along with 3G and 4G networks will further increase the use of mobile platforms in the healthcare systems (mHealth).

- **Zero-power or Self-powered Sensors – sub Task 4.2 Power for Autonomous Systems**

Energy efficiency per electronic function needs progress. The enabling zero-power approach will be disruptive overall for efficient autonomous systems. The combination of low power sensing and energy harvesting appears to be the most elegant solution. However, batteries implemented efficiency can extend sufficiently the lifetime of the device (5-10 years) and environmentally friendly printed batteries can be the solution for limited lifetime devices (few months).

- **Sensor Fusion and Wireless Sensor Network (WSN) – Task 5.1 System Design**

Multiparemeter sensing (as for medical diagnostics and healthcare monitoring), sensor fusion (as for the cameras in a car) are relevant applications that need to be study at system level including the network, the database (big data and security issues) and the analytics layer (algorithms).

WSN is a network of distributed autonomous sensors placed at a remote plant area, which uses the wireless technology to send signals or measurements to a control room thereby monitoring physical or environmental conditions. Battery enabled power is one of the main challenge to success.

- **Sensor packaging– Task 5.2 Heterogeneous Integration**

The packaging is considered as the most important feature to take into account in the sensor design and development (System in Package SiP versus System on Chip SoC). It is considered to be even more important than materials especially for bionic sensors and it make more sense for its optimization than the sensor itself. Close collaboration with WP5 is needed to create a specific sensor packaging road-mapping

- **Eco-system – WP6**

A full eco-system (“from transistor to housing”) which includes the multi-domain co-design (chip, package, system) and the reliability are general challenges from the automotive and health markets covering the technologies and packaging. Smart sensors manufacturing ecosystem in Europe is needed to avoid that the sensor market is monopolized by a few. With the design done by research institutes or universities,

standard frontend and backend, control of wafer compatibility, secure shipping/processing of wafers and high throughput at high quality is the way to success in the future.

V. 4.1.7 Recommendations

General recommendations for the smart sensors in the automotive and in the medical/healthcare segment described previously are the following:

- **Shared manufacture infrastructure cost** with other applications (e.g. between automotive and consumer), improved processes that further lower cost (like CMOS MEMS) or the creation of new devices with added value (e.g. software embedded within the sensor to deliver higher level functions) are some ways to improve margins as for example in MEMS market.

- **CMOS integration, compatibility and readout circuitry**. New enabling technologies keep coming. However, integration becomes more challenging and reliability gets less predictable. It is predicted that smart sensors will remain as close as possible to CMOS standards.
- **Stability and reliability** are the two most important features for the industrial take up of smart sensors. High reproducibility, ppb detection limits due to concentration, signature for functionalization, form factor and the power consumption of the platform are secondary characteristics that have to be taken into consideration for the sensor development. As mentioned already, selectivity is not the most important feature for sensing.
- **Regulations and guidelines** are required to limit vehicle emissions and thus further reduce pollution and dependence on oil, to stablish emission standards that dictate the limits of pollutants (CO_2, NO_x, etc.) in indoor and outdoor air environments. Vehicle safety regulations are also a priority for Europe to reduce 50% of road accidents (cars, bicycles, pedestrian, etc.) by 2030. On the other hand, the different regulations and languages among national health organization are not helping to develop the medical market in Europe. Medical devices development including market introduction is very long (minimum 10 to 15 years), expensive and difficult nowadays, related to the long and tedious development stage, followed by the high cost of clinical validations, and the difficult process of CE labelling / FDA approval in case of novel device concepts (non-standard validation tests). The creation of a *European excellence consulting and advising clinical validation center* would support the development of novel medical devices and reduce the time to market for them.
- **Assembly testing, standards and metrology** are crucial for the future success of smart sensors. There is a lack of metrology standards, commonly is difficult to interpret and it results in time consuming investigations.
- **Auto-calibrated**, self-calibrated or an easy way of sensor calibration is not a common feature for the sensors in the market yet. However, this is highly interesting and required for future industrialization and a long-term sensor stability. As an example, CMOS capacitive sensors have the advantage that they do not need to be calibrated but it might have a poor sensitivity.
- The **maturity level** of each sensor technology has to be assigned, estimating than a technology with a TRL higher than 6 would result to a product into market in less than 3 years approximately. The standards will be pushed very high in the different road-mapping but without excluding any technology for the next 10-year long term projection. The reason is that some application domains need mostly performance as in military while for others is the cost the most important factor or the repeatability, stability, reliability and yield for huge volume productions. A clear TRL correlation with technologies needs to be established.

Thus, some of the smart sensor identified gaps by 2030 concern: manufacturability and cost (hybrid integration), low power consumption (energy efficiency), robustness of design and in production, and reliability.

V. 4.2 Smart Energy (T4.2)

V. 4.2.1 Executive summary

Power devices based on wide bandgap semiconductors (WBS), like GaN, SiC, Ga_2O_3, are poised to play an important role in future power electronics systems. WBS has a high breakdown strength and, in the case of GaN, allows for fabrication of high electron mobility lateral transistors, for which the electron mobility is not degraded as would be the case for traditional silicon MOSFETs. These facts combined allow the fabrication of devices which have orders of magnitude better trade-off between the specific on-resistance of the devices and the breakdown voltage.

The roadmap for devices has been set up along three tracks, the first considers the GaN based devices starting from materials towards integration. The second track is related to the evolution of SiC (again from materials to applications). Finally future material systems (AlN, Diamond, Ga_2O_3) are considered which could offer benefits over the actual WBS in certain domains.

V. 4.2.2 Relevance and competitive value

Power Electronics is the technology associated with the efficient conversion, control and conditioning of electric energy from the source to the load. It is the enabling technology for the generation, distribution and efficient use of electrical energy. It is a cross-functional technology covering the very high Giga Watt (GW) power (e.g. in energy transmission lines) down to the very low milliWatt (mW) power needed to operate a mobile phone. Many market segments such as domestic and office appliances, computer and communication, ventilation, air conditioning and lighting, factory automation and drives, traction, automotive and renewable energy, can potentially benefit from the application of power electronics technology. The ambitious goals of the European Union to reduce the energy consumption and CO_2 emissions can only be achieved by an extensive application and use of Power Electronics, as power electronics is the basic prerequisite for:

- Efficiently feeding-in wind and solar energy to the grids;
- The stabilization of the power grids with increasing share of fluctuating renewable energy sources;
- Highly efficient variable speed motor drives;
- Energy efficient and low-emission mobility with hybrid and full electric vehicles;
- An energy saving lighting technology;
- Efficient recovery of braking energy;
- Energy management of batteries;
- Control appliances and building management systems via the grid interface (smart grids).

V. 4.2.3 Vision

Smart Energy has the ambition to ensure the European technological capabilities needed for generating, distributing and consuming electrical energy and for replacing with electrical energy other sources like mechanical, hydraulic or combustion engines. The Smart Energy Task focus on the definition of the roadmap for technologies, materials, integration methodologies and processes for the realization of more efficient power management devices. Roadmaps for smart power need to cover different sectors:

- New highly efficient power devices based on high gap semiconductor materials, like GaN on Silicon and later Diamond on Silicon.
- High temperature capable packages serving new materials and 3D technologies with lifetimes fulfilling highest requirements and the integration capabilities for new kind of different interface conditions.

V. 4.2.4 Scope and ambition

The Smart Energy roadmap will present the medium and long term targets of the two main WBS, (SiC and GaN) as well as for the new promising WBS: Ga_2O_3, AlN, and Diamond. The aspects that will be covered within this roadmap are: i) materials and processing issues (including device architectures), ii) Applications, iii) Technology and design challenges; iv) Figures of Merit.

V. 4.2.5 Main Concepts

V.4.2.5.1. Concept 1: GaN-devices and substrates

Substrate Diameter: Today, 6"- 8" wafer size, low vertical leakage current, current collapse free GaN-on-Si wafers are available on the open market. Pricing for such material has come down significantly in recent years. It is generally agreed that the magic cost target of 3$/cm^2 for epimaterial, which is also the price point at which GaN technology becomes cost-competitive with Si-based components at the device-level, can be achieved within the next couple of years under the important assumption that the wafers can be produced in volume. A next logical evolution would be to make the transition to 300mm wafer diameters, but it is as yet an open question whether this makes sense from an economical as well as technical perspective.

Voltage Rating: Standard products of GaN-on-Si typically feature an epilayer thickness of 4µm to 6µm, yielding a voltage handling capability of 650V, including derating for temperature and lack of avalanche capability. Recent literature reports on boosted voltage rating of epiwafers, by improvements in epitaxial recipes as well as increased layer thicknesses, to values beyond 1200V. However, due to the high intrinsic strain in GaN-on-Si layer stacks as well as the drive towards the adoption of semi standard substrate thicknesses, there is a fundamental limit to the maximal thickness (and breakdown voltage) that can be achieved.

Transport properties: The hetero-structures are typically based on AlGaN barrier material and have a sheet resistance of around 400 Ohm/sq (which directly influences the devices' on-state resistance). Future developments will see the sheet resistance reduced to values below 200 Ohm/sq. by adopting highly polarised AlN barriers or by using lattice matched InAlN barriers.

Vertical Devices: Besides lateral devices, there is also discussion on vertical devices. These hold the promise of higher attainable power densities as well as avalanche capability, but they lack the benefit of electron transport along the 2 Dimensional Electron Gas (2DEG). The vertical current flow makes this type of devices more sensitive to (vertical) threading dislocations, which pushes this technology towards growth on native GaN (or AlN) substrates. The latter are currently only available in small diameters and at a very high cost: significant progress on both aspects is required to make this a viable approach. Nonetheless, recently vertical GaN-on-Si devices were demonstrated for the first time[24]. An alternative track is possible to circumvent the high cost of bulk GaN substrates, which will need to come down significantly before devices can be produced economically, namely growing on foreign substrates (GaN-on-X), where X should be a substrate which allows high quality GaN growth with higher quality and thicker buffers compared to what is currently possible on silicon.

On Chip Integration: A further path to cost reduction for GaN technology is to include several components on a single chip, allowing to save component, packaging and design costs for creating a full system. Beyond merely costs advantages, a monolithic integration will also enable the main potential of GaN to be tapped, which is a high commutation speed, leading to an increased switching frequency for the power circuit. Discrete Si power components can be quite readily integrated in a power circuit, however GaN components can deliver high power at a fast switching frequency. These properties lead to a stringent requirement on the design of circuit and interconnect parasitic. Integrating e.g. two switches

[24] Mase et al., Applied Physics Express 9, 111005 (2016).

on a single die can also significantly reduce interconnect parasitic, offering further system level performance benefits.

a- Table of concept 1 GaN-devices and substrates

	Medium term: 5+	Long term: 10+
Concept 1: GaN substrates and devices		
a) Key research questions or issues		
GaN-bulk Material	Defect Density Quality Wafer size, 6” Cost	Defect Density Quality Wafer size, 8” Cost
GaN-on-Si substrate	Cost Dislocation density <1 E9/cm2 Further deepened understanding of defects and their relation to reliability	Wafer size scale up to 12” Dislocation density <1 E8/cm2
Normally OFF devices	Gate leakage Reliability Avalanche & short circuit robustness Cost/die	Isolated gate device Smart power GaN
Vertical devices	Cost Performance Reliability Gate dielectric Robustness	Cost Reliability
b) Potential for application or Application needs and Impact for Europe		…
Low power DC/DC converter (POL)[25]	Volume	Predominant
Power supplies (PFC[26], e.g. for data centre)	Volume	Predominant
Automotive EV/HEV (DC-DC converter, charger)	Prototype	Volume
PV (roof/home)	prototype	Volume
c) Technology and design challenges		…
GaN-on-Si substrate diameter	Cost Wafer size, 8”	Cost Wafer size, 12”
GaN-on-Si substrate thickness	Semi std	
p-Gate architecture	Selective Regrowth Polarization engineering	Polarization engineering Others
Gate recess	(selective) Regrowth Dit engineering	
MIS-Gate structures	(selective) Regrowth Dit engineering	
Ohmic contacts		Regrown contacts
On-Chip Integration	Topology Reliability Thermal management Packaging	Cost
d) Definition of FoMs (quantitative or qualitative) or		…

[25] POL: Point of Load
[26] PFC: Power Factor Correction

planned evolution (based on SoA @ 2017 and evolution vs time)		
R_{on} x A (Reduction vs 2017) 100V: 35 mΩ.mm^2 600V: 5 mΩ.cm^2	1/2 100V: 17mΩ·mm^2 600V: 2.5mΩ·cm^2	1/4 100V: 9mΩ·mm^2 600V: 1.2mΩ·cm^2
R_{on}·Q_g 100V: 40 mΩ.nC 600V: 400 mΩ.nC	100V: 20 mΩ.nC 600V: 200 mΩ.nC	100V: 10 mΩ.nC 600V: 100 mΩ.nC
R_{on}·Q_{oss} 100V: 200 mΩ.nC 600V: 4000 mΩ.nC	100V: 100 mΩ.nC 600V: 2000 mΩ.nC	100V: 500 mΩ.nC 600V:1000 mΩ.nC
Ig	<1µA/mm	<10nA/mm
Vth **(at I_{DS} 10µA/mm)**	>2.5V	>3.5V (tunable Vth 1V to 5V)
Lifetime **(yrs @ Temp)**	10yrs at 150°C	20yrs at 175°C
Parasitic Charge (**Reduction vs. 2017)**	-50%	-75%
Robustness	10µs at 80% of Vrating	>10µs at 100% of Vrating (or 5years)
e) Other issues and challenges, and interaction with other Tasks/WPs.		…
Parasitic (current collapse) **over full V and T range**	<10%	<5%
Reliability issues	Proven field failure rate <1FIT[27]	Proven field failure rate <1FIT

b- Competitive situation for concept 1 GaN-devices and substrates

GaN semiconductor devices provide a competitive advantage in terms of thermal performance, efficiency, weight and size. GaN is anticipated to be the next generation power semiconductor and thus different countries are indulged in developing widespread applications of GaN semiconductors. The wide band gap semiconductor technology has matured rapidly over several years. In fact, Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have been available as commercial off-the-shelf devices since 2005.

c- Recommendations for concept 1 GaN-devices and substrates

One of the major restraints of the GaN semiconductor devices market is the high production cost of pure Gallium nitride as compared to silicon carbide, which has been a dominant semiconductor material for high voltage power electronics for a decade. The various costs involved in the production of GaN devices include cost of substrate, fabrication, packaging, support electronics and development. Thus, high cost is one of the major challenges in the commercialization of GaN based devices. Though producing GaN in large volumes can help overcome these issues, currently, there is no widespread adopted method for growing GaN in bulk due to high operating pressures and temperatures, low material quality and limited scalability.

V.4.2.5.2. Concept 2: SiC-based substrates

Power semiconductors are the key components of any power electronics circuit. Compared to the standard material silicon, SiC has superior properties for the application in power electronics, i.e. higher breakdown voltage, lower losses as well as the capability for high frequency switching and high temperature operation. These performance data are related to important material properties, e.g. higher energy bandgap, breakdown electric field, and thermal conductivity.
Recently, SiC devices with breakdown voltages of 10 kV and higher have been developed for MV applications. This voltage rating noticeably surpasses that of commercial Si devices, such as 6.5 kV IGBTs.

[27] FIT: Failures In Time

The breakdown voltage rating of this new device generation has not yet reached its limit. Latest SiC High Voltage (HV) power semiconductors, for example, MOSFETs, IGBTs, diodes and GTOs are presented that offer innovative opportunities for medium-voltage applications. These properties make SiC the ideal material for high current density devices at high voltages.

a- Table of concept 2 SiC-based substrates

	Medium term: 5+	Long term: 10+
i) Concept 2: SiC substrates and devices		
a) Key research questions or issues		
Thick epi layers with low defect density for high operating voltages	Enhanced growth rate	Life time defect engineering
Trench power devices with high gate oxide reliability	Enhanced mobility	Novel architectures
Bipolar devices (e.g. n-IGBT, BiFET)	Enhanced minority carrier lifetime	Compensation devices
Solid state circuit breakers	Low loss designs	High blocking voltages
High-reliability power devices (exceptional lifetime, e.g. for aviation applications) and driver circuits	Rugged design, low defects	Higher integration density
b) Potential for application or Application needs and Impact for Europe		…
Power supplies (PFC, e.g. for data centre)	Volume	Volume
PV (roof/home)	Volume	Volume
PV (MV, central)	Volume	Predominant
Automotive EV/HEV (DC-DC converter, charger)	Volume	Volume
Automotive EV/HEV (traction inverter)	Volume	Predominant
Motor drives (industry)	Volume	Predominant
Traction (trains, trams)	Volume	Predominant
Wind power	Volume	Predominant
Grid: power transmission and distribution (e.g. HVDC)	Prototype	Volume
Airplanes	Prototype	
c) Technology and design challenges		
Advanced passivation for high voltages and 3D integration	In the substrate	On the chip
Self-aligned process techniques for high manufacturability (e.g. TrenchMOS)	Prototype	Volume
Wafer thinning and bonding	R_{on} reduction	n-IGBT
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		…
R_{on}	1/2	1/4
Idss	2x	4x
Lifetime (yrs @ Temp)	10yrs @ 175°C	20 yrs @ 225°C
Parasitic Charge	0.5x	0.4x
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Novel methods for accelerating life-time testing	On chips	On modules
Novel reliability models	For chips	For modules

b- Competitive situation of concept 2 SiC-based substrates

SiC is on the verge of market penetration for very high current densities and high voltages over 1000V with

the potential to allow for voltages far above 10kV, being the most promising material. Next to the improvement of the device parameters and extending the limits, the appropriate integration of such advanced devices in new module architectures is of utmost importance to exploit all the benefits of the devices.

c- Recommendations for concept 2 SiC-based substrates

It is highly recommend focusing on the growth of thick epitaxial layers with low defect densities, e.g. high current density devices, and high carrier lifetimes for high voltage devices, e.g. bipolar devices. To really deal with the high voltages the passivation on chip, e.g junction termination or advanced in chip passivation, as well as in the module for 3D integration has to be addressed.
Next to the costs and the yield of the SiC devices, the reliability issues have to be addressed. The current devices show a high robustness against high voltages and temperatures. But, to derive adequate reliability and life time predictions, novel accelerating life-time testing and modelling of these devices have to be established. To exploit all the benefits of high current and high voltage devices, advanced 3D integration concepts have to be developed.

V.4.2.5.3 Concept 3: Alternative Wide Bandgap Semiconductors

Besides GaN, a number of other wide-bandgap materials exist. The most cited is diamond that is considered to be the “ultimate material”. However, technological obstacles (lack of efficient n-type doping, conductive surface channels and difficulties to make ohmic contacts) have for a long type blocked the demonstration of performant devices. Unless spectacular progress is made on these issues, no real-world implementations are foreseen and as such diamond is not included in the roadmap. Besides SiC (for which a separate part of the roadmap is dedicated), we identify two major candidate materials: AlN and Ga_2O_3.
AlN native substrate is probably the most interesting wide bandgap material, because it combines high thermal conductivity with a very large bandgap of 6.2eV, higher than that of diamond. It can easily be combined with GaN-based materials to form heterojunctions (such as HEMTs). Finally, it shares its growth method to make AlN bulk boles with SiC, for which a mature commercial supply chain exists, up to 6” and at reasonable pricing, so that it can at least be envisaged that also AlN bulk substrates reach a similar level of maturity over time. Currently few AlN bulk substrate suppliers exist (Hexatech, Crystal-N) and the substrates are 2” in diameter or below.
Gallium oxide (Ga_2O_3**)** is the latest semiconductor in the block of wide bandgap materials. As it can be grown from the melt, it is potentially a low-cost material. It can be easily doped to make vertical devices and can be combined with Al_2O_3 as a gate dielectric. Recently, a number of publications reported on promising device characteristics. Ga_2O_3 is a material system which allows processing devices with improved breakdown voltages compared to SiC and even GaN. However, the main advantage stems from the fact that the material can be grown from the melt and can thus be produced at very cheap rates when compared to GaN & SiC. However the main disadvantage of this material is the very low thermal conductivity, which is a really undesirable property of power devices. Further research will have to demonstrate if devices can be fabricated which can overcome this issue.
Diamond is considered by many the ultimate material for fabricating power components. It has the highest breakdown strength of any known material, combined with an extremely high thermal conductivity. However, due to the wide bandgap it is also challenging to find a suitable dopant for diamond. Apart from this the growth of the material is also quite challenging. Initial demonstrator transistors are available in diamond, but much work will be needed to improve performance towards practical performance and demonstrate the capabilities of the material system.

a- Table of Concept 3: Alternative Wide Bandgap Semiconductors

This table refers to very new/innovative materials, where figures of merits are not clearly finalized yet. Most of these figures of merit will be added/finalized in the final version.

	Medium term: 5+	Long term: 10+
i) Concept 3: Alternative Wide Bandgap Semiconductors		
a) Key research questions or issues		
AlN-bulk Material	Cost Wafer size Supply chain	Cost Wafer size Supply chain
Ga_2O_3 substrate	Wafer size Supply chain p-doping mobility	Supply chain
Diamond	Cost Wafer size Supply chain	Cost Wafer size Supply chain
b) Potential for application or Application needs and Impact for Europe		…
Power switching converters		Sampling
Automotive		
Data Center		Sampling
c) Technology and design challenges		…
Thermal conductivity		…
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
R_{on}	will be completed in the Second part of NEREID Project	
Idss		
Vth		
Lifetime		
Parasitic Charge		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Parassitic (current collapse)		
Reliability issues		

b- Competitive situation Table of Concept 3 Alternative Wide Bandgap Semiconductors

Competitive situation will be added in the final version.

c- Recommendations for Table of Concept 3: Alternative Wide Bandgap Semiconductors

Recommendations will be added in the final version

V. 4.2.6 Synergies with other topics (WP topics, if applicable)

No synergy with other WP could be identified at this stage.

V. 4.2.7 Recommendations (of the WP topic)

Apart from WBG device development the WBG system integration is necessary to exploit the full potential.

- Packaging and system integration technologies enabling low parasitic inductances to master EMC[28] issues
- Packaging and system integration technologies enabling reliability at higher temperatures
- Handling higher voltages on package/module level and system level: SiC in medium voltage (MV) applications e.g. in traction and industry
- Low inductance packaging and integration technologies: power PCB with chip embedding, system-in-package (SIP), switching cell in a package
- Passive components for fast switching: mainly inductors, reduce losses at high switching frequencies, thermal management of (integrated) passives
- Characterisation, testing, modelling and reliability analysis of WBG packages, modules and converters

V. 4.3 Energy for autonomous systems (Sub T4.2)

V. 4.3.1 Executive summary

As the communicating systems market is booming, the role of energy harvesting (EH) will be growing. Indeed, the number of connected devices is planned to increase by a huge factor of 200, while the number of mobile phones is just planned to increase by a factor 3. Connected devices are going to be used more and more in several fields such as healthcare, wearables, home automation, etc. The Internet of Things (IoT) market grows considerably leading also to the boom of the connected devices, and so highlighting the importance of energy needed to supply them in view of the limitations of current battery technology. In this particular case, we are focusing on small connected devices with low power consumption below a few mW (or even a few tens of µW).

Different wasted energy sources can be exploited and converted into electricity: sun or artificial light, heat, mechanical movements and vibrations... Moreover this converted energy needs to be used and transferred wisely to sensors, microcontrollers or other electronic components included in the system. Thus power management circuitry becomes also an essential element.

In this mid-term roadmap report, we have assessed several promising technologies for EH and power management circuits including photovoltaic cells for outdoor/indoor light EH, mechanical EH based on two concepts: piezoelectric materials and electrostatic energy conversion, and finally the power management circuits. Other promising technologies will be covered in the second half of the project.

V. 4.3.2 Relevance and competitive value

Providing energetic autonomy to electronic devices will be a key factor in booming technologies like sensor networks and IoTs. This is true for applications with specific requirements, where a simple battery would not be sufficient, where using power cords increases largely the cost or complexity (i.e. avionics), or when the number of devices are so numerous that changing batteries could increase the cost. Other examples are in harsh environment were the electronic devices could not be reached/accessed easily, or in biomedical devices. The interest of the EH concept will be also to develop new devices compatible with Silicon technologies for implementation in the fabrication line, which would attract the interest of semiconductor companies. New green solutions based on non-toxic, widely available materials would be of high interest for the dissemination of energy harvesters.

[28] EMC: ElectroMagnetic Compatibility

V. 4.3.3 Vision

Dissemination of energy autonomous electronic devices will only be possible if it is driven by applications. Currently, the energy that can be generated from small EH devices is quite low with most of the technologies, but this could be sufficient for many sensing applications, knowing the fact that energy is in general randomly generated. In addition, research is progressing towards the development of micro-power architectures of application circuits. The evolution of the EH technologies will enable a growing number of possible applications and products to be placed on the market, which were unfeasible up to now. In the medium (>5 years) and long term (>10 years) roadmap of the covered technologies, we expect an increase on their performance or efficiency (more electrical energy produced for a given available energy). For the long term in particular, new materials (polymers, triboelectric materials, organic, perovskite…) and nanotechnologies will be used to obtain higher performances but also to replace toxic/rare materials used today (i.e. Bi2Te3 in thermal EH and lead based materials for piezoelectric conversion).
Power management circuits are expected to require lower input power (<100nW), input voltage (<10mV) and smaller surfaces (<mm^2) in the long term.

V. 4.3.4 Scope and ambition

Targeting EH technologies with low fabrication cost, with high efficiency, and without toxic/rare materials is the main challenge. Adding flexibility is also an increasing demand for compatibility with wearables applications.
For the semiconductor companies, the interest is also to develop new devices compatible with Silicon technologies. The fabrication of components dedicated to energy harvesting and in particular to thermal energy is of high interest as no solution based on silicon technologies is available for implementation as of today.
Mechanical EH rely typically on input vibrations, and one of the main challenge is the compatibility with low frequency vibration source (most of applications use frequency vibrations <100Hz) and the increase of the frequency bandwidth.
Although photovoltaic EH technology is mature (silicon based) for both outdoor/indoor applications, emerging materials are promising for their potential to add flexibility and low weight (thin films) at reduced cost and high efficiency (organics, dye sensitized, perovskites, etc.).
The main challenges associated to power management circuits are related to the miniaturization of the system embedding micro-transformers or power converters, the reduction of overall leakage enabling low power consumption and the development of energy-aware circuit design techniques.

V. 4.3.5 Main Concepts

V.4.3.5.1. Concept 1: Mechanical EH: Electrostatic transduction

The principle of operation relies on the use of mechanical forces to do work against the attraction of oppositely charged capacitor's plates; thus those generators can be considered as mechanically variable capacitors whose plates are vibrated by the movement of the vibration source. Typical structures include capacitor plates in form of fingers installed in central oscillating mass and in stationary comb. When the capacity is at its maximum value the electric charge stored in the capacitor is transferred to the external battery. To insure good capacitive coupling between the oscillating mass and stationary comb, the distance between fingers has to be as small as possible. In order to avoid the charging and discharging cycles, electrets (dielectric material with trapped electrical charges) can be implanted into one of the two parallel electrodes. This technology is a promising solution for CMOS-compatible, low cost, micro scale EHs. Most of the challenges will rely on the development of stable materials able to keep the electrical charges over many years and related to mechanical structures that can work in a large frequency bandwidth, in order to improve the harvested energy.

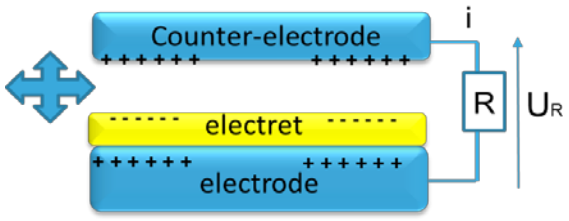


Figure XX. Cantilever-based electret energy harvesters[29]

a- Table of concept 1: Mechanical EH: Electrostatic transduction

Concept 1: Mechanical EH: Electrostatic transduction	Medium term: 5+	Long term: 10+
a) Key research questions or issues		
Improve efficiency with a reduced surface, volume	New materials: Fluorin polymers / surface texturation	Fluorin polymers / surface texturation
Increase input bandwidth, reduce working frequency for portable applications, adaptable devices	Non-linear mechanical systems for larger frequency bandwith >30Hz	>100Hz
Improve scalable technologies at low cost / related to efficiency -> but miniaturization reduce the energy	Higher energy density	
Increase reliability of integrated systems / stability vs time / keep polarization and charges >10years Increase performance of electret materials (charges leakage reduction)	Develop stable layers with time (polymers)	Encapsulated SiO_2 / triboelectric materials
b) Potential for application or Application needs and Impact for Europe		
Industrial / Infrastructures monitoring for security (autonomous sensors) - on vibrating sources	Harvesting on pumps, industrial machines	
Develop wireless autonomous monitoring in transportation (car, planes…)	Harvesting on railway, train	Harvesting on cars, planes
Develop Wearable systems (electrostatic materials / triboelectricity) for human movement harvesting	Shoes	Medical patches
c) Technology and design challenges		
Develop low cost solutions and flexible approach to conform body	Optimized polymers	Low cost polymers
Develop triboelectricity	Fluorin polymers / surface texturation	Low cost
d) Definition of FoMs		
Volume power density (mW/cm^3) @1G[30]	0.5mW/cm^3 (100Hz)	1mW/cm^3 (100Hz)
Volume energy per cycle[31] (µJ/cm^3) @1G	5µJ/cm^3 per cycle	10µJ/cm^3 per cycle
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Power consumption of power management circuit		
Develop applications		

b- Competitive situation for concept 1 Mechanical EH: Electrostatic transduction

[29] *S Boisseau, G Despesse, T Ricart, E Defay and A Sylvestre Published 31 August 2011 • IOP Publishing Ltd , Smart Materials and Structures, Volume 20, Number 10*

[30] G: input acceleration (1G= 9.81m/s^2)

[31] Cycle : 1 period of time defined by the given frequency

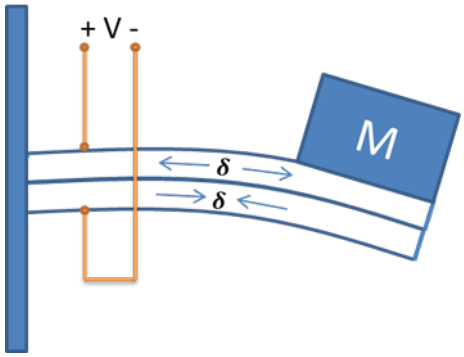
Among vibrational energy harvesters, the electrostatic transduction allows maximal miniaturization using MEMS technologies. Many proof of concept devices have been presented to the scientific community but no industrial devices have been commercialized yet.

c- Recommendations for concept 1 Mechanical EH: Electrostatic transduction

-For vibration based harvesting, enlarge the frequency bandwidth (>50Hz) around low frequency target (below 100Hz) is key to fit with applications.
-Develop dedicated power management circuits.
-Reliability of Material is the key to maintain the charges over 10 years.
-Flexible and low cost approaches for wearable (body) applications should be developed.

V.4.3.5.2. Concept 2: Mechanical EH: Piezoelectric transduction

Most piezoelectric harvesters are based in a resonating device made of a cantilever beam, covered by a piezoelectric material and an inertial mass attached (see Fig. below), this device is tuned to the characteristic mechanical vibration frequency of the application. As the cantilever is bent, strain is transferred to the piezo layer, which induces an asymmetric charge distribution, and therefore a voltage is generated. MEMS devices are very promising because their fabrication is CMOS compatible. Many companies exist actually exploiting this principle and integrating piezoelectric materials (mostly PZT, being toxic) on different substrates (metal foils, PCB…), very recently MEMS devices can be also found on the market by integrating AlN. Similar to the electrostatic concept, the main challenges rely on the increase of the resonance bandwidth, reduction of the working frequency to adapt to the applications, and increase of the energy generated per unit surface or volume.



Classical structure of a piezoelectric energy harvester[32]

a- Table of concept 2 Mechanical EH: Piezoelectric transduction

Concept 2 Mechanical EH: Piezoelectric transduction	Medium term: 5+	Long term: 10+
a) Key research questions or issues		
Improve efficiency with a reduced surface, volume	Develop packaging (Vacuum), integrate higher density seismic masses.	Small scale hybrid devices. Work on mechanical properties (fatigue strength,

[32] *Larcher, L., Roy, S., Mallick, D., Podder, P., de Vittorio, M., Todaro, T., Guido, F., Bertacchini, A., Hinchet, R., Keraudy, J. and Ardila, G. (2014) Vibrational Energy Harvesting, in Beyond-CMOS Nanodevices 1 (ed F. Balestra), John Wiley & Sons, Inc., Hoboken, NJ, USA. doi: 10.1002/9781118984772.ch6)*

		elasticity…)
Increase input bandwidth, reduce working frequency for portable applications, adaptable devices	Exploitation of non-linarites, frequency-up converting	Adaptable devices
Increase performance of piezoelectric materials	Porous materials	Nanotechnology, nanocomposites
b) Potential for application or Application needs and Impact for Europe		
Industrial / Infrastructures monitoring for security (autonomous sensors) - on vibrating sources	Harvesting on industrial machines	
Develop wireless autonomous monitoring in transportation (car, planes…)	Harvesting on railway, train	Harvesting on cars, planes
Develop Wearable systems for human movement harvesting	Shoes	Medical patches
c) Technology and design challenges		
Bio-compatibility	Piezo-electret, composites without lead	Nanotechnology, nanocomposites without lead
Low temperature integration, reduction of process temperature without affecting global performance	Composites, Piezo-electret	Nanotechnology, nanocomposites
d) Main FoMs		
MEMS devices (f<300Hz, G<0.5)		
FoM1: Volume power density (mW/cm^3)	1	1.5
FoM2: Surface power density (mW/cm^2)	0.15	0.2
Industrial devices: Piezoelectrics on flexible substrates (@50Hz, 0.5G)		
FoM3: Surface power density (mW/cm^2)	0.1	0.15
e) Other issues and challenges, and interaction with other Tasks/WPs.	…	…
Interaction with “heterogeneous integration”		
Interaction with “Equipment and materials”		

b- Competitive situation for concept 2 Mechanical EH: Piezoelectric transduction

Among vibrational energy harvesters, the piezoelectric transduction is one of the most exploited in research and at industrial level (MIDE and Piezo Systems in USA, PI, CEDRAT and ARVENI in Europe) thanks to its simple structure. It allows decent performance at small scales (~few cm^3 prototypes).

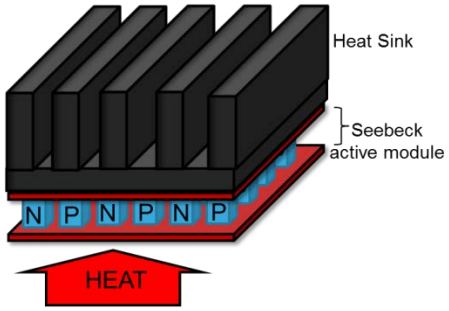
c- Recommendations for concept 2 Mechanical EH: Piezoelectric transduction

- New sustainable materials should be considered to avoid lead (Pb) based piezoelectric materials.
- Develop micro and nano piezo-composites could be a key to improve devices performance.
- Develop new concepts leading to performance and bandwidth improvement at low frequency (e.g. frequency-up converters, hybrid, adaptable devices, exploiting non-linearities…).
- Device miniaturization and/or integratability on flexible substrates would a key to fit wearables and IoT applications.
- Packaging is also a key to improve performance and reliability, in particular under vacuum.

V.4.3.5.3. Concept 3: Thermal energy harvesting

These devices convert thermal energy to electrical energy via the Seebeck effect. There are two main technologies: bulk technology and thin film technology. The bulk technology is adapted for applications (e.g. automotive, industrial applications, etc.) for which the size of thermoelectric (TE) devices is not a constraint (size vary from some cm² to some tens of cm²) and for which high power is required (W to kW range). The thin film technology is adapted for the confined environment, for which the size is a key point

(mm² to few cm²) and for which power from the µW to mW range is required. Most of the commercialized thin film TE devices are made of Bi_2Te_3 active materials (toxic/rare/expensive/not compatible with Si technologies). The main FoM is ZT, a dimensionless parameter defined by $ZT=\sigma S^2T/\lambda$, with σ the electrical conductivity, S the Seebeck coefficient, λ the thermal conductivity and T the temperature. For many years, Bi_2Te_3 has been the best TE material at room temperature with a ZT close to 1, and the objective would be to increase the ZT value up to 3.



Basic Seebeck thermo-generatorstructure schematic with heat sink[33]

a- Table of concept 3 Thermal energy harvesting

Concept 3 Thermal energy harvesting	Medium term: 5+	Long term: 10+
a) Key research questions or issues		
Improve efficiency of thermal to electricity transformation near room temperature (<400K)	ZT>2,5	ZT>3
Develop "green" solutions for near-room temperature use cases (<400K), not based on Bi_2Te_3	Nanostructured materials / SiGe based solutions	Nanostructured materials / Si based solutions
Develop scalable technologies at low cost	SiGe based solutions (bulk & thin films)	Si based solutions (thin films)
Reduce the size of the "bulky systems" integrated with heat sink	Thermal engineering at product level	High ZT material
b) Potential for application or Application needs and Impact for Europe		
Industrial monitoring for security (autonomous sensors)	Hvac, Hot pipelines, electrical installations	Hvac, Hot pipelines, pumps…
Infrastructure monitoring for security (autonomous sensors)	Pipe leaks, electrical lines	
Home automation for energy saving (autonomous sensors and heat systems monitoring)	Heating systems control, ETRV	Boiler tank, solar thermal monitoring
Develop wireless autonomous monitoring in transportation (car, planes…)	Sensors in cars (exhaust), trains	Sensors in cars (motor), planes
c) Technology and design challenges		
Develop new material for improved efficiency without Bi_2Te_3 near room temperature	Nano structured materials / SiGe based solutions	Phonon engineering / Si based solutions
Maintain the thermal gradient on thin devices / reduce size of heat sink: This can be addressed with ZT improvement, system architecture and heat sink engineering	ZT>2,5	ZT>3
Develop alternatives to Seebeck approaches	Phase change solutions (materials, liquids) or thermomechanics approaches	Alternative solutions at microscale
d) Definition of FoMs		
ZT	>2,5	>3

[33] *Puscasu, O., Monfray, S., Savelli, G., Maitre, C., Pemeant, J. P., Coronel & Guyomar, D. (2012, December). An innovative heat harvesting technology (HEATec) for above-Seebeck performance. In Electron Devices Meeting (IEDM), 2012 IEEE International (pp. 12-5). IEEE.*

Expected Output power vs available temperature difference on the TEG (mW/K²/cm²) in function of area (based on Tcold=300K)	>0,15mW/K²/cm²	>0,2mW/K²/cm²
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Power consumption of power management circuit in function of temperature.		
Increase reliability of integrated systems		
Develop low cost solutions / flexible materials		
Leakage of storage element at high temperature		

b- Competitive situation on the Thermal energy harvesting

All commercially available modules are based on Bi2Te3 material with a ZT value close to 1 (Laird Technology, Thermogen, Nextream, Microplelt…). The main challenge in the future would be to reach similar and above performances with less rare material (like Si-based materials).

c- Recommendations for the Thermal energy harvesting

-From material point of view, new sustainable materials should be considered to avoid Bi_2Te_3.
-Cost is a key point for energy harvesting: miniaturized solutions should focus on Si or SiGe material (nanostructured materials, phonon engineering) for compatibility with standard semi-conductor industries to reduce production costs.
-For non-miniaturized solutions, low cost and flexibles materials should be developed, with optimized thermal engineering at the product level to reduce the size of the heat sink.
-Improvement of ZT will allow heat sink size reduction
-New thermal energy approaches (non Seebeck) needs also to be developed (i.e. phase change of liquid, thermomechanical approaches, thermodynamic cycles…)

V.4.3.5.4. Concept 4: Photovoltaic Energy Harvesting

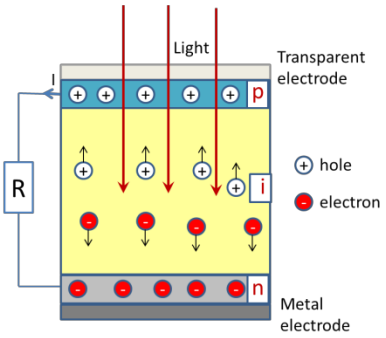
Photovoltaic (PV) effect consists in the absorption of light by the semiconductor, generation of electron-hole pairs and collection of charge carriers (thanks to the semiconductor device), allowing the generation of power (see Fig. below). the FoM usually used for solar cells working under sun light is the power conversion efficiency (output power density divided by incident sun power density of 1kW/m^2 (Solar spectra: AM1.5@25°C)). However, the output power density of the solar cell is depending on the incident light intensity, absorption and electronic properties of the material, spectral sensitivity of the solar cell to the light, electronic quality and properties of the semiconductor device. Therefore for solar cells working in indoor conditions, standard outdoor measurement conditions are not relevant because artificial modern light (fluorescent, LED) presents a different spectrum and far lower intensity compared to sunlight. For indoor light conditions, the parameter usually used is the output power density under specified artificial light intensity, but no standard measurement conditions are defined. The photovoltaic production is dominated by silicon based solar cells due to its abundance, well-known and mature technology thanks to microelectronic industry. Indeed most of the outdoor commercialized solar cells are made of crystalline silicon (c-Si) and for indoor applications amorphous Si (a-Si) solar cells are commercialized.
For outdoor solar cells, thin film cells (CdTe, CIGS, a-Si) are also commercialized, as well as high efficiency solar cells working under concentrated sun light[34,35,36,37].

[34] Technology Roadmap, Solar Photovoltaic Energy, IEA, 2014

[35] International Technology Roadmap for PV 2016

[36] Photovoltaic Report, Fraunhofer ISE, 2016

[37] Current Status of concentrator photovoltaic (CPV) technology, ISE, NREL, 2016



- A Si pin solar cell[38]

a- Table of concept 4 Photovoltaic Energy Harvesting

Concept 4 Photovoltaic Energy Harvesting	Medium term: 5+	Long term: 10+
a) Key research questions or issues		
Improve PV cell output power density for indoor applications	Organic, DSSC, Perovskite, semiconductors compounds (III-V, CdTe…), a-Si	Multi-junction PV cell, nanostructured materials…
Improve PV cell output power density for outdoor applications	Si solar cells, tandem cells on Si, semiconductors compounds (CdTe, CIGS…)	Multi-junctions, nanostructured materials, quantum dots…
Develop flexible, high power conversion efficiency and low cost PV cells	Thin-film PV cells (perovskite, organic, DSSC…)	Thin-Film, multi-junctions, nanostructured…
b) Potential for application or Application needs and Impact for Europe		
(Bottom-up) Autonomous systems : portable devices, IoT, health applications	Sensors, IoT, portable electronic devices, home automation, security systems…	IoT, health applications, factory automation, smart buildings…
c) Technology and design challenges		
Optimize the structure of the solar cell for Indoor and/or outdoor applications.		
Develop PV cells based on inorganic semiconductor compounds, DSSC (Dye sensitized solar cells), organic materials or perovskite with improved lifetime and stability. Increase the efficiency and reduce the cost of PV cells for energy harvesting applications.	Commercialized organic and inorganic (III-V compounds, DSSC…) for indoor and outdoor applications with improved efficiency and low cost	Low cost PV cells with increased efficiency (III-V compounds, multi-junction, nanostructured, thin film…)
d) Definition of FoMs		
Commercialized output power density (W/cm^2) under standard output sunlight conditions (AM1.5G, 1kW/m^2, 25°C)	>23mW/cm^2 (efficiency : 23%) for c-Si cells ; >18% CdTe or CIGS cells ; >13% a-Si, organic, DSSC	>25mW/cm^2 (efficiency : 25%) for c-Si cells ; >22% CdTe or CIGS cells ; >16% a-Si, organic, DSSC
Commercialized output power density (W/cm^2) and efficiency for indoor modern artificial light conditions (300lux, LED or fluorescent)	>20µW/cm^2	>25µW/cm^2
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Interaction with “heterogeneous integration”		
Interaction with “Equipment and materials”		
Decrease the consumption of associated management circuits		

[38] http://panasonic.co.jp/es/pesam/en/products/pdf/Catalog_Amorton_ENG.pdf

b- Competitive situation for concept 4 Photovoltaic Energy Harvesting

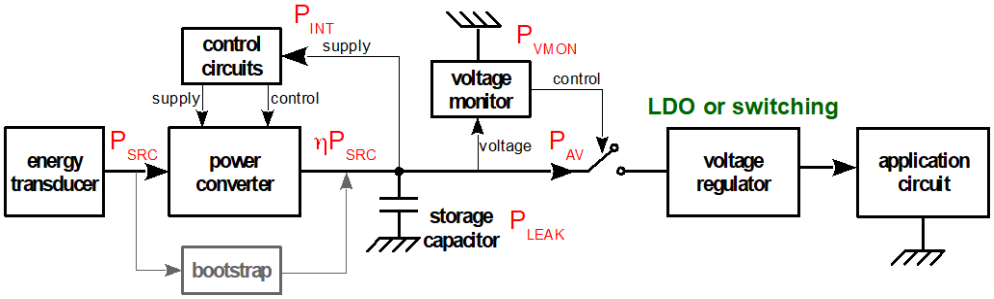
If light is available for a given autonomous application, the photovoltaic principle is the best choice among all the harvesting technologies (especially in outdoor conditions) providing the highest electrical power density. Silicon technology is very mature for these outdoor conditions (Jinko Solar, Canadian Solar, Hanwha Q-cells, Sunpower…) but also for indoor (Panasonic, Schott Solar…).

c- Recommendations for concept 4 Photovoltaic Energy Harvesting

- Define standard procedures for indoor photovoltaic cells characterization (light intensity and spectra, direct and diffuse light, temperature…).
- Design and optimize structures for outdoor or/and indoor light and for different type of application: sensitivity to different light sources (sun, artificial light, diffuse and/or direct light), flexibility if necessary, cost, output power, material abundance (especially for mass production such as outdoor applications).
- a-Si is the most used material for indoor energy harvesting and c-Si for outdoor photovoltaic. However other materials and structures (organic, perovskite, dye, III-V compounds, nanostructured materials, multijunction…) present interesting potential for energy harvesting providing flexibility, high output power, etc. For those materials it is recommended to decrease the cost (for III-V compounds, multijunction, nanostructured), increase lifetime and/or stability (organic, perovskite, dye) and efficiency (organic, dye…).

V.4.3.5.5. Concept 5: Micro-Power Management (PM)

In order to take advantage from energy transducers, it is essential to develop electronic circuits for converting power, storing energy, and distributing it to application circuits efficiently, consuming less than the available input power. The design must tackle several trade-offs in achieving: (i) the PM circuits bias the source in its maximum power point (MPP); (ii) High efficiency in power conversion; (iii) the lowest intrinsic power consumption.
The most important FoM, which determine the low operating boundaries, are the intrinsic power consumption and the minimum input voltage, either during steady-state operation or during a cold start-up. Other FoMs include efficiency, and the surface area of the whole converter circuit.
. Commercial discrete components allow cost-effective solutions with intrinsic consumptions down to 1 µA and input voltages down to few tens of mV[39,40]. CMOS implementations go further and achieve from hundreds nW[41] down to few nW[42].



Block diagram of a battery-less power conversion and management system including a duty-cycled load.
Ref: *A. Romani et al., IEEE Computer 2017*

[39] S. Boisseau, P. Gasnier, M. Gallardo, G. Despesse, Self-starting power management circuits for piezoelectric and electret-based electrostatic mechanical energy harvesters, in: J. Phys. Conf. Ser., IOP Publishing, 2013: p. 012080. doi:10.1088/1742-6596/476/1/012080.

[40] A. Camarda, A. Romani, E. Macrelli, and M. Tartagni, "A 32 mV/69 mV input voltage booster based on a piezoelectric transformer for energy harvesting applications," Sensors Actuators A Phys., vol. 232, pp. 341–352, May 2015.

[41] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A Nano-Current Power Management IC for Low Voltage Energy Harvesting," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4292–4304, 2015.

[42] W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, and D. Blaauw, "A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 398–399.

a- Table of concept 5 Micro-Power Management (PM)

Concept 5 Micro-Power Management	Medium term: 5+	Long term: 10+
a) Key research questions or issues		
Achieve operation with ultra-low input voltage and power levels (minimization of self-consumption and trade-offs with efficiency)	Power conversion/management ICs operating with < 1 µW and starting with 50-100 mV	Integrated SoC or SiP embedding power conversion/management and their specific functions operating in the 10-100 nW range
Perform battery-less start-up from fully discharged state	Fully integrated step-up converters based on low-VTH/native MOSFETs down to 50 mV. Integrated step-up converters aided by external magnetic or piezoelectric transformers down to few mV	Miniature systems with embedded micro-transformers (magnetic or piezoelectric) at package level starting from few mV
Are external passive required (C, L) or can the circuit be fully integrated? Overall size.	More efficient fully integrated inductor-less switched-capacitor converters Miniaturization of magnetic components	Development of alternatives of inductors for power conversion compatible with wafer-level processing, such as MEMS piezoelectric transformers Nanopower SoC and miniature passive + energy transducer integrated at package level (mm-scale systems)
Type of maximum power point tracking and/or source impedance matching provided	FOCV or derived techniques for DC sources with more responsive MPPT. Cancellation of reactive components of source impedance in vibrational energy harvesters	More complex MPPT algorithms implemented on-chip with ultra-low consumption
Reduce the power consumption of power management circuit	<1µW / 70% efficiency	<100nW / 80% efficiency
b) Potential for application or Application needs and Impact for Europe	…	…
Wearable electronics	Body sensors for sport or for worksuits	Smart clothes/textiles
Implantable electronics / biomedical devices	Basic wearable monitoring of physiological parameters (temperature, ECG, motion, etc.)	Implantable chips for monitoring physiological/biochemical parameters, or for being embedded in smart prosthesis
Environmental monitoring	Miniature energy autonomous nodes powered by multiple sources	More efficient implementations
Industrial applications (smart machinery parts)	Smart machinery parts (e.g. rotating)	More efficient implementations
Automotive	On-board and on-engine wireless sensor networks	More efficient implementations
Logistics and tracking goods	Smarter UHF RFID tags with enhanced functions, such as localization, sensing, datalogging, on multiple chips and components.	Single-chip cost-effective RFID-like tags
c) Technology and design challenges		
Power management distributed at many levels	Development of energy-aware circuit design techniques for power converters in the 1-100 nA range	Energy-aware design of all system parts with reduced leakage, lower active currents, and harmonized energy

		management policies
Development of dedicated microelectronic process options and devices	Improved availability of low-threshold/native/depletion MOSFETs for supporting energy harvesting from ultra-low voltage sources (tens of mV) Improved power switch performance (lower driving voltage, lower leakage, lower on-resistance)	Development of more efficient power switches with low control voltage and negligible leakage (microelectronic, or micromechanical alternatives)
System integration and smart packaging	cm-scale energy autonomous systems	mm-scale energy autonomous systems
Accept high input voltages on microelectronic implementations	Implementations on BCD or CMOS-HV processes	
d) Definition of FoMs		
Minimum 'steady-state' allowed input voltage and power	< 50 mV, < 1 µW	< 10 mV, < 100 nW
Minimum input voltage and power for cold-start-up	< 100 mV, 1 µW	< 10 mV, < 100 nW
Minimum Conversion efficiency	70%	80%
Maximum input voltage allowed	20 V	10 V

b- Competitive situation for concept 5 Micro-Power Management (PM)

Power management circuits are essential to autonomous systems. , and CMOS implementations have demonstrated dramatic reduction of the accepted input power and voltages. Major silicon foundries have proposed in the last years dedicated products operating down to few µW and few hundreds mV, along with very tiny implementations requiring few components. (STMicroelectronics, Texas Instruments, Analog Devices, Linear Technology, etc.)

c- Recommendations on concept 5 Micro-Power Management (PM)

- Refinement of energy-aware nano-power design techniques for micro-power management circuits, in order to define adequate trade-offs between intrinsic power consumption, efficiency and performance.
- Power-constrained re-design of WSN circuits is recommended. This is key for application compatibility and to further reduction in intrinsic power of converters
- In order to devise mm-scale autonomous systems and dramatic reductions in system size, the recommendations include: Investigate size reduction of inductors; enhancement of efficiency of inductor-less power converter circuit topologies; develop planar alternative to inductors which can be integrated at wafer-level (e.g. MEMS piezoelectric transformers)
- Tune microelectronic process parameters to reduce leakage and to allow lower activation voltages, improve the quality of the switches including also the exploration of low-voltage electromechanical switches.

V. 4.3.6 Synergies with other topics (WP topics, if applicable)

Materials and equipment (Task 6.1)

All the energy harvesting concepts covered so far use specific materials (piezoelectric, composites, thermoelectric, semiconductors…), their constraints will depend on the application (low temperature, integration into flexible substrates…) and thus will require different fabrication techniques/equipment.

Heterogeneous integration (task 5.2)

The integration and packaging of the different components of an autonomous device (sensors, power management systems, energy storage, energy harvesters, antennas…) need to be considered as a function of the final application (wearables, IoT…).

Smart sensors (sub-task 4.1)
The development of low power sensing is compatible with energy harvesting technologies to build self-powered sensors.

V. 4.3.7 Recommendations (of the WP topic)

In general, the development of applications is the key to success for EH. IoT and energy harvesting are application-driven today, so projects should mainly focus on the development of a complete application (from harvesting to the use case). Concerning the concepts covered so far in this mid-term roadmap (vibrational, solar, thermal EH and power management), the improvement of their performance and efficiency is as important as the development of "green" materials, replacing toxic/rare materials used nowadays (lead based piezoelectrics, Bi2Te3 for thermoelectrics). The use of nanotechnologies is foreseen to increase the performance of all the concepts in general. Flexible and low cost approaches for wearable applications should be developed as well. Increasing the bandwidth at a low frequency target (below 100Hz) will help to fit applications for vibration based mechanical energy harvesters. Concerning indoor photovoltaic applications, adapted structures and materials (light intensity and spectra…) should be developed. Concerning power management circuits, it would be key to investigate size reduction of inductors, to enhance the efficiency of inductor-less power converter circuit topologies, to develop planar alternative to inductors and to tune microelectronic process parameters and technologies to reduce leakage for reduced power consumption and allowing low input voltages.

V. 5 System Design and Heterogeneous Integration (WP5)

V. 5.1 System Design and Heterogeneous Integration (WP5 T5.1 and T5.2)

V. 5.1.1 Executive summary

Building a roadmap for System Design and Heterogeneous Integration is a tough challenge, because of the variety of applications involved, demanding for very different requirements, sometimes even contrasting in terms of values, limits and importance. Several roadmapping attempts have been done in the past. The first example is the 2007 revision of ITRS[43] where some quantitative Figures of Merit (FoM) were given in terms of percentage of improvement over standards or targets. In the following ITRS revisions of 2009[44] and 2011[45], quantitative FoMs have been replaced by bar charts, related to the topic's development status with respect to the time horizon.
It is therefore justified to consider a new approach for roadmapping System Design and System Level Applications, which goes beyond the simple inclusion of static numerical tables. The NEREID approach is to build a general *Top-Down* description of the requirements (a hierarchical map) that has to be met in a *Bottom-Up* process, with concepts, methods, values and expectations strictly related to the application of reference.
In this first version of the roadmap chapter on System Design and Heterogeneous Integration, concepts are split in the two parts of the headline (System Design and Heterogeneous Integration) allowing a better

[43] International Technology Roadmap for Semiconductors, Design, 2007 Edition
[44] International Technology Roadmap for Semiconductors, Design, 2009 Edition
[45] International Technology Roadmap for Semiconductors, Design, 2011 Edition

initial orientation, improved focusing opportunities and effectiveness in deciding. However, the final goal is to generate a unique Roadmap in the second version (that will be released next year), merging the different contributions.

V. 5.1.2 Relevance and competitive value

Relevance of System Design and Heterogeneous Integration

System design and heterogeneous integration are core facilities that will enable to overcome the design challenges due to the ever increasing complexity of embedded systems, which require to design System on Chips (with integration of digital and analog functions) and systems of SoC. Accordingly every application expert emphasized the importance of system design and heterogeneous integration during all discussions on the different NEREID Workshops.

Competitive value

With respect to other continents, Europe can rely on a huge and original knowledge on system level applications and in More than Moore technologies. Smart Systems are strategic assets present in Europe and so European companies can play a leadership role in the related worldwide market.

It is not only the technologies in Europe that are present, as a result of the ingenuity of a number of device and systems manufacturing companies, the design capabilities at system level are also very important. The strong presence of systems in the European industrial and commercial scenario is also confirmed by the fact that international roadmaps (as for example IRDS) are very much less concentrated on systems. This is mainly due to the fact that American and Asian markets are more focused on other technological aspects where they have market advantages.

All of this highlights the importance of Europe working on a systems level roadmap and for European manufacturers and academics to invest resources into pushing this European leadership in Smart Systems and system level knowledge.

Social Benefit

As mentioned in the previous section, the strength of systems manufacturing and design in Europe is a reality, bringing the possibility to increase the presence of European companies in this field, with a direct impact on the availability of well-paid professional employment jobs across the European community. The value of creating the need of high level competences, related to conception and design of systems, both in system design and at physical level for conceiving innovative solutions in heterogeneous integration, has a very much larger value than to invest in basic knowledge for device production.

In systems, knowledge is the key, because the problems and the scenarios relating to where systems are to be applied are very different and as systems require strong competences in all the different levels of system design and integration. Nowadays heterogeneous integration is playing a fundamental role in productivity and environmental monitoring as well as in health and automotive applications and it is important for Europe to invest in education and system design capabilities. This will provide European workers with the opportunity to become the reference for these aspects on a global scale.

V. 5.1.3 Vision of System Design and Heterogeneous Integration

The approach for the roadmap on System Design and Heterogeneous Integration is to proceed in two steps:

1. A Hierarchical Tree Map has been created using a *Top-Down* approach. In this map the various concepts have been identified along with the related keys of the roadmap and these have been mapped using a hierarchical structure;

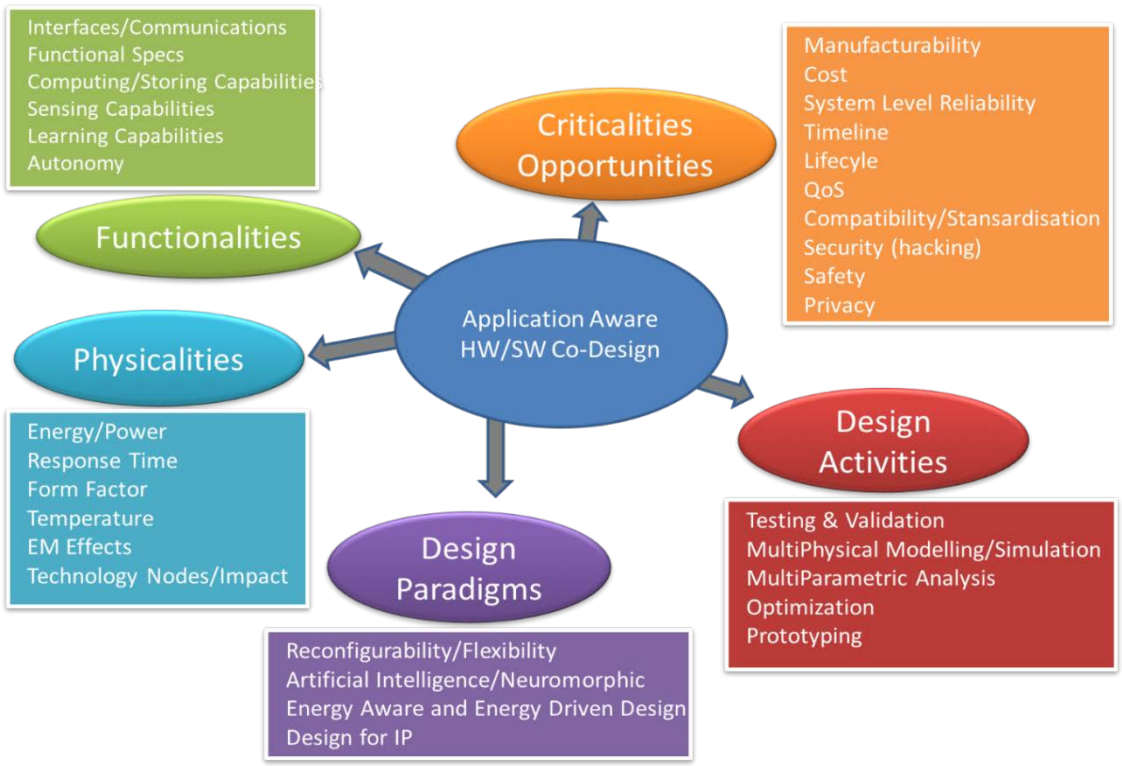
2. A *Bottom-Up* process is then needed to populate the map with content as a first step. This process starts with the requirement to identify a specific application domain, and this drives the agenda and provides a context for the information requests confines them and ensures that they are application-driven.

In the first instance, the two high level applications Automotive and Biomedical Devices (and everything that goes into building them) have been identified as reference domains. These were chosen because of their relevance for Europe and as they reflect different and complementary application challenges. For example, if a system is for automotive it can have access to some form of bulky replaceable battery, if it is for an implantable device, the power supply would needs to be small, biocompatible and would ideally never need to be replaced.

It is also clear that in any case, even these domains are too large to provide a coherent roadmap because even inside these domains there are dramatically conflicting technology requirements. With that in mind roadmaps will be produced for Autonomous Driving and Implantable Devices, because these are subsets which represent different application challenges. These roadmaps will be populated using application-driven bottom-up approaches aligning the map with the general constraints associated with each application sub domain.

V. 5.1.4 Scope and ambition of System Design and Heterogeneous Integration

The first version of the *Top-Down Map* is reported in the depicted scheme below. This is the result of the work done inside the NEREID project, where the requirements from different application domains were shared by experts in their respective fields.



The map starts from the central concept that a system must be aware first of the application and that the HW/SW Co-Design must nowadays play a key role in system design. From the specific application, five "concepts" were derived:

1. Functionalities, the aspects that cover a system's functions ;

2. "Physicalities", the aspects related to performances and characteristics at physical level;
3. Criticalities/Opportunities[46], the aspects that define risks and threats;
4. Design Paradigms, the aspects that need to be considered for modalities of design and integration;
5. Design Activities, the aspects that need to be considered for design and integration itself.

For each of these concepts the research Keys, individuated in the roadmap exercise inside NEREID, will be detailed. Research "Keys" in NEREID Roadmap are the key questions or issues related to the concept that is developed in the roadmap table.

For some cases the acronym **A.D.** is used in the tables of the concepts indicating that something is *Application Dependent*. This acronym will be used for the parameters/keys that are to be considered in the roadmap, but cannot be considered general in terms of values. These will be formalized in the second version of the roadmap, when the specific application domain is chosen and mapped in the Bottom-Up roadmap population process.

V. 5.1.5 Main Concepts of System Design and Heterogeneous Integration

V.5.1.5.1. Concept 1: System Design Concepts

a- Table of concept 1: Functionalities

In this table are reported the most important functionalities to be considered in the System, considering its internal and external interactions.

Concept 1: Functionalities	Medium term: 5+	Long term: 10+
i) Functionalities		
a) Key research questions or issues		
• Functional Specs • Interfaces/Communications • Computing/Storing Capabilities • Sensing Capabilities • Learning Capabilities • Autonomy • Speed		
b) Potential for application or Application needs and Impact for Europe	+++	+++
c) Technology and design challenges		
Functional Specs		
- What to Measure	A.D.	A.D.
- What to Calculate	A.D.	A.D.
- How Well	A.D.	A.D.
- Reusability	+++	+++
- Assembly for automation	+++	+++
- System Synthesis	++	+++
- What to Verify	+++	+++
- Cross Domain Specification	A.D.	A.D.
Interfaces/Communications		
- Hardware	++	++
- Software	+++	+++
- External	A.D.	A.D.

[46] These are together because a criticality it becomes an opportunity too, when the solution to it is found.

- Internal	A.D.	A.D.
- Bio-Interfaces	A.D.	A.D.
Computing/Storing Capabilities	A.D.	A.D.
Sensing Capabilities		
- Sensor Fusion	+++	+++
- Accuracy	A.D.	A.D.
- Precision	A.D.	A.D.
Learning Capabilities	++	+++
Autonomy		
- Functional Autonomy	A.D.	A.D.
- Power Autonomy	A.D.	A.D.
Speed		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
To be filled when the Bottom-Up process is implemented, applying the specific request of the Application Domain	A.D.	A.D.
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Beyond CMOS, WP2	++	+++
Advanced Logic and Connectivity, WP 3	+++	+++
Functional Diversification, WP4	+++	+++
Heterogeneous Integration, Task 5.2	+++	+++

A.D. = Application Dependent

b- Competitive situation of concept 1 Functionalities

Europe is well positioned in the global market for what concerns the innovation in System functionalities.

c- Recommendations for concept 1 Functionalities

- *The value is not in the Device itself, but in System Integration and in the related Data*, the Information is at Systemic Level
- The future is to move *from Embedded Computing to Embedded Intelligence*
- *Re-Usability and Reconfigurability* are key issues for new Systems
- *Software-like re-programmability* with (almost) hardware like efficiency is a solution that must be considered and nowadays in Europe companies such as ARM can become a reference

V.5.1.5.2. Concept 2: "Physicalities"

Physicalities are the aspects related to performances and characteristics at Physical level. This concept has a strong link with Heterogeneous Integration.

a- Table of concept 2 Physicalities

Concept 2 Physicalities	Medium term: 5+	Long term: 10+
ii) Physicalities		
a) Key research questions or issues		
• Energy/Power • Response Time • Form Factor • Environment • Temperature		

• Electro-Magnetic Effects • Technology Nodes/Impact on Technology • Robustness		
b) Potential for application or Application needs and Impact for Europe	+++	+++
c) Technology and design challenges		
Energy/Power		
- Profile of Energy Sources	A.D.	A.D.
- Energy Transparency (requested energy)	A.D.	A.D.
- Low Consumption	A.D.	A.D.
- Energy-driven Design	+++	+++
Response Time	A.D.	A.D.
Form Factor		
- Size	A.D.	A.D.
- Weight	A.D.	A.D.
- Footprint	A.D.	A.D.
- Dimensionality	A.D.	A.D.
Environment		
- Environment-aware Design	++	+++
Temperature	A.D.	A.D.
Electro-Magnetic Effects	A.D.	A.D.
Technology Nodes/Impact on Technology	+++	+++
Robustness	+++	+++
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
To be filled when the Bottom-Up process is implemented, applying the specific request of the Application Domain	A.D.	A.D.
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Heterogeneous Integration, Task 5.2	+++	+++

A.D. = Application Dependent

b- Competitive situation of concept 2 Physicalities

For what concerns the physical realisation of a device and a system, Europe can be considered strong in the design and production of systems, but the leadership of the fabrication at device level is in general stronger outside Europe, and cooperation with American and Asian makers is a must.
In Europe are present very important competences in Power devices and Sensors, where European companies are leading the market, and so moving to the direction of System Integration is a natural step forward, increasing competitiveness of Europe.

c- Recommendations of concept 2 Physicalities

- *Balance of how much happens at each node and the energy for transmission* (for reliability/security reasons too)
- For Energy the key issues are:
  - *Management*
  - To Consume *when and where is necessary only*
  - Importance of *categorizing the application in terms of Energy Boundaries*
- *Environment* is part of the System

V.5.1.5.3. Concept 3: Criticalities & Opportunities

In this concept, Criticalities and Opportunities are together because a Criticality becomes an Opportunity too, when the solution to it is found. The Keys are at different levels and the impact it is from physical to system architecture.

a- Table of concept 3 Criticalities & Opportunities

	Medium term: 5+	Long term: 10+
iii) Criticalities & Opportunities		
a) Key research questions or issues		
• Manufacturability • Cost • System Level Reliability • Timeline • Lifecyle • QoS • Compatibility/Standardisation • Security (hacking) • Privacy • Safety • Designer Education		
b) Potential for application or Application needs and Impact for Europe	+++	+++
c) Technology and design challenges		
Manufacturability		
- Technical (investing in technical manufacturability)	+	+
- Cost	+++	+++
- Material Availability	A.D.	A.D.
- Low Volume Production	A.D.	A.D.
- Process variations impact and related design choices	++	+++
Lifecyle		
- Duration	A.D.	A.D.
- Recycling	+++	+++
Security (hacking)		
- Trusted Executing Environment	++	+++
- Design for Security	+++	+++
Cost		
- Full System Verification	+++	+++
- Full System metrics settings	+++	+++
- System Coverage, scenario definition	+++	+++
- Cross Domain Simulation	++	+++
- Coverage across domains	++	+++
System Level Reliability	+++	+++
Timeline		
- Design Timeline	A.D.	A.D.
- Product Timeline / Time to Market	A.D.	A.D.
- Cross-learning among project by Machine Learning	A.D.	A.D.
- New engines between Chip Level and System Level models for Design speedup	A.D.	A.D.
- Return of Investment (ROI)	+++	+++
Quality of Service (QoS)	A.D.	A.D.
Compatibility/Standardisation		

- Standard-aware Design	A.D.	A.D.
- Environment Compatibility	+++	+++
- Conformity to Regulations	+++	+++
Privacy	+++	+++
Safety	+++	+++
Designer Education	+++	+++
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
To be filled when the Bottom-Up process is implemented, applying the specific request of the Application Domain	A.D.	A.D.
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Advanced Logic and Connectivity, WP 3		
Functional Diversification, WP4	+++	+++
Heterogeneous Integration, Task 5.2	+++	+++
Equipment and Manufacturing, WP6	+++	+++

A.D. = Application Dependent

b- Competitive situation of concept 3 Criticalities & Opportunities

As already previously discussed, are valid the comments given for Functionalities, indicating for Europe an important opportunity to invest for continuing its leadership in Systems.

c- Recommendations for concept 3 Criticalities & Opportunities

- To develop *novel Design Tools* for reducing the Time to Market of products and increase ROI
- To stop regarding Systems as Connected Devices, but to consider them to be as *Distributed Embedded Systems* (System of Systems)

V.5.1.5.4. Concept 4: Design Paradigms

In this table, the roadmap covers the design paradigms that are considered of importance for system design.

a- Table of concept 4 Design Paradigms

	Medium term: 5+	Long term: 10+
iv) Design Paradigms		
a) Key research questions or issues		
• Hardware/Software Co-Design • Reconfigurability/Flexibility • New Paradigms • Energy Aware and Energy Driven Design • Design for IP • Open Source / Open Cores • Automated Design		
b) Potential for application or Application needs and Impact for Europe	+++	+++
c) Technology and design challenges		
HW/SW Co-Design		
- Power-Compute Co-Design	+++	+++
- Energy-Compute Co-Design	+++	+++
- Power/Energy-Quality Co-Design	+++	+++
Reconfigurability/Flexibility		

- Hardware	+++	++
- On Site Reconfigurability (Critical? Safe?)	++	+++
- Closed-loop Adaptation	++	+++
New Paradigms		
- Artificial Intelligence	A.D.	A.D.
- Neuromorphic Computing	A.D.	A.D.
- Bio-Inspired (from energy-driven to survival-driven)	A.D.	A.D.
Energy Aware and Energy Driven Design		
- Energy strategies for intelligent distribution of consumption in the different nodes/components/subsystems	A.D.	A.D.
- On-request Energy consumption	+++	+++
Design for IP		
- System IPs	++	+++
Open Source / Open Cores		
- Open IPs	+	+
- For Connectivity	+++	+++
Automated Design		
- Automated Design Space Exploration	++	+++
- Automated Design Decisions (architectural, safety, timing)	++	+++
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
To be filled when the Bottom-Up process is implemented, applying the specific request of the Application Domain	A.D.	A.D.
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Beyond CMOS, WP2	+++	+++
Advanced Logic and Connectivity, WP 3	+++	+++

A.D. = Application Dependent

b- Competitive situation of concept 4 Design Paradigms

In System Design the market is in this moment open. In fact several new technologies and solutions are appearing (some will be successful, some not) that are raising a sure request of new design paradigms. New paradigms as Artificial Intelligence, Neuromorphic Computing or Bio-Inspired Architectures are already present and request an effort in developing new tools for System Design.
European tool developers are now not so strong as US CAD tool companies as Cadence, Synopsys, Mentor, but the openness of the new approaches can be a perfect moment in which to invest for increasing competiveness of Europe in this field.
EDA initiatives and companies (as for example MunEDA) are present in Europe, but small and focused on specific topics. Opening European competences in the development of System Level tools could bring new opportunities of European CAD vendors, differentiating them from the big players and taking benefit of the neighbourhood with key companies in System Level devices as Bosch, Siemens, ST Microelectronics, or MEMS producers as Tronics, Sensonor and ST Microelectronics again.

c- Recommendations for concept 4 Design Paradigms

- *Add Software in the middle*, starting from the Application
- Definition of *Standards for Interoperabilty*, but Openess of standard cannot prevent monetisation
- Give to the Designer efficient tools for:
    - Automated *Design Space Exploration*
    - Automated *Design Decisions* (for networking choices too)

V.5.1.5.5. Concept 5: Design Activities

The design activities cover the different levels of the System, from modelling, to analysis, up to verification and validation. The table reports the important keys that must be considered in System Design and their importance for the future.

a- Table of concept 5 Design Activities

	Medium term: 5+	Long term: 10+
v) Design Activities		
a) Key research questions or issues		
• Verification • Testing & Validation • MultiPhysical Domain Modelling and Simulation • MultiParametric Analysis • Optimization • Prototyping • Constraints aware design • Design for Maintenance • Network Synthesis		
b) Potential for application or Application needs and Impact for Europe	+++	+++
c) Technology and design challenges		
Verification		
- IP Verification	+++	+++
- System on Chip (SoC) Verification	A.D.	A.D.
- Software bring-up	++	+++
- Cost of Verification	+++	+++
- New verification methods for Machine Learning Systems (how to verify them?)	++	+++
- Network Verification Tools	+++	+++
Testing & Validation		
- For mixed signals and different physical domains	+++	+++
- For Manufacturing		
Device Level	A.D.	A.D.
Process Level	A.D.	A.D.
- For Functionality		
Reliability	+++	+++
Safety	+++	+++
Privacy	+++	+++
Security	+++	+++
MultiPhysical Domain Modelling and Simulation	A.D.	A.D.
MultiParametric Analysis	+++	+++
Optimization		
- Performance/Power Balancing and allocation (where to do what)	+++	+++
- Energy for Transmission	+++	+++
Prototyping		
- 3D Printing	A.D.	A.D.
- Virtual Reality for Demonstration	A.D.	A.D.
Constraints aware design		
- Constraint Propagation	+++	+++
- Embedded Real Time constraints hard/soft	+++	+++
- Constraints for Systems of Systems	++	+++
Design for Maintenance		

- Design for Maintainability/Serviceability	+++	+++
- Virtual Reality	+	+++
Network Synthesis	+	+++
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
To be filled when the Bottom-Up process is implemented, applying the specific request of the Application Domain	A.D.	A.D.
e) Other issues and challenges, and interaction with other Tasks/WPs.	…	…
Advanced Logic and Connectivity, WP 3	+++	+++
Functional Diversification, WP4	+++	+++
Heterogeneous Integration, Task 5.2	+++	+++
Equipment and Manufacturing, WP6	+++	+++

A.D. = Application Dependent

b- Competitive situation of Design Activities

The capability of an efficient System Design is an asset of European companies, so has to be maintained and continuously updated with efficient actions in education and internal training of designers.

c- Recommendations for Design Activities

- Validation: here needs to be a statement of the level of robustness that is acceptable, this will provide Confidence as to *when the verification has been completed. If this is not done validation will continue until all of the time is used up?*
- *Where to position the intelligence needs to be decided, is it in the node or in the cloud?*
- *Continuous Training on System Design is essential if* for European academia and industry are to keep pace with innovations in the area.

V. 5.2 Heterogeneous Integration Concepts

V.5.1.5.6. Concept 6: Energy Autonomy

5.1 a- Table of concept 6: Energy Autonomy

	Medium term: 5+	Long term: 10+
Energy Autonomy		
a) Key research questions or issues		
• Low-power electronics • Long-lifetime storage and energy harvesting capability for systems providing mobility, portability, wearable use, off-grid, real-time local analysis		
b) Potential for application or Application needs and Impact for Europe		
From "smart-++" (++ for cities, building, transport…) to "benevolent-++" Societal needs not only so-called "silver domain", but also all groups of people with special needs Medical monitoring and "patients-at-home" are huge markets Food, water and agriculture at large Water quality, water treatment, water re-treatment		
c) Technology and design challenges		
How to close the gap between energy generated/stored and the energy needed to implement application specs • Low-power architectures and power management • Battery integration (e.g. as function of system volume, form factor conformity, discharge properties)		

• Energy harvesting (e.g. for eternal off-grid devices) • Power-efficient algorithms (see sensor fusion) Flexible solutions needed for wearables and thin, large area electronics		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• energy consumed & dissipated per duty cycle (for constant volume) • power management end-to-end efficiency • energy (power) density of storage device • energy generated per duty cycle (for constant volume) • leakage current of storage device • series resistance of storage device • forward voltage (diodes)[47] • compatibility with system on flex • new materials for energy harvesting • solid state storage	+++ Typical >90% >10Wh/kg(10^5 W/kg) +++ <0.1mA <10mOhm < 0.5V ++ +++ +++	+++ Typical >95% > 30Wh/kg(10^6 W/kg) +++ <0.001mA <1mOhm < 0.3V +++ ++ +++
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Task 4.2 on Smart Energy		

b- Competitive situation for concept 6 Energy Autonomy

This is an opportunity for Europe to maintain a leading role in enabling energy autonomy for heterogeneous integrated systems for applications smart environments and citizen-centric services. European companies are offering state-of-the-art solutions whereas European research advances the fields of energy harvesting from ambient sources and long-lifetime portable storage. Considerable expertise also exists in low-power circuits and power electronics.

c- Recommendations for concept 6 Energy Autonomy

For energy autonomy of miniaturised autonomous smart objects the fundamental limits of energy harvesters, managing hybrid energy harvesting and integrating novel energy storage with high-energy density and high-power capability is essential. It is also necessary to apply a holistic approach from device to circuit to architectures as necessary for application specific implementations, aiming at the limits of energy consumption for each layer and as a whole. In this context, new computing paradigms could be explored so that energy consumption is pushed below pJ per operation.

V.5.1.5.7 Concept 7: Connectivity

a- Table of concept 7: Connectivity

	Medium term: 5+	Long term: 10+
Connectivity		
a) Key research questions or issues		
To enable low-power connectivity (WiFi, LiFi, Bluetooth etc.) in small form factor systems and high-data rate applications		
b) Potential for application or Application needs and Impact for Europe		
• Welfare, first-responders		

[47] Need to revisit FoM based on discussion at http://www.power-mag.com/pdf/feature_pdf/1418657695_OnSemi_Feature_Layout_1.pdf

• Healthcare • IoT for cars • Industry 4.0		
c) Technology and design challenges		
• RF-enabled devices need logic dies for BLE or NFC, how to make these low cost and power efficient • Antennas for low power consumption, new designs/materials will be needed • Antennas for massive multiple frequencies, and multiple antennas (M-MIMO)		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• Increase antenna performance per area • Antenna area reduction (based on performance and frequency increase) • New materials for antennas (e.g. CNTs, graphene) • New materials for low-loss substrates integrating high-conductivity metal interconnects (e.g., PZT, AlN, porous Si) • New designs (e.g. fractal) and modelling tools	10% x 0.5 +++ ++ +++	20% x 0.1 +++ +++ ++
e) Other issues and challenges, and interaction with other Tasks/WPs.	…	…
WP3 How to exploit optically based communication (LiFi) WP3 Connectivity between devices that are off-line WP3 APIs open to third parties, interoperable APIs		

b- Competitive situation of concept 7: Connectivity

Several European policies have been promoting increased connectivity including 5G wireless technology, WiFi access to citizens (WiFi4EU). This has huge implications in the European market, hence, both industry actors and the research community have been mobilised to provide the necessary solutions. Similar to the developments of standards, European research on RF-enabled devices and antennas is strong with many regional pockets of excellence, however, the community is still fragmented.

c- Recommendations for concept 7: Connectivity

New applications will continue to drive the increase of global mobile data and hardware has to adapt to the challenges of increased performance and miniaturisation and to this end a critical mass for integrating (low-power) connectivity in small form factor systems needs to be created. However, connectivity also relates critically with the concept of energy autonomy as communication is widely accepted to be the primary consumer of energy. Whatever advances are made in hardware and communication protocols, energy efficiency in connectivity has to be a primary objective.

V.5.1.5.8 Concept 8: Sensor Integration

a- Table of concept 8: Sensor Integration

	Medium term: 5+	Long term: 10+
Sensor Fusion		
a) Key research questions or issues		
To enable adaptive intelligent data acquisition systems through (low-power) multi-parameter sensing originating from diverse stimuli: optical, fluidic, mechanical, thermal, magnetic, inertia, chemical, radiation		
b) Potential for application or Application needs and Impact for Europe		

Sensor Fusion is already a main innovation driver in automotive and Industry 4.0 and is an enabling technology in medical devices, healthcare and smart cities applications. In the Built Environment, civil engineers have been able to monitor in real-time, structures such as buildings, bridges and tunnels all the way through their lifecycle, from the construction phase to the operational phase through the provision of real-time multi-parameter data sets for the first time. In the field of environmental monitoring, the temporal granularity of the multi-modal sensor datasets provided has enabled exploring the characteristics of the "environmental nervous system" incl. tackling climate change.		
c) Technology and design challenges		
Cooperation and complementarity between sensors Redundancy Adaptation to the environment; for example, interference in the built environment, particularly in industrial applications, can be an issue due to noise and the crowded EM spectrum		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	…	…
• Latency • Bandwidth • Calibration procedure • Functional partitioning • Power efficient algorithms • AI, machine learning	Application dependent +++ +++ +++ +++	Application dependent ++ ++ +++ +++
e) Other issues and challenges, and interaction with other Tasks/WPs.	…	…
Task 4.1 on Smart Sensors		

b- Competitive situation for concept 8 Sensor Integration

Sensor Fusion software platforms are offered by all major European companies offering smart electronics components. Opportunities exist at both system and network level (Distributed Embedded Systems, System of Systems) to develop the next generation of smart adaptive systems for autonomous sensing, embedded intelligence and data analytics.

c- Recommendations for concept 8 Sensor Integration

The particular requirements for every sensor system deployment are in general individual to that deployment. As such, there is no single solution to meet the needs of all sensor networks, a "one size fits all" solution. There is currently no generic WSN solution to meet the demands of all scenarios and which would enable scale up of manufacture and economies of scale associated with large volume manufacture. Adaptable (through software solutions) systems offer the best hope for volume production of hardware platforms capable of operating in multiple scenarios and application domains. These smart sensing systems will need to exhibit learning and adaptive behaviour so they can exist in multiple application domains and adapt their behaviour so that it is appropriate to the domain in which they are deployed.

V.5.1.5.9 Concept 9: Reliability, Functional Safety & Security[48]

a- Table of concept 9: Reliability, Functional Safety & Security

	Medium term: 5+	Long term: 10+
Reliability, Functional Safety & Security		
a) Key research questions or issues		
To function as specified under stated conditions for a specified lifetime and within control recognised parameters to achieve an acceptable level of risk such as to prevent physical injuries or damages to the health of people, either directly or indirectly, and to provide secure operation against intrusion		
b) Potential for application or Application needs and Impact for Europe		
Most demanding applications, e.g., in Healthcare, automotive, Industry 4.0, require new functionalities and higher performance in integrated systems whilst operating safely and securely. Also, while global competition and outsourcing offer opportunities for decreasing time-to-market and cost per product the increased complexity of the supply chain raises the risk of security and quality.		
c) Technology and design challenges		
There is an increasing number, complexity and diversity of the functional features generated and integrated components There are many new technologies and materials for which no standard methods and tools for testing exist There is a need to increase in reliability and safety level, in particular as integrated systems are being deployed in ever harsher environments		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
• Hardware security, tamper protection • Cyber Security incl. data encryption, transfer protocols and data privacy • Physics of failure, modelling and virtual testing • Reliability and accelerated testing • Temperature control (energy-efficient thermal management of hot spots) • Operating temperature (harsh environment) • Hermeticity/insulation • Humidity • Biofouling • Corrosion resistance • Fault tolerance	+++ +++ +++ +++ <0.1 degree >100° C Operational constraints that are determined by application; Profiling sensors and data log/monitoring is required in field products	+++ +++ +++ +++ <0.05 degree >150° C Operational constraints that are determined by application; Profiling sensors and data log/monitoring is required in field products
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Interactions with all WPs		

b- Competitive situation for concept 9 Reliability, Functional Safety & Security

It is difficult to assess the competitive situation as solutions vary widely on applications and products. In many cases, in particular for new heterogeneous systems, testing schemes are based on standards developed for old technologies but not fully and rigorously adapted to advanced technologies

[48]Reliability was added to this table as distinct to Functional Safety after receiving feedback at the 2nd GW

c- Recommendations for concept 9 Reliability, Functional Safety & Security

This is an opportunity for European industrial leadership in reliability and safety methodologies based on determining the physics of failure, fast qualification of technologies and products, quantification schemes for design of excellence and prognostic health monitoring. Also, it is important for Europe to address the increasing application-dependent demands on operational constraints for advanced heterogeneous systems. Security needs to be addressed separately at the level of supply of critical components, hardware and data protection.

V.5.1.5.10 Concept 10: Ubiquitous/Pervasive

a- Table of Concept 10: Ubiquitous/Pervasive

	Medium term: 5+	Long term: 10+
Ubiquitous/Pervasive		
a) Key research questions or issues		
To sustainably[49] advance ambient intelligence, where electronics seamlessly integrated with any type of environment, to monitor and respond to the user's specifications by further miniaturisation and cost-efficient manufacture of smart(er) integrated systems		
b) Potential for application or Application needs and Impact for Europe		
Miniaturisation along with functional integration and high-volume manufacturing will revolutionise the use of smart sensing and actuating systems with a transformative impact in manufacturing and citizen-centric services in smart environments incl. transportation, mobility, health, buildings etc.		
c) Technology and design challenges		
Manufacturing tools for robust integration of new materials, sensors and actuators in multi-component miniaturised smart systems on-chip and in-package Low-cost manufacturing for heterogeneous system integration Discovery and use of new eco-friendly and recyclable materials of heterogeneous components on various substrates		
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)[50]		
• Handling thin die • Flip chip placement accuracy • TSV aspect ratio (diameter) • Inspection tools for 2.5D and 3D devices and reliability tests • Heterogeneous integration exploiting transfer printing, 3D additive manufacturing etc. • Thin and large area electronics including R2R, S2S • Biocompatible and invisible sustainable materials • Lifecycle analysis (duration, recyclable)	10µm ±0.1µm >10 (<10µm) +++ +++ +++ +++ +++	<5µm less than ±0.1µm >? (<?µm) +++ +++ ++ +++ +++
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Interaction with WP6 Equipment, Materials and Manufacturing Science is needed to define Assembly & Packaging technologies for manufacturability of miniaturised heterogeneous systems		

[49] In environmental context

[50] Coordination is needed with Chapter V.6 to harmonise FoM according to new proposed tables on Assembly & Packaging technologies for manufacturability of miniaturised heterogeneous systems

b- Competitive situation for concept 10 Ubiquitous/Pervasive

For over a decade, Europe has been driving heterogeneous technologies for manufacturability of miniaturised smart systems based on diverse new materials and components. Europe is in a strong position to maintain this lead.

c- Recommendations for concept 10 Ubiquitous/Pervasive

Heterogeneous technologies for manufacturability of miniaturised smart systems need a long-term research and investment commitment. While much has been done for the translation gap at high TRLs (5-7), the innovation gap at TRLs 2-4 needs also to be addressed. Owing to the increased complexity of the value chain for heterogeneous technologies many more resources are required on the path-finding and development phases of new materials, sensors and actuators as well as their robust integration in multi-component miniaturised smart systems on-chip and in-package. Industrial design is essential to ensure users will integrate such technologies.

V. 5.1.6 Synergies with other topics

The synergies of the System Design and Heterogeneous Integration chapter with other chapters are natural. System Design and Heterogeneous Integration is on the top of all the other topics collecting their outputs that must be considered for optimising the design and the implementation of heterogeneous integrated systems.
Specifically, the most important interconnections with topics covered in other chapters are:

- Chapter V.2 for considering novel approaches in device behaviours, not only related to fabrication, and so with a direct impact on heterogeneous integration, but on design too, where new paradigms have to be considered and implemented in the design-production chain;
- with Chapter V.3 the link is stronger on communication side, it was several times mentioned the importance of considering the interconnection (both logical and physical) as a milestone in the design of a system; with Advanced Logic the link is for the realisation of the needed design tools and the integration of the new technological solutions;
- Chapter V.4 contributes in bringing the issues related to sensors with their integration with readout interfaces and, for example, packaging specifications. The system is nowadays a merge of different technologies and physical domains, analysed in Chapter V.4;
- Chapter V.6 has the strongest link with the Heterogeneous Integration part, where the needed novel technologies must be bring to an industrial level, studying the manufacturing solutions and the related fabrication equipment.

V. 5.1.7 Recommendations

In the following, the most important recommendations related to System Design and Heterogeneous Integration are summarised:

- **Add Software in the middle**, starting from the application;
- **The value is not in the device itself, but in system integration and in the related data**, the Information is at systemic level;
- **Validation**: which is the level of robustness that is acceptable, confidence => When is it done?
- **Balance of how much happens at each node and the energy for transmission** (for reliability/security reasons too);
- **Where to position the intelligence;**
- The future is to move **from Embedded Computing to Embedded Intelligence;**
- Definition of **standards** for interoperability. Openness of standard cannot prevent monetisation.
- **Re-Usability / Reconfigurability**

- **Software-like re-programmability** with (almost) hardware like efficiency
- **Energy**
  - Management
  - Consumption when is necessary only
  - Importance of **categorizing the application in terms of Energy Boundaries**
- **Automated Design Space Exploration and Automated Design Decisions**
- **From Connected Devices to Distributed Embedded Systems** (System of Systems) => Network Synthesis, **Network is a Design Dimension**
- **Environment is Part of the System**

The strategic conclusion is that **it is for Europe a very good opportunity to drive an increase in System Knowledge**. In Europe many important stakeholders are present, with original knowledge, bringing Europe to a leading possibility for System Level Applications.

V. 6 Equipment and Manufacturing Science (WP6)

V. 6. 1 Executive summary

NEREID's approach to create a comprehensive "NanoElectronics Roadmap for Europe" is quite a challenge, in particular for WP6, where all other topics of the roadmap, e.g. Beyond CMOS, Nanoscale FET etc., have to be considered from equipment, materials and manufacturing perspective. In this first version, WP6 - Equipment, Materials and Manufacturing Science is mainly concentrating on equipment and materials, but does also reflect some manufacturing related things as well. The second version, which will be released next year, will include more manufacturing related topics.

The first version was drafted after several consultations with technical experts of WP6 during WP6 domain workshops, by analysing the available information of the other work packages and by reviewing the application oriented talks presented during the first and second general workshops. As a first attempt, no real figures of merits were given in the context of equipment and material. Nevertheless, there are indications on two different time horizons, when corresponding equipment and materials have to be available on the market for the different technologies.

V. 6. 2 Relevance and competitive value

In all the discussions with the NEREID WP6 Experts, it was clear that it will not be possible to include real figure of merits (FOMs) for this very broad section of the NEREID roadmap, but the availability indications are of high value as well.

The timely availability of required equipment and materials provides the suppliers the long-term visibility, which is needed to allocate the R&D investments to guarantee the successful continuation of the nanoelectronics industry in Europe. In fact Europe has a well-established supplier industry for nearly all application markets: More Moore, More-than-More, Heterogeneous Integration etc. The suppliers will take the advantage to initiate R&D work by them or in cooperation with the existing and excellent R&D ecosystem in Europe. But also European manufactures of ICs, MEMS and smart systems etc. will benefit by this road mapping activity. The topics around manufacturing science will guarantee, that the European manufactures stay competitive, even with partly mature facilities.

V. 6. 3 Vision

Processing tools and high quality materials have been the key enabling factors in the evolution of Nanoelectronics, and in particular in the area of More Moore. The objective of this WP is to extend this benefit to the increased complexity and variety of technologies developed for More-than-Moore but also

for nanoscale FET and Beyond CMOS, covered in this WP6 roadmap. A close cooperation was established between device and process developers, on one side, and equipment and materials supplier on the other side.

The scaling down of the MOS transistor has driven the progress in the ICs performance and the cost per function of the devices has dropped accordingly. For complex devices, the decrease of the cost per functions is achieved by the development of derivative options on top of the core processes and the integration of heterogeneous processes. This leads to increasingly complex line management driven by many process generations, multiple products with short life cycle and high variability in terms of demand. The roadmap aims to activate a converging network of experience and competency involving the academic community for the development of new tools and methods for fab productivity needed to increase efficiency in the fab by managing cycle time, advancing equipment and process control and yield enhancement by providing a reference schedule.

V. 6. 4 Scope and ambition

The first version of the WP6 roadmap is broken down into several concepts:

- More Moore
- More-than-Moore
- Manufacturing Science

And for each of them there will be detailed information listed in the tables of the next section.

V. 6. 5 Main Concepts

V.6. 5.1. Concept 1: More Moore

a- Table of concept 1: More Moore

Concepts/Technologies			
		Medium term: 5+	**Long term: 10+**
i) Concept 1: More Moore			
a) Key research questions or issues			
Nanoscale FET CMOS			
	Si based technology	X	
	Si(Ge) to Ge	X	X
	III/V		X
	FDSOI	X	X
	FinFET	X	X
	Nanowires	X	X
	3D Sequential	X	
Interconnects			
	Advanced low-k to airgap	X	
	Cu based (including liner / barrier)	X	
	Beyond Cu metallization		X
Emerging devices beyond CMOS			
	Tunneling FET (conventional materials)	X	
	Tunneling FET (2D materials)		X
	from charge based to spin based		X
Computing paradigms			

	Quantum computing		X
	Neuromorphic		X
b) Potential for application or Application needs and Impact for Europe			
The feeling exist that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered.			
c) Technology and design challenges --> Material and Process Technology Challenges			
Advanced Surface Passivation / defect passivation (new materials, scaled technologies)			
Material / thin film growth			
	Conventional semiconductor technologies	X	
	2D materials		X
	Spin based materials / stacking		X
Patterning			
	Area Selective Deposition	X	X
	Area Selective Etching	X	X
	EUVL	X	X
	DSA based litho	X	X
Metrology			
	Materials and contamination analysis	X	X
	CD and overlay	X	X
	3D metrology (physical and chemical parameters),	X	X
	Film thickness	X	X
	Metrology requirements for system integration	X	X

b- Competitive situation of concept 1 More Moore

The feeling exist that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered – but in certain domains (e.g. litho) Europe is playing leading role.

c- Recommendations on concept 1 More Moore

More specific needs in the other NEREID domains need to be identified.

V6.5.2. Concept 2: More than Moore

a- Table of concept 2: More than Moore

Concepts/Technologies			
Concept 2: More than Moore			
a) Key research questions or issues			
Sensors			
	Multi-parameter sensing	X	X
	Autonomous sensor systems	X	X
	Role of new materials and nanostructues in sensing (vs. Mature CMOS sensors)	X	X
	System-in-package (SiP) sensors	X	X
Energy			
	Energy usage	X	X
	High power / high Voltage	X	X
c) Technology and design challenges			
Material			

	Si	X	
	SiC	X	X
	GaN	X	X
	Others …		x
Manufacturing			
	CMOS integration, compatibility and readout circuit	X	X
	Maturitiy level	X	X
	Packaging	X	X
	Safety / Security	X	X
	Minituarization / form factor	X	X
	Biocompatibility	X	X
	Manufacturability /sensing functionality and micro-pumps	X	X
	Energy harvesting	X	X
Metrology and Test			
	Assembling testing, metrology and calibration	x	x
	Materials and contamination analysis	X	X
	3D metrology (physical and chemical parameters),	X	X
	Film thickness	X	X
	Metrology requirements for system integration	X	X

b- Competitive situation of concept 2 More than Moore

The EU has a strong international position in the field of More than Moore.

c- Recommendations on concept 2 More than Moore

Cover activities in WP6 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention (e.g. OLED)

V.6. 5.3. Concept 3: Manufacturing Science

a- Table of Concept 3: Manufacturing Science

Concept 3: Manufacturing Science			
a) Key research questions or issues			
ESH			
	Replacement materials	x	x
Productivity			
	Reference to IRDS /ITRS section where possible	x	x
Automation			
	Reference to IRDS /ITRS section where possible	x	x
YIELD			
	Reference to IRDS /ITRS section where possible	x	x

b- Competitive situation of concept 3 Manufacturing Science

There are a lot of standards (e. g. SEMI) on ESH, productivity, and automation for equipment available. Equipment has to be as compliant as possible.

c- Recommendations on concept 3 Manufacturing Science

References to IRDS/ITRS tables will be given whenever possible in the second part of NEREID to avoid duplication of work.

V. 6. 6 Synergies with other topics (WP topics, if applicable)

- The application specific requirements for materials, processes and manufacturing are best covered within the roadmap of the other WP's (WP2 – WP5).
- Analysis of all other WPs material (presentation etc.) performed to derive requirements for WP6.
- Intensify communication with other WPs for further improvement of the WP6 roadmap.

V. 6. 7 Recommendations

- Concurrent WP's (WP2 – WP5) are analyzing their domains in view of the presented applications and derive immediate and long-term requirements in terms of materials, processes and manufacturing needs.
- The feeling exist that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered. However, more specific needs in the other NEREID domains need to be identified.
- Cover activities in WP6 roadmap where Europe is leading in terms of materials, processes and manufacturing, but where the demand from application side is stronger outside of Europe (e.g. EUV litho)
- Cover activities in WP6 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention (e.g. OLED)
- Build synergies with ITRS/IRDS activities whenever possible, in particular for the section manufacturing science.

VI General Recommendations

The aim of future research activities in the field of Nanoelectronics is to further develop Europe's S&T excellence to support technology development and innovation and strengthen its competitiveness and market leadership of the related industries. Research and innovations in Nanoelectronics, covering the medium to long-term impacts, are crucial to the European technological leadership in ICT. They are complementary to ECSEL activities mainly devoted to short term applications.

The main recommendations for the Nanoelectronic Technologies covered by NEREID are mentioned below:

For Beyond-CMOS:

A thread running through most of the alternative computing approaches is the need to understand at conceptual, experimental and technological levels the thermal properties of materials and interfaces involved. This is currently a handicap ("show stopper") in the form of heat dissipation in almost all current and emerging technologies, where a shift of paradigm in the perception of the challenge is needed. Europe has the potential to lead in this field and, consequently, to remove this roadblock.

Silicon CMOS technology is currently dealing with the heat dissipation challenge mainly by tolerating the wafer real state cost of "dark silicon" and limiting the frequency of operation to the low GHz range, despite higher frequencies been demonstrated, albeit at a higher power consumption. In the long term, Brownian or entropy computing may well offer a better solution on their own or in a hybrid approach with other

state variables. Nevertheless, efforts are few and far between pursued by fragmented communities, each excellent in their own right.

In the near term neuromorphic computation holds a high promise applications such as the in IoT and big data, and is making inroads in hardware and algorithms. There are several technology candidates and the planned FET CSA may well accelerate progress currently in progress in the Brain flagship, in ICT LEIT projects and future constellations.

Si-based quantum photonics must be an integral part of the Quantum Technology flagship building on the European leadership in the field, already breaking frontiers in chip-level integration and competing globally in innovations, for example, with the nanophotonics-based components such as single photon detectors based on phase change materials.

The range of materials under investigation within alternative computing paradigms goes well beyond silicon, e.g., in quantum (nano)photonics, neuromorphic computing and spintronics. Steep slope devices are no exception. Thus technological advances are urgently needed with technological figures of merit in mind of several non-silicon based materials, ranging from scalable material production technologies, through wafer-scale nanofabrication with innovative tools and last but not least, a combined effort from the start with the design and architecture community.

For Nanoscale FETs:

-For Nanowires, identify the best material and geometry options for logics (high-speed as well as low-power), develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar), and consider the 3D aspects of processing.

-For FD SOI, develop differentiated options (RF, Embedded Memories, Imaging or molecules sensors) on FDSOI (applications for automotive, IoT, smart sensors…), ULP design (Vd<0,4V) for IoT market (wearable, medical…), and 3D integration for future neuromorphic and quantum computing approaches

-For FinFET, develop co-integration of different channel materials, low contact resistivity and high strain solutions, improve finFET analog performance

-For non-charge-based Memories, overcome the HRS broadening for OxRAM, improve the process for GST patterning for PCRAM, develop new materials enabling horizontal scaling

-For 3D sequential integration, define which applications will benefit from very high density interconnections (IOT, neuromorphic…), and develop a 3D place and route tool

-For Modelling/Simulation and Characterization, develop new tools taking into account all the new materials, technologies and device architectures in order speed-up technology optimization and reduce the cost of technology development.

For Connectivity:

Antennas & Passives:

On demand Re-configurable and tunable Antennas and Passives, very compact and massive MIMO antennas, with beamforming systems and very high antennas' directivity for all the used band, 0-6GHz and mmW. Work may address metamaterials, NEMs, MEMs and integrated passives technologies, packaging and modules, design, systems and microsystems.

Transceivers & Front End Radio:

High Data Rate:

Up to 100GHz and up to THz Transceivers, stable and accurate local oscillators, and antennas' interfaces targeting high and agile spectrum usage, with wider communication bands, allowing Full-duplex communications and solving Interference management, with on demand new PHY waveforms generation. Work may address New generation of nm CMOS, beyond CMOS, and mixed Silicon-III-V technologies, NEMs, MEMs, and new physics devices, combined with new design methodologies, modelisation and wireless long range, short range or wave guided systems.

Low Power Radio:

Ultra-low power transceivers for WSN and IoT Networks, with µW consumed power objectives. Work may address Wake-Up Radio, Ultra-stable ultra-low power time reference, charge transfer, or time-frequency modelisation and design methodologies, CMOS, Beyond CMOS, NEMs MEMs, and new physics devices, wireless, including ultrasonic, or silk guided systems.

Wireline:

Low cost 1300nm and 1500nm laser sources, optic modulators, LEDs, and PIN diodes, with their electrical interfaces, drivers and Trans impedance receivers, for modulations giving 400Gbs to Tbs. Work may address photonics integrated components, including laser and VCSELs, copper wireline interfaces, 3D packaging methodology, Multiphysics modelisation and simulations, CMOS beyond CMOS, and low cost exotic More than Moore processes.

For Smart Sensors:

Stability and reliability are the two most important features for the sensors. High reproducibility, ppb detection limits due to concentration, signature for functionalization, form factor and the power consumption of the platform are secondary characteristics that have to be taken into consideration for the sensor development. As mentioned already, selectivity is not the most important feature for sensing.

Assembly testing, metrology and calibration are crucial for the future success of smart sensors. There is a lack of metrology standards, commonly is difficult to interpret and it results in time consuming investigations. In addition, an easy way of calibration of the sensors or even better self-calibrated sensors does not exist in the market yet but is highly interesting and demanded. As an example, CMOS capacitive sensors have the advantage that they do not need to be calibrated.

CMOS integration, compatibility and readout circuitry. New enabling technologies keep coming. However, integration becomes more challenging and reliability gets less predictable. It is predicted that smart sensors will remain as close as possible to CMOS standards.

The maturity level of each sensor technology has to be assigned, estimating than a technology with a TRL higher than 6 would result to a product into market in less than 3 years approximately. The standards will be pushed very high in the different road-mapping but without excluding any technology for the next 10-year long term projection. The reason is that some application domains need mostly performance as in military while for others is the cost the most important factor or the repeatability, stability, reliability and yield for huge volume productions. A clear TRL correlation with technologies needs to be established.

Thus, the main identified gaps between 1980s and 2030 are manufacturability and cost (hybrid integration), robustness of design and in production, power computing and reliability.

For Smart Energy:

Apart from WBG device development the WBG system integration is necessary to exploit the full potential.

- Packaging and system integration technologies enabling low parasitic inductances to master EMC issues
- Packaging and system integration technologies enabling reliability at higher temperatures

- Handling higher voltages on package/module level and system level: SiC in medium voltage (MV) applications e.g. in traction and industry
- Low inductance packaging and integration technologies: power PCB with chip embedding, system-in-package (SIP), switching cell in a package
- Passive components for fast switching: mainly inductors, reduce losses at high switching frequencies, thermal management of (integrated) passives
- Characterisation, testing, modelling and reliability analysis of WBG packages, modules and converters.

For Energy Harvesting:

In general, the development of applications is the key. IoT and energy harvesting are application-driven today, so projects should mainly focus on the development of a complete application (from harvesting to the use case). Concerning the concepts covered so far in this mid-term roadmap (vibrational, solar, thermal EH and power management), the improvement of their performance and efficiency is as important as the development of "green" materials, replacing toxic/rare materials used nowadays (lead based piezoelectrics, Bi2Te3 for thermoelectrics). The use of nanotechnologies is foreseen to increase the performance of all the concepts in general. Flexible and low cost approaches for wearable applications should be developed as well. Increasing the bandwidth at a low frequency target (below 100Hz) will help to fit applications for vibration based mechanical energy harvesters. Concerning indoor photovoltaic applications, adapted structures and materials (light intensity and spectra…) should be developed. Concerning power management circuits, it would be key to investigate size reduction of inductors, to enhance the efficiency of inductor-less power converter circuit topologies, to develop planar alternative to inductors and to tune microelectronic process parameters and technologies to reduce leakage for reduced power consumption and allowing low input voltages.

For System Design and Heterogeneous Integration:

- Add Software in the middle, starting from the Application;
- The value is not in the Device itself, but in System Integration and in the related Data, the Information is at Systemic Level;
- Validation: which is the Level of Robustness that is Acceptable, Confidence => When is it done?
- Balance of how much happens at each node and the energy for transmission (for reliability/security reasons too);
- Where to position the intelligence;
- The future is to move from Embedded Computing to Embedded Intelligence;
- Definition of Standards for Interoperability. Openness of standard cannot prevent monetisation.
- Re-Usability / Reconfigurability
- Software-like re-programmability with (almost) hardware like efficiency
- Energy
    - Management
    - Consumption when is necessary only
    - Importance of categorizing the application in terms of Energy Boundaries
- Automated Design Space Exploration and Automated Design Decisions
- From Connected Devices to Distributed Embedded Systems (System of Systems) => Network Synthesis, Network is a Design Dimension
- Environment is Part of the System

The strategic conclusion is that it is for Europe a very good opportunity to drive the increase in System Knowledge. In Europe are present many important stakeholders, with original knowledge, bringing Europe to a leading possibility for System Level Applications.

For Equipment and Manufacturing Science:

- Concurrent WP's (WP2 – WP5) are analyzing their domains in view of the presented applications and derive immediate and long-term requirements in terms of materials, processes and manufacturing needs.
- The feeling exist that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered. However, more specific needs in the other NEREID domains need to be identified.
- Cover activities in WP6 roadmap where Europe is leading in terms of materials, processes and manufacturing, but where the demand from application side is stronger outside of Europe (e.g. EUV litho)
- Cover activities in WP6 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention (e.g. OLED)
- Build synergies with ITRS/IRDS activities whenever possible, in particular for the section manufacturing science.

VII Next steps

The mid-term Roadmap at Month 18 took into account the most promising nanoelectronic technologies needed to satisfy many applications very important for the EU economy and society. In the second part of NEREID (M18-36), this analysis will be refined for the proposed technologies and some other complementary options will be considered for the final Roadmap.

VIII General Conclusion

The first 18 months of the NEREID Project was very successful and led to a preliminary mid-term Nanoelectronic Roadmap including all the important technologies for many applications representing large future markets. The Nereid Roadmap took into account the specificity of the European industrial and academic landscape and will be very useful for equipment, semiconductors and application developments.

The project supported the participation of more than 100 application and technology experts, coming from leading research actors in industry and academia, to General and Domain Workshops. These Workshops allowed the consortium to better define the technology roadmap in terms of applications requirements (in the fields of Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing) and technology evolution (Advanced Logic and Connectivity, Functional diversification, Beyond-CMOS, Heterogeneous Integration and System design, Equipment, Materials and Manufacturing Science), and to discuss the convergence between applications and technologies.

This common work between technology and application experts is leading to the early identification of the main challenges and the most promising technologies needing additional R&D activities, which will be very useful for the future electronic components systems of European companies leading to a strong impact on the European economy and society.