SiNANO-NEREID Workshop:

Towards a new NanoElectronics Roadmap for Europe

Leuven, September 11th, 2017

WP3/Task 3.2

Connectivity

RF and mmW Design

Outline

- Connectivity, what connectivity?
- High data rates
  - Key parameters
  - Design trends
  - Design examples
- Low data rates
  - Key parameters
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  - Design examples
- Conclusion

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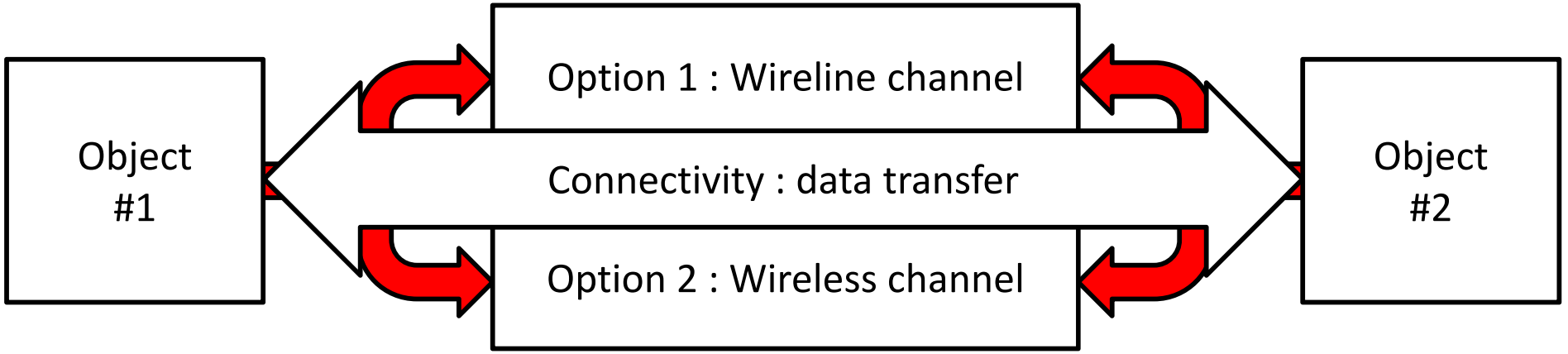
Connectivity, what connectivity?

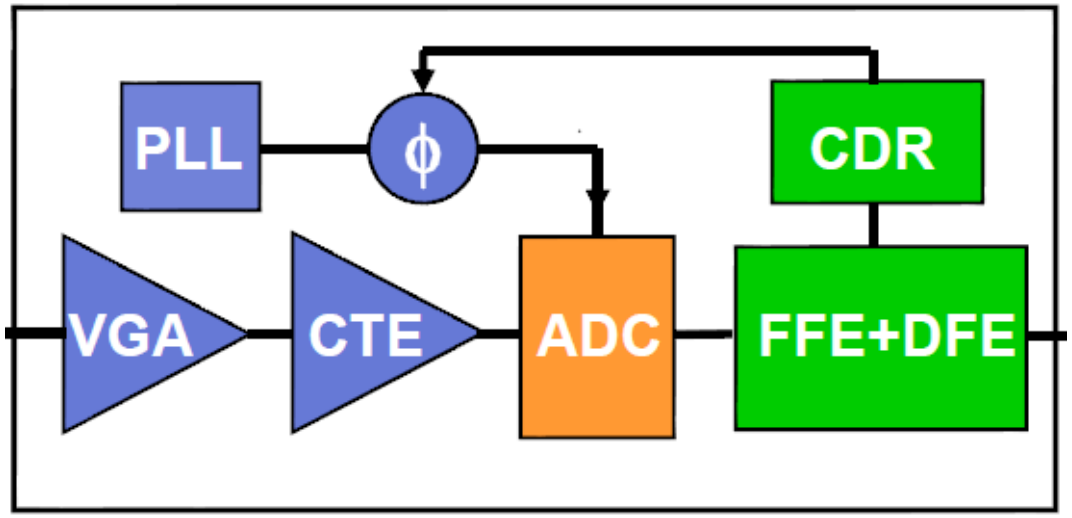


An object can be

- A thing (Internet of Things - IoT)
- A computer (HPC, data centers, etc.)
- A chip (chip-to-chip communication)
- Anything that produces and/or uses data

Wireline digital transmissions

- To increase the data rate, the industry is currently moving from NRZ to multilevel modulation formats (PAM-4, as a first step, for 100-400G) instead of further increasing frequency
- To ease signal processing when it comes to PAM-4, analog CDR are replaced by data converters
- The approach is similar to the one adopted by wireless transmissions a couple of years ago, starting from FSK (2G - GSM) to 64QAM (4G - LTE).



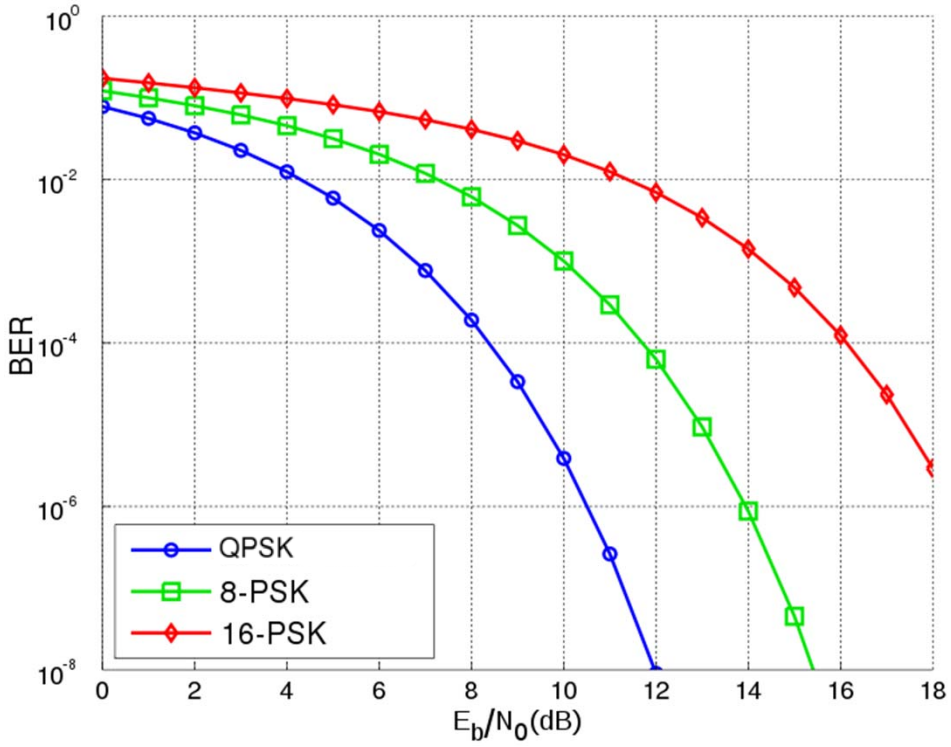
MACOM, 2017

Data converter based data receiver for M-ary (multilevel) modulation

M-ary modulation scheme issue

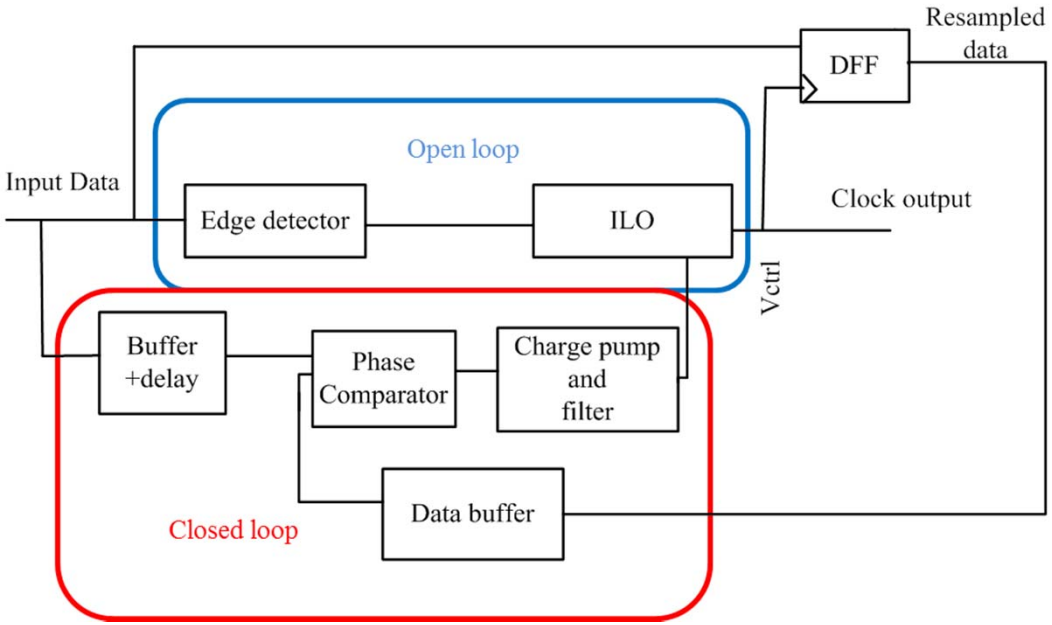
$$SNR_{dB} = 10\,Log\left(\frac{E_B}{N_0}\right)$$

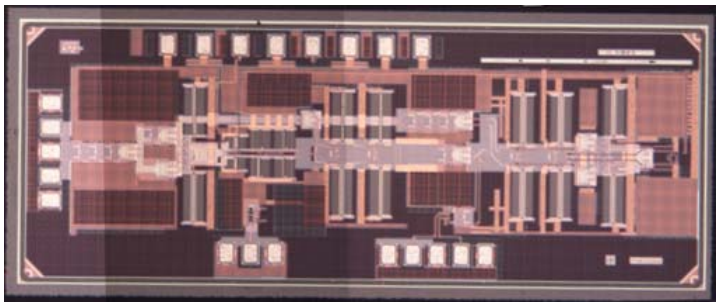
- E_B Energy per bit
- N_0 Noise spectral density (per 1 Hz)



NRZ to PAM-4
SNR loss : ~10dB

Feasibility has already been demonstrated

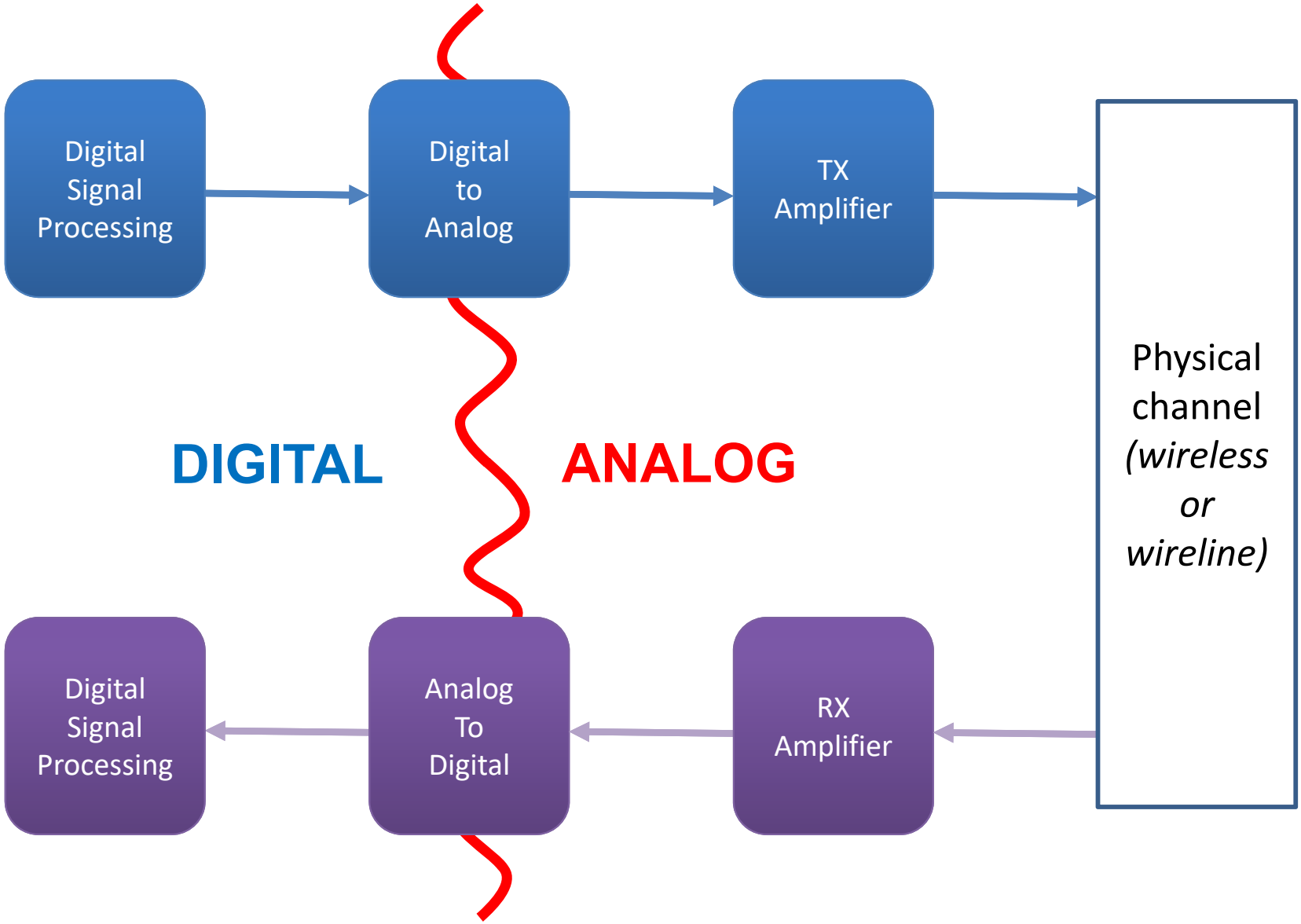




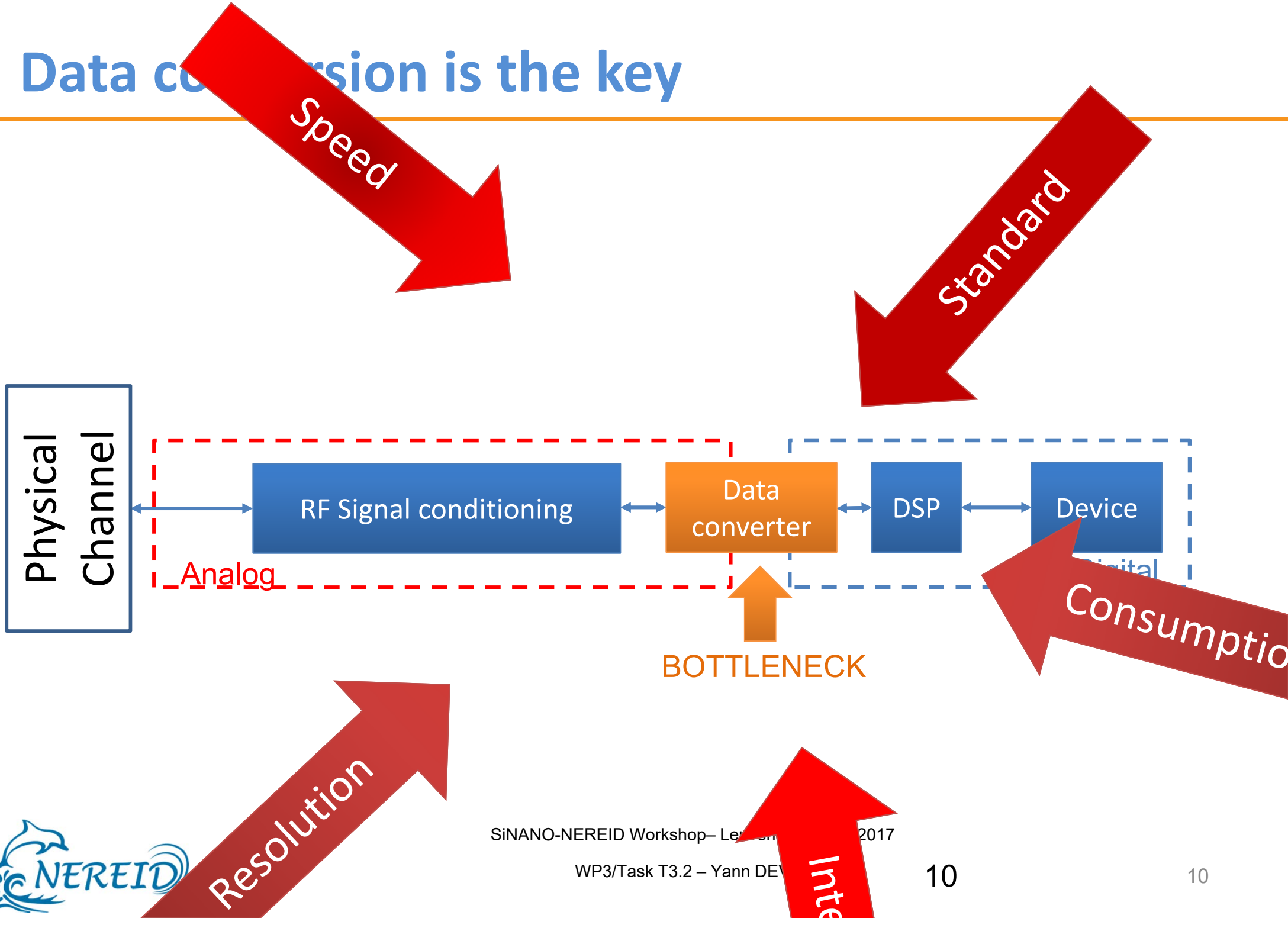
100 Gbps ILO-based CDR
(130nm SiGe, 1.4W)

- ILO can replace PLL for CDR at multi-100Gbps data rates
  - Resynchronization is mandatory within the demux when used as a receiver
- However power consumption is still quite high
- Low cost CMOS implementations are required to address mass market

Digital data connectivity



Data co rsion is the key



Connectivity trends

- Two use cases in parallel
  - High data rate devices
    - Wireline or wireless communications
    - Power consumption is an issue, thought not a critical one
    - Performance is the key : the higher the frequency, the better
    - Battery operated devices depict a dramatically reduced operating lifetime
  - Low data rate devices
    - Sensors and actuators – IoT
    - Mostly wireless, due to device mobility (static devices may use wireline)
    - RF frequency is preferred due to small range of mmW and THz
    - Power efficiency is the key : the longer the battery life, the better
- Low cost is an issue in both use cases
  - The mass market imposes its law

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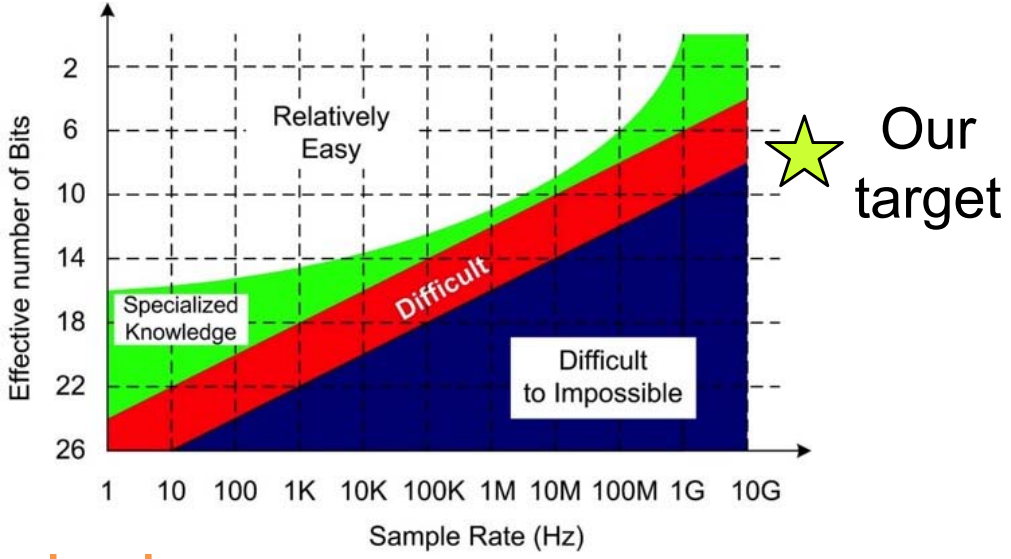
Key parameters

❖ Data conversion

➢ ENOB and clock frequency are criticals

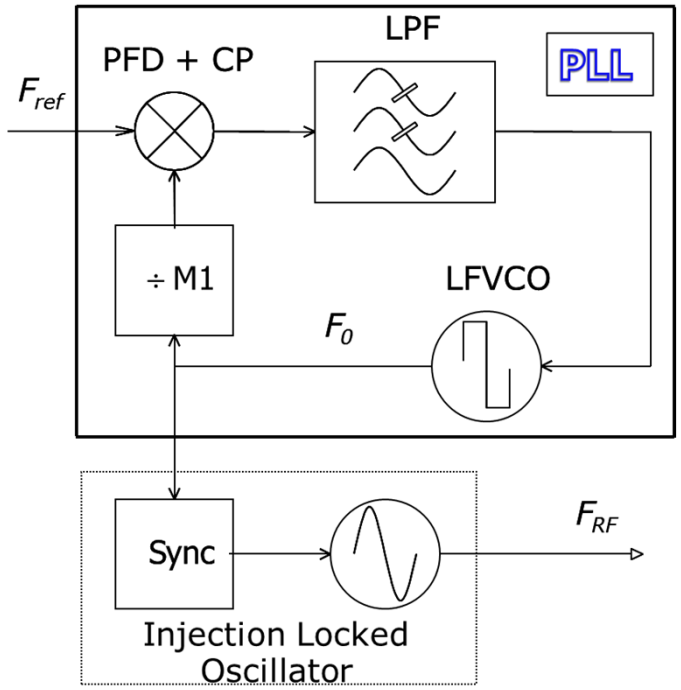
- PAM-4 requires 6-7 bits of resolution with a 60-100 GHz clock in order to reach the 100-400 Gbps barrier

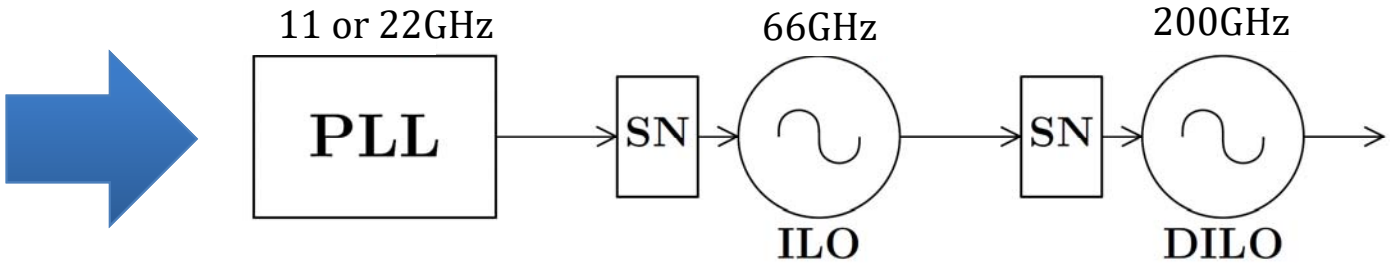


❖ High frequency clock

➢ The domain of interest is mmW to THz – and CMOS is mandatory…

Sub-THz frequency generation





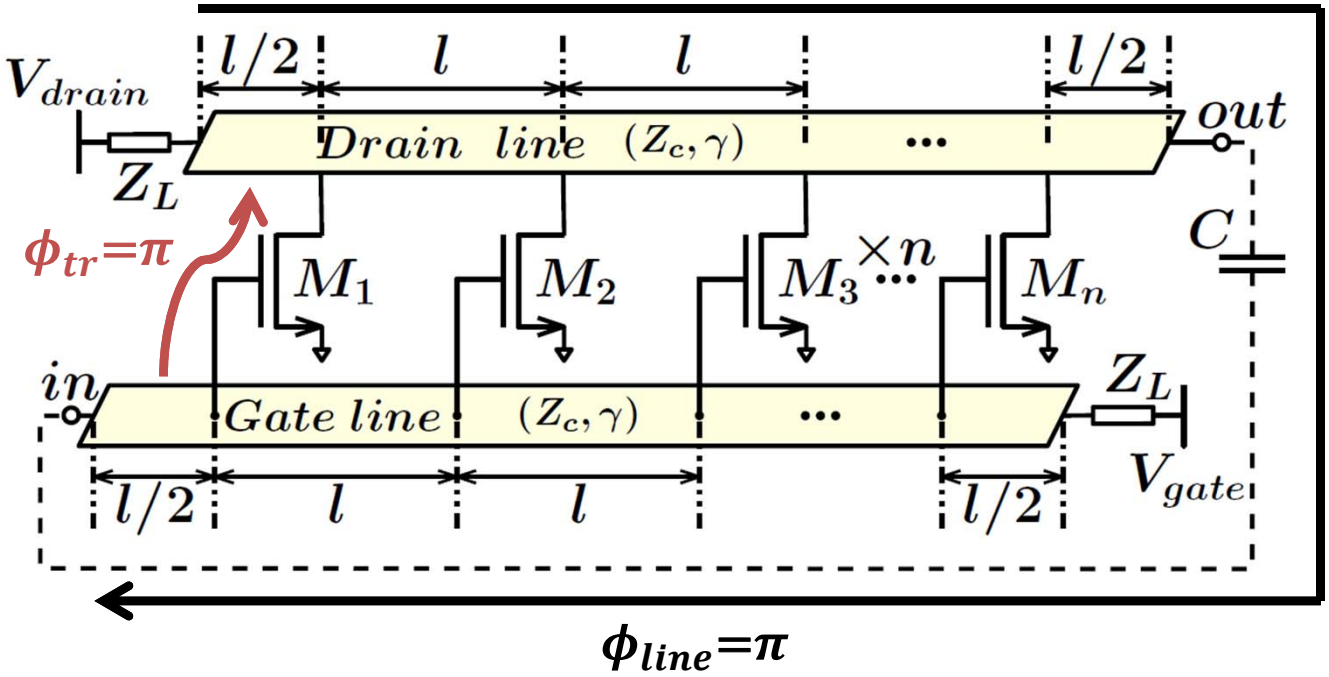
❖ Multi-loop synthesizer with injection locked oscillators in series

Sub-THz frequency generation : the approach

- Fundamental generation:
  - High output power
  - High efficiency
  - Low active component f_{max}
- Harmonic recombination:
  - High oscillation frequency
  - Low output power
  - Low efficiency

- New alternative, Distributed-Oscillators:
  - f_{osc} can exceed active component f_{max}
  - High efficiency close to f_{max}
  - Low sensitivity to active elements dispersion
  - Very compact for high frequency

Distributed oscillator principle



- Based on ideal distributed oscillator theory, oscillation frequency is given by:

$$f_{osc} = \frac{1}{2nl\sqrt{LC}}$$

[H. Wu, *et al*, JSSC 2001]

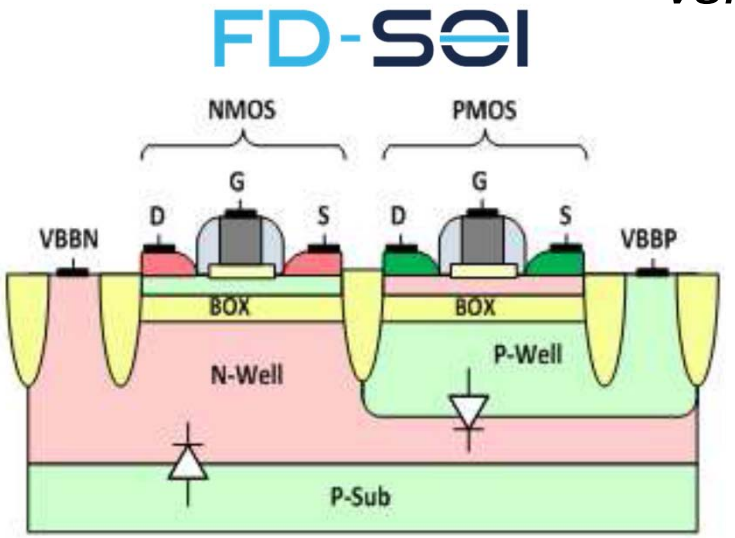
Wide-range Body Bias Enabled Phase Noise Tuning

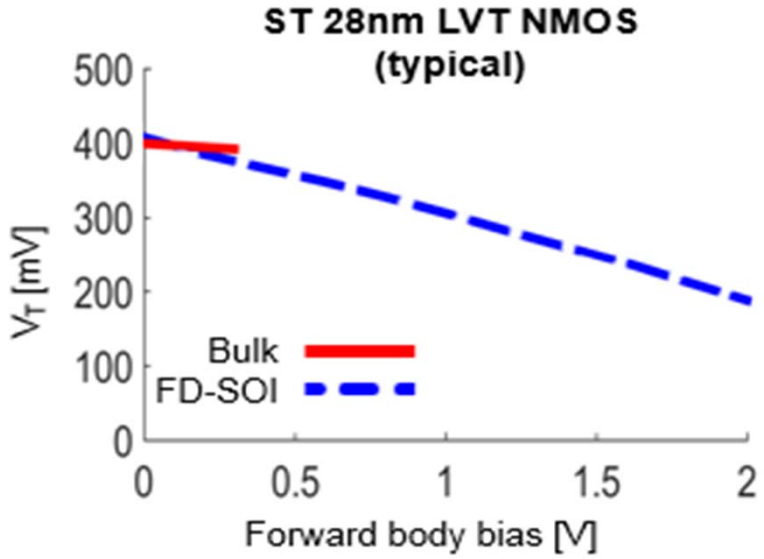
$$L(\Delta\omega) = 10\log\left[\frac{kT}{{V_{out}}^2}\cdot\frac{1}{R_p(C\omega_0)^2}\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right]$$

$$V_{out} \approx V_T + \frac{2I_D}{G_m} \approx V_T + 2nI_D(Z_L\|Z_c)\cdot e^{-\alpha nl}$$

Phase noise optimisation with « VT tuning knob »:

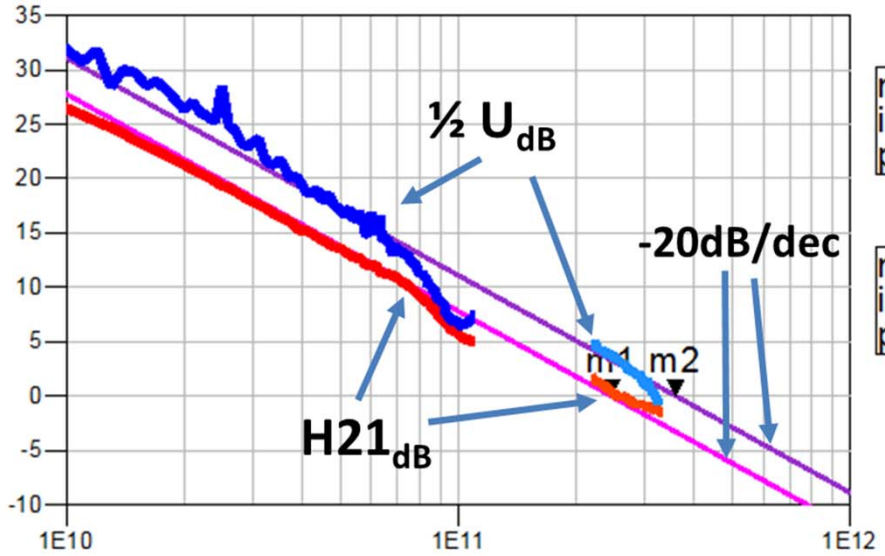
- Unique ~250mV V_T tuning range in FD-SOI *vs.* ~ 10's mV in any bulk CMOS

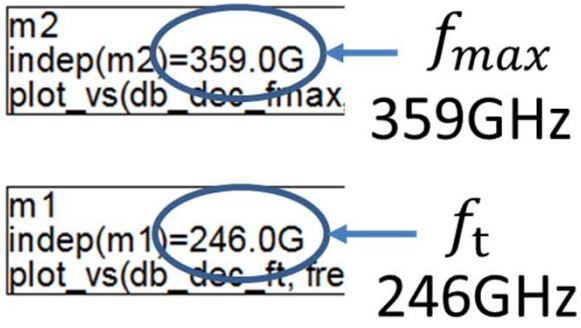




Extracted f_t/f_{max} for the proposed 28nm transistor

FD-SOI



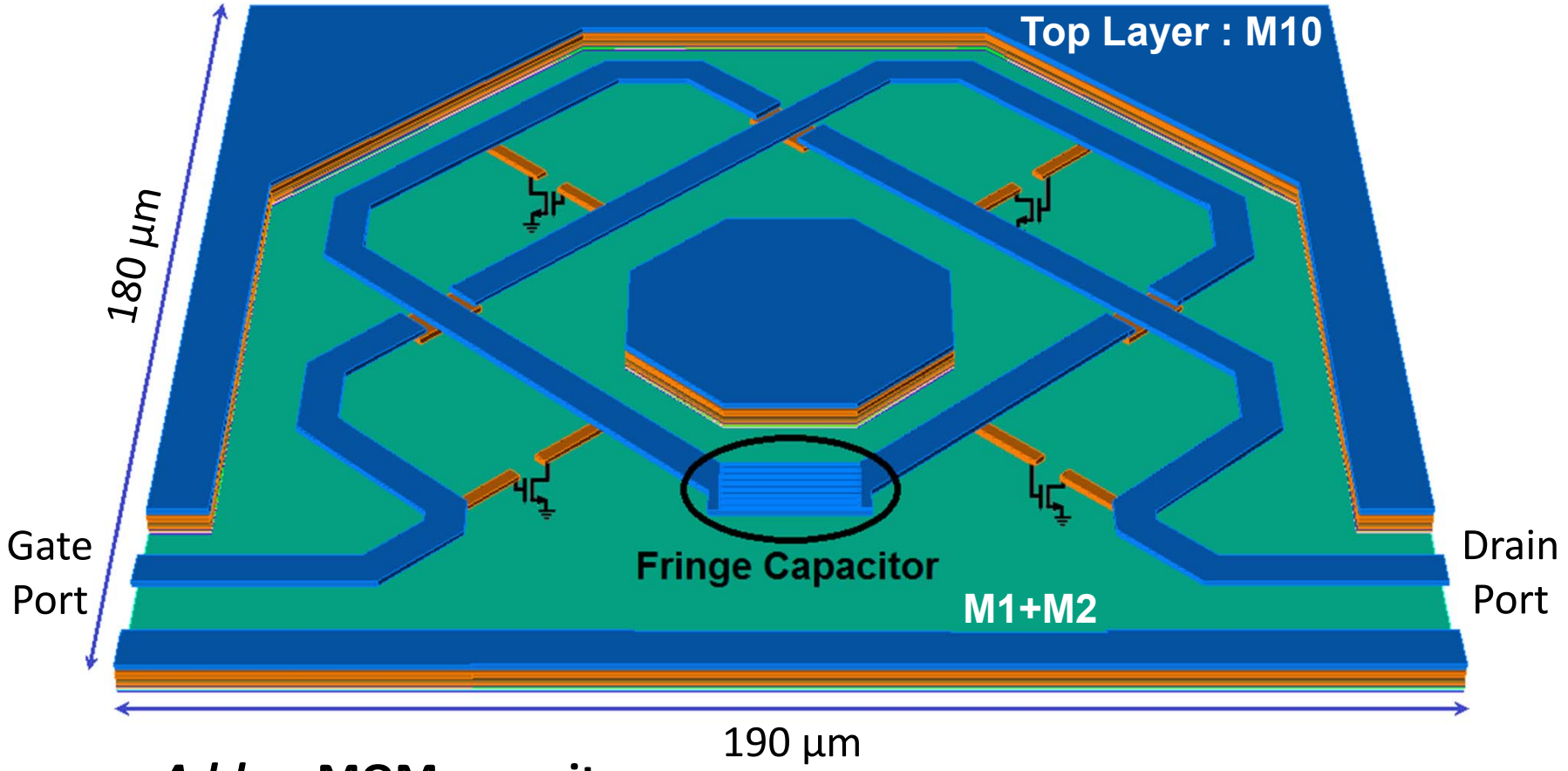


	Simulation PCell (M1)	Simulation Pcell + Full BEOL	Measurement
f_t	295 GHz	253 GHz	246 GHz
f_{max}	394 GHz	370 GHz	359 GHz

Nota: *on-wafer measurements with classical pads and access de-embedding method; Measurements performed on 10-110GHz and 220-330GHz test benches independently*

Physical implementation

Simplified layout view @134GHz

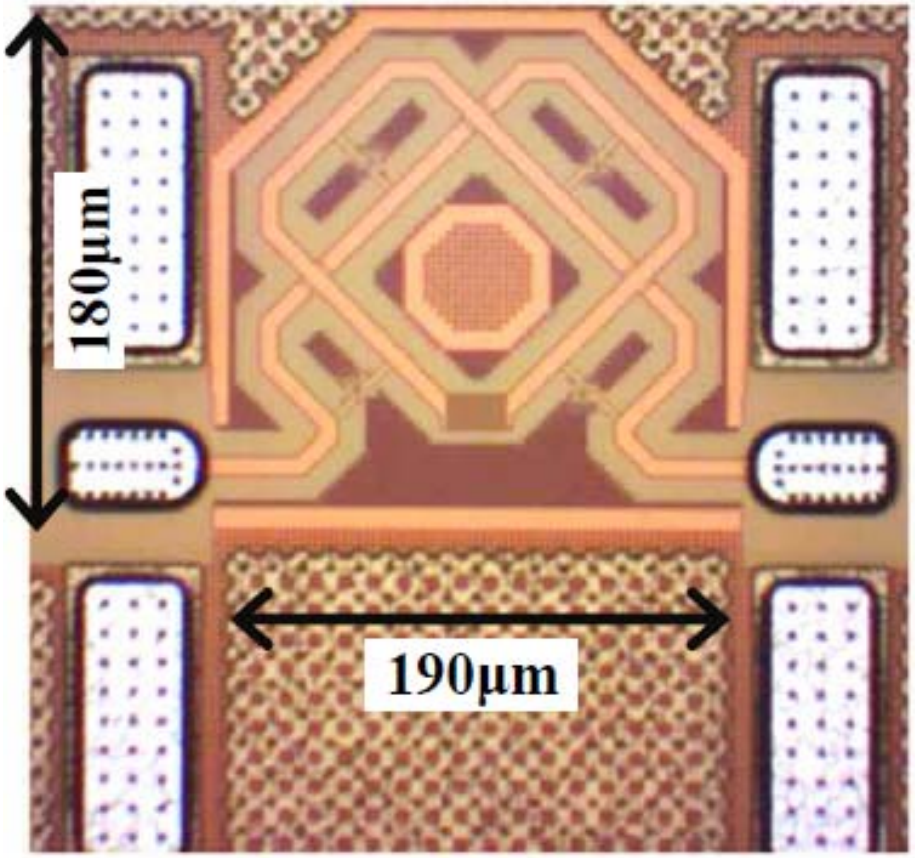


***Ad-hoc* MOM capacitor losses < 0.3dB @134GHz**

Total losses between the two ports: ~2dB

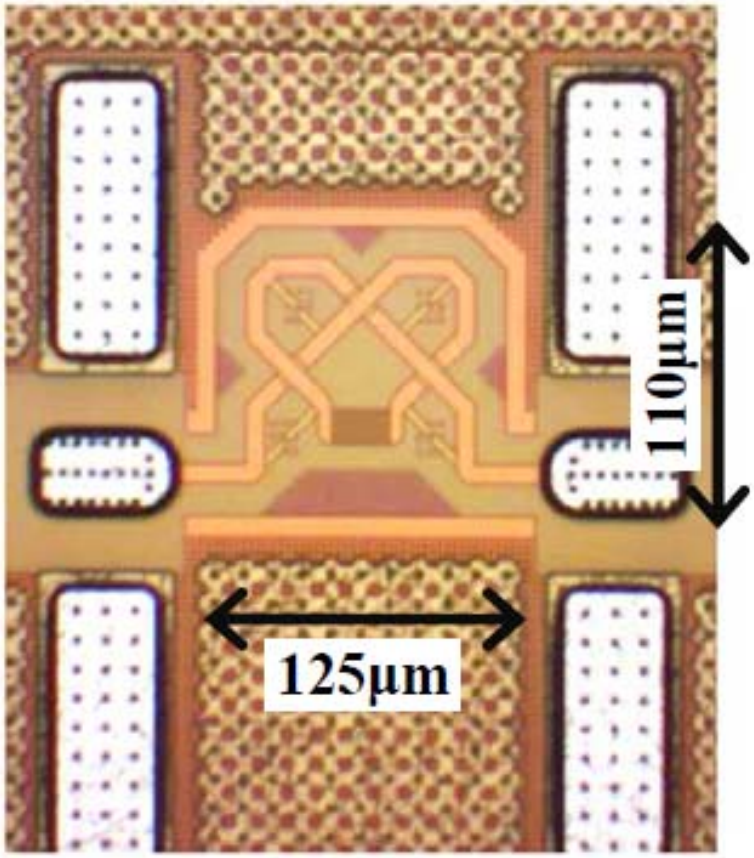
Chip microphotograph

@134GHz



Area with Pads : 0.087 mm²
Active area : 0.034 mm²

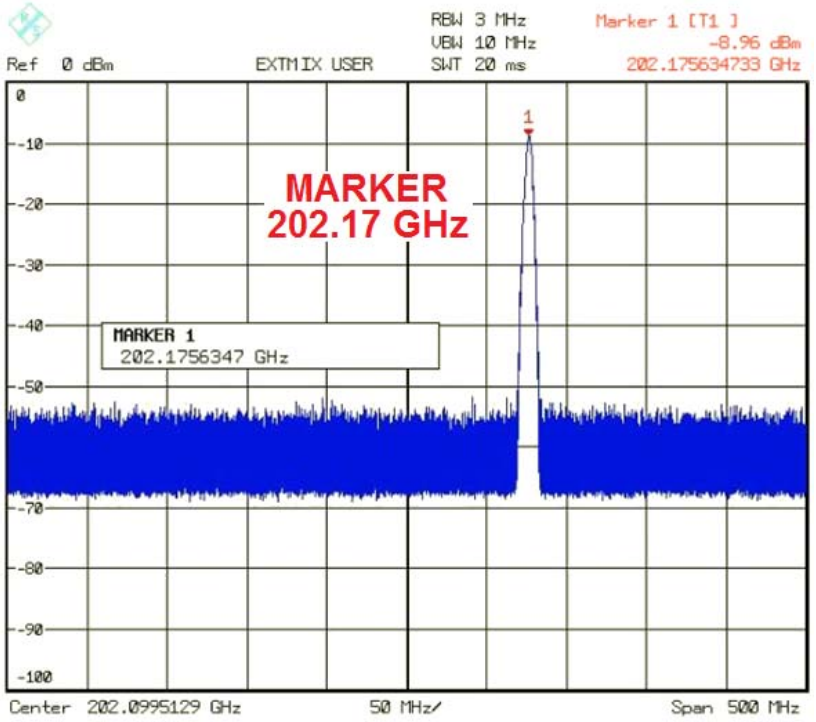
@202GHz



Area with Pads : 0.065 mm²
Active area : 0.014 mm²

202 GHz oscillator measurement results

Measured output spectrum and phase-noise

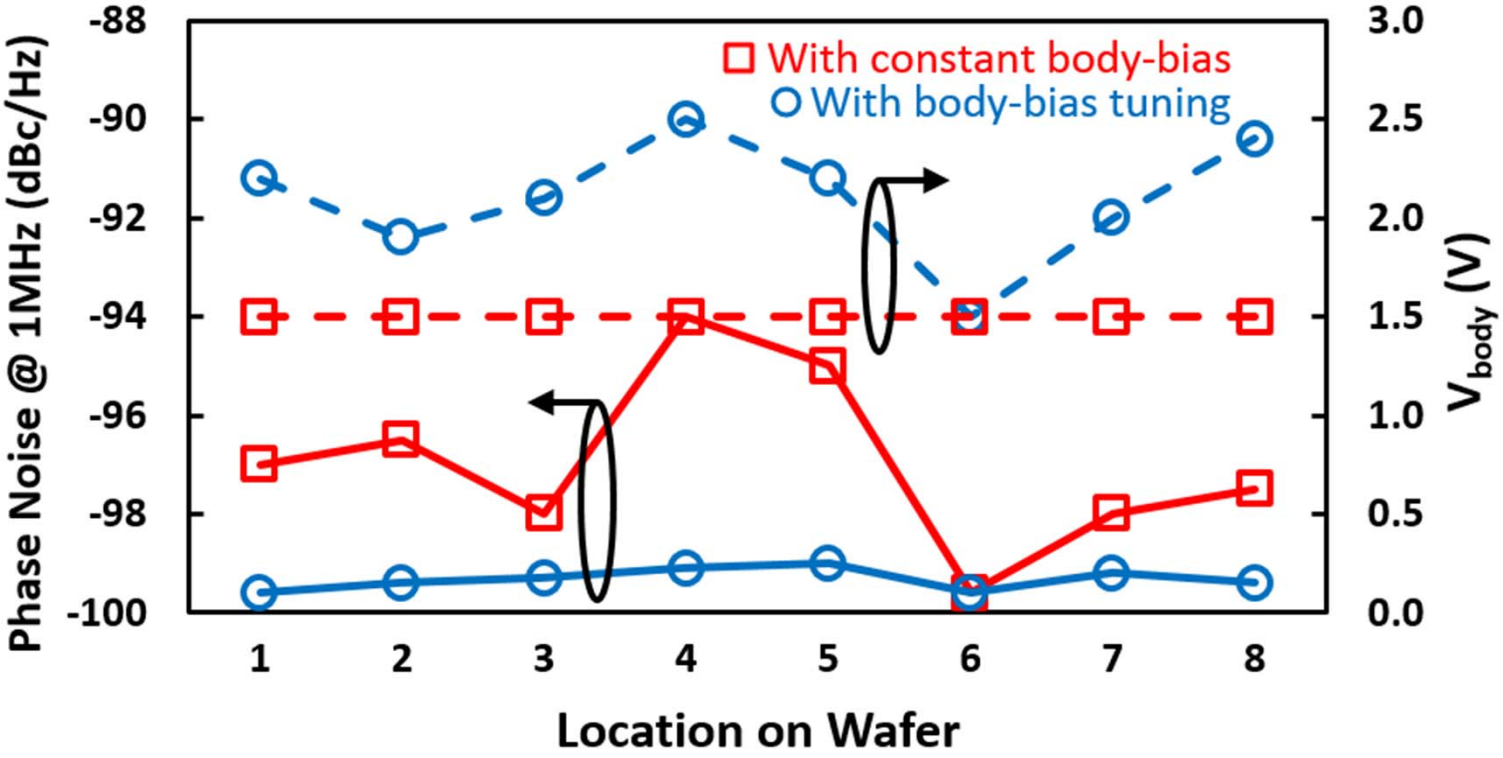


* Non de-embedded amplitude

V_{body} = 1.5 V, V_{drain} = 1 V, V_{gate} = 0.5 V

Phase noise optimization with body bias

Measured phase noise @ 1MHz offset, for different locations (#8).



V_{body} : Sweep
V_{drain} = 1 V
V_{gate} = 0.5 V

For constant $V_{body,}$ less than 6% variation
Optimization through body-bias tuning

Power consumption is only 20mW

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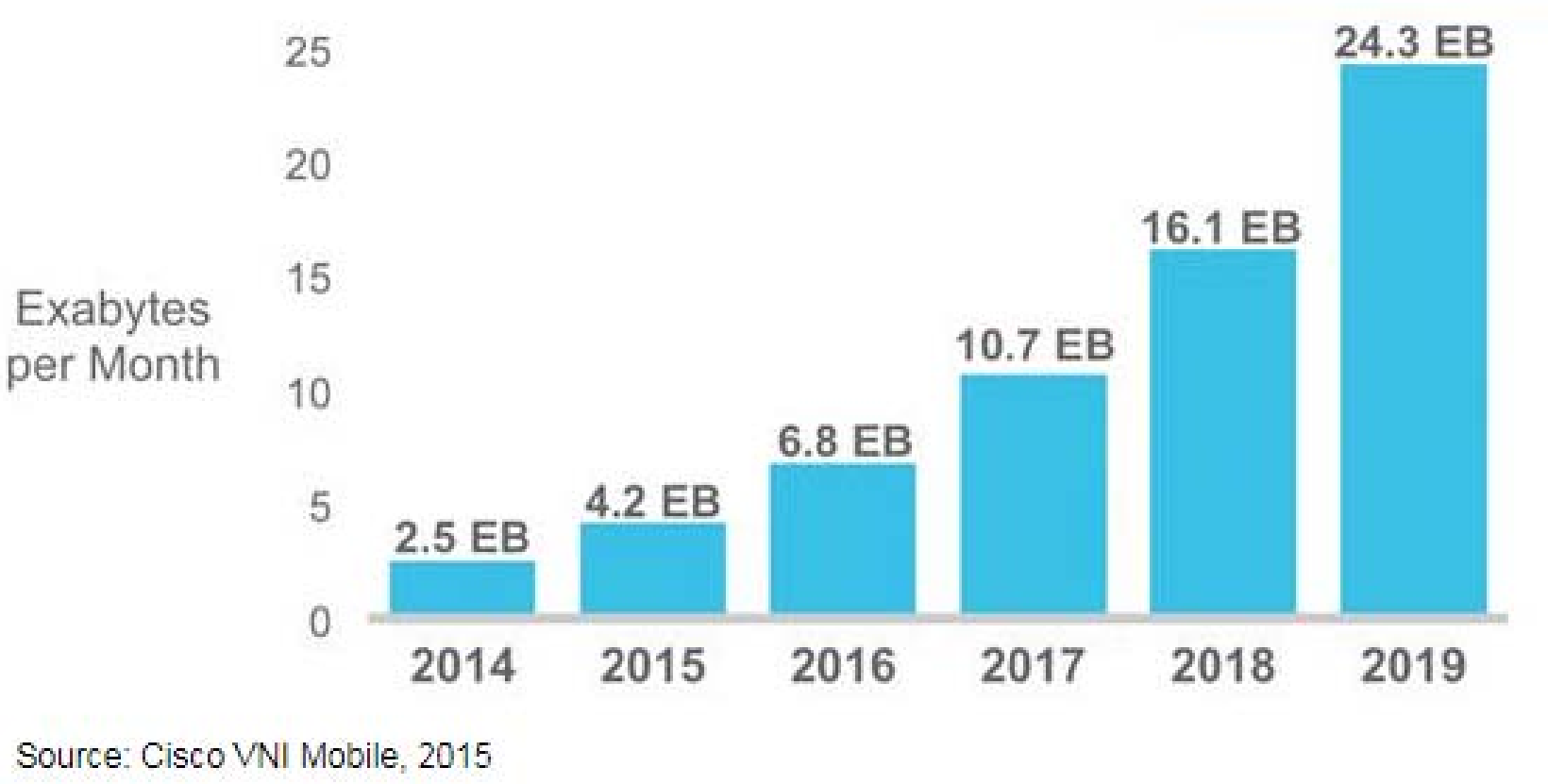
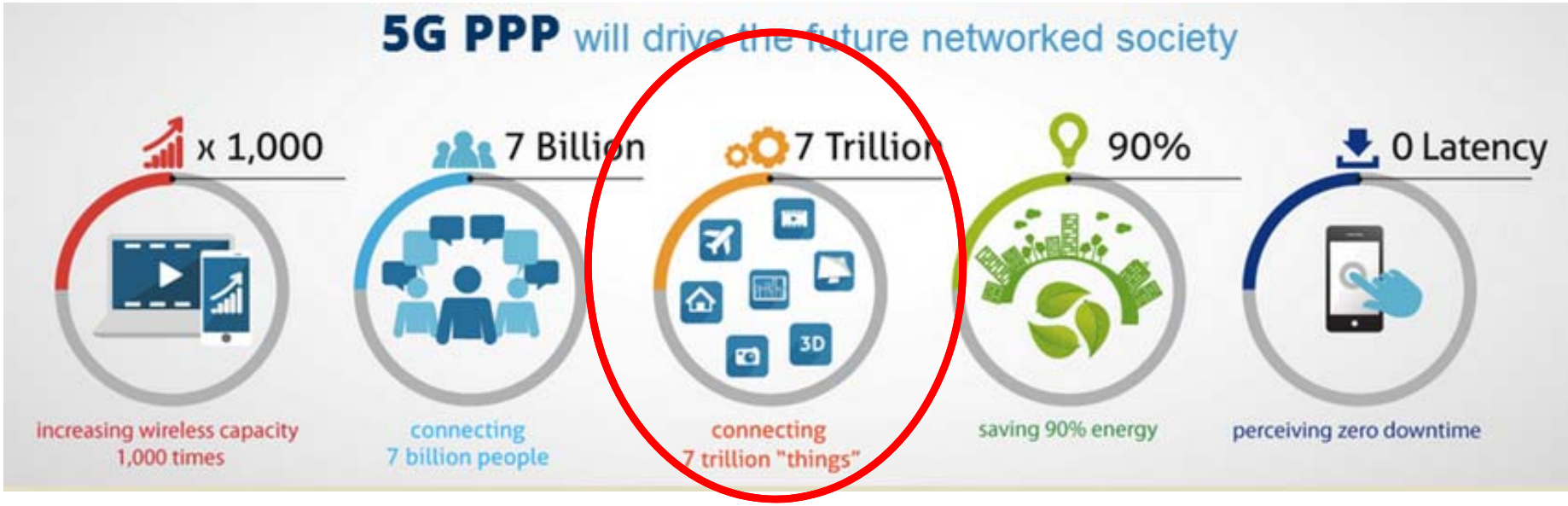
Wireless data consumption



Source: Cisco VNI Mobile, 2015

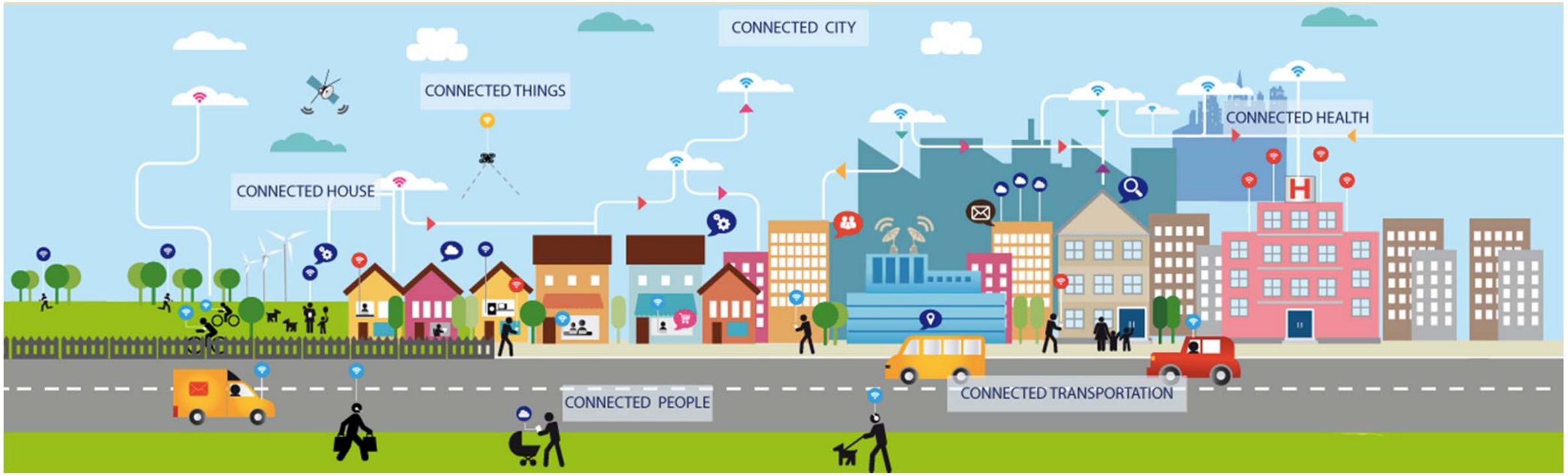
97% of this will be used by smartphone

Why do we have to take care of the 3% ?



An ocean of silicon!

IoT : a world of connected devices



Trillions of battery-powered wireless devices

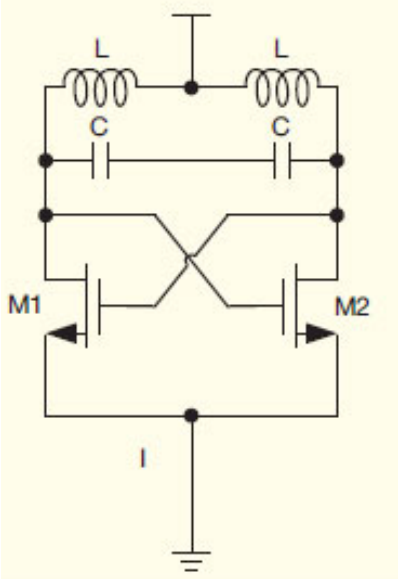
Low cost (CMOS)

Low consumption (RF frequency)

Inductorless ICs are mandatory to stay tiny

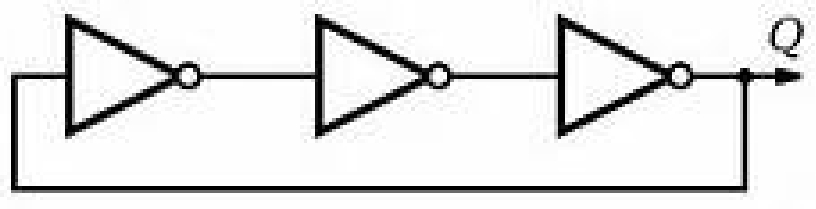
The oscillator case study

LC tank resonator



- Low phase noise
- High power consumption
- Large die area

Ring oscillators



- Low power consumption
- Small area
- Poor phase noise
- PVT sensitive

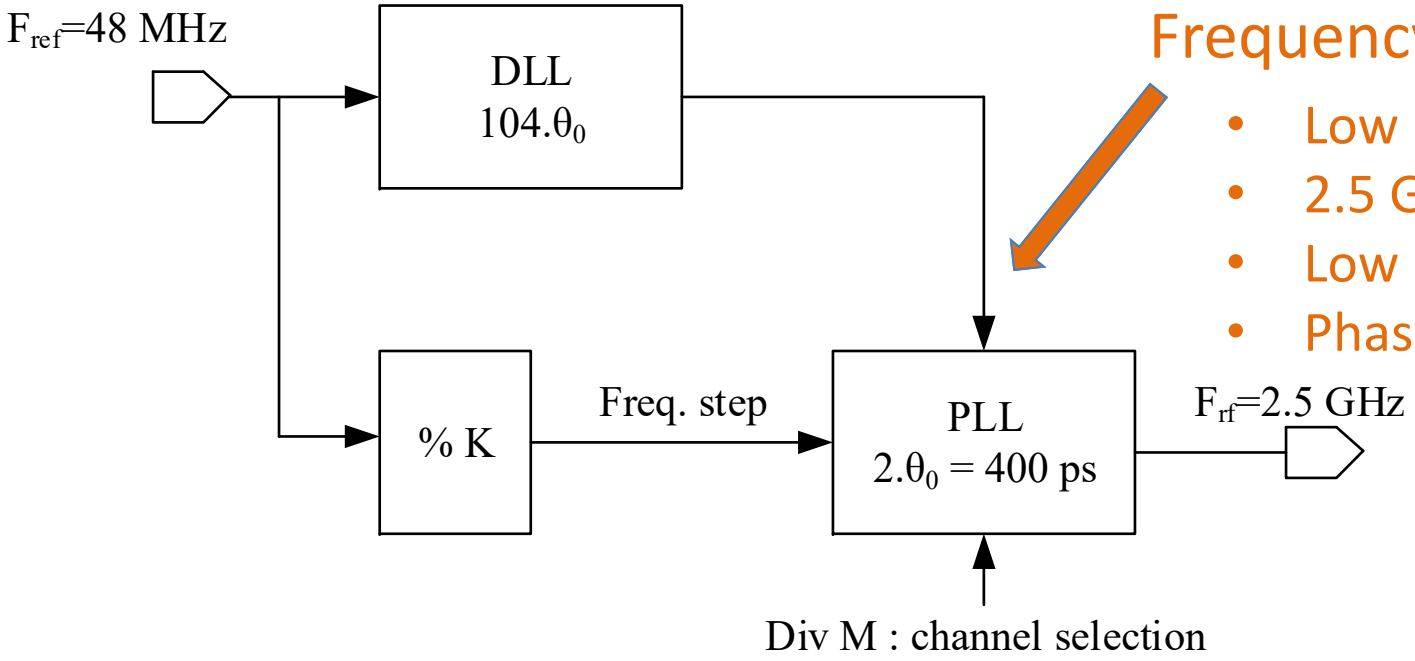
A potential solution : the FD-SOI DLL-enhanced PLL

Delay element coarse tuning

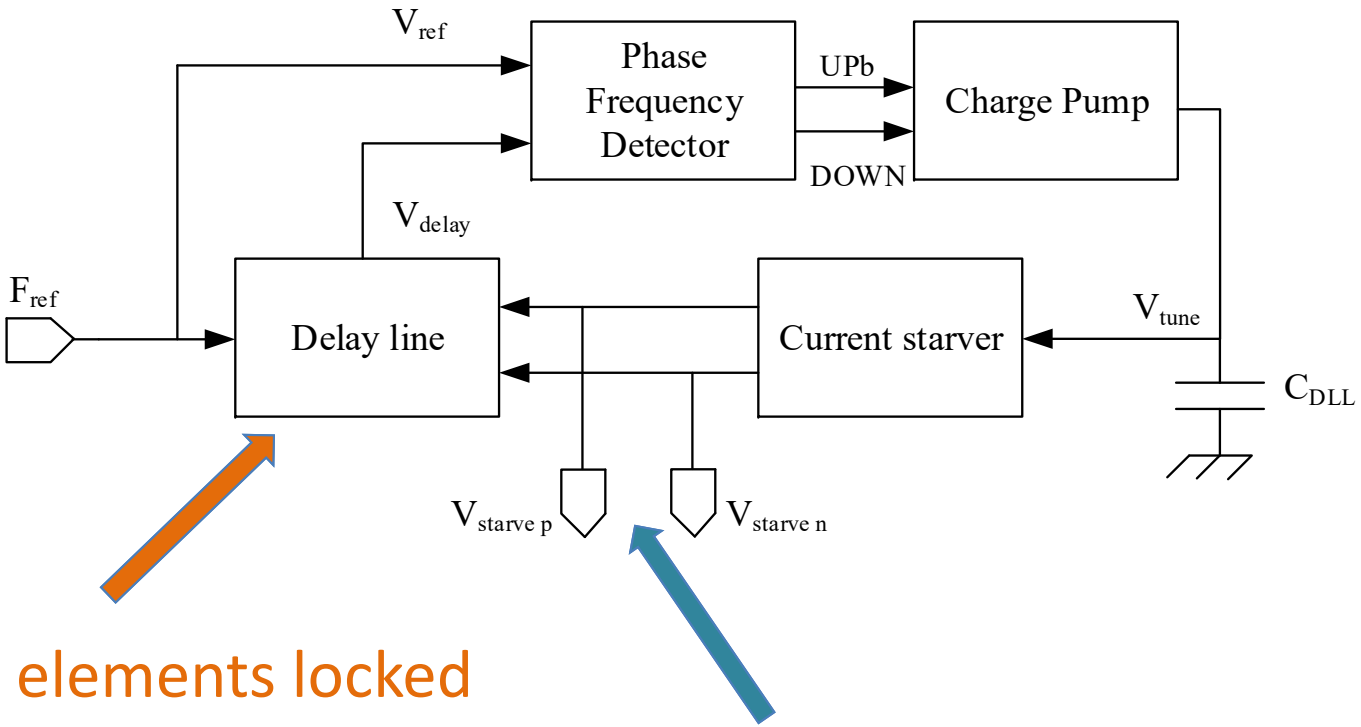
- PVT compensation
- 400 ps (2.5 GHz) single-element delay locking

Frequency synthesizer

- Low K_{vco} for reduced coupling
- 2.5 GHz center frequency
- Low power oscillator
- Phase noise cleaning



Delay Locked Loop design



N unit-delay elements locked to a reference period through current starving

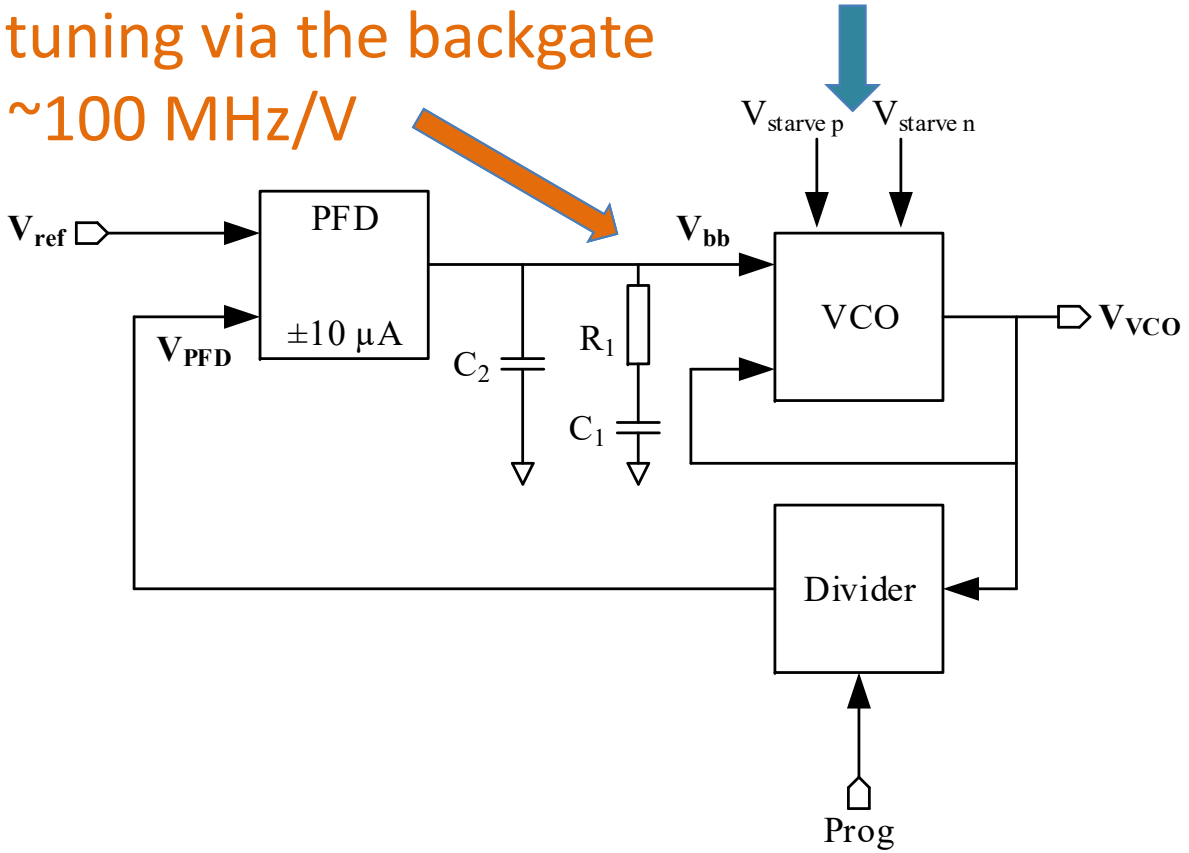
The starving voltages drive the unit-delay oscillating element in the PLL

Phase Locked Loop design

Starving voltages from the DLL

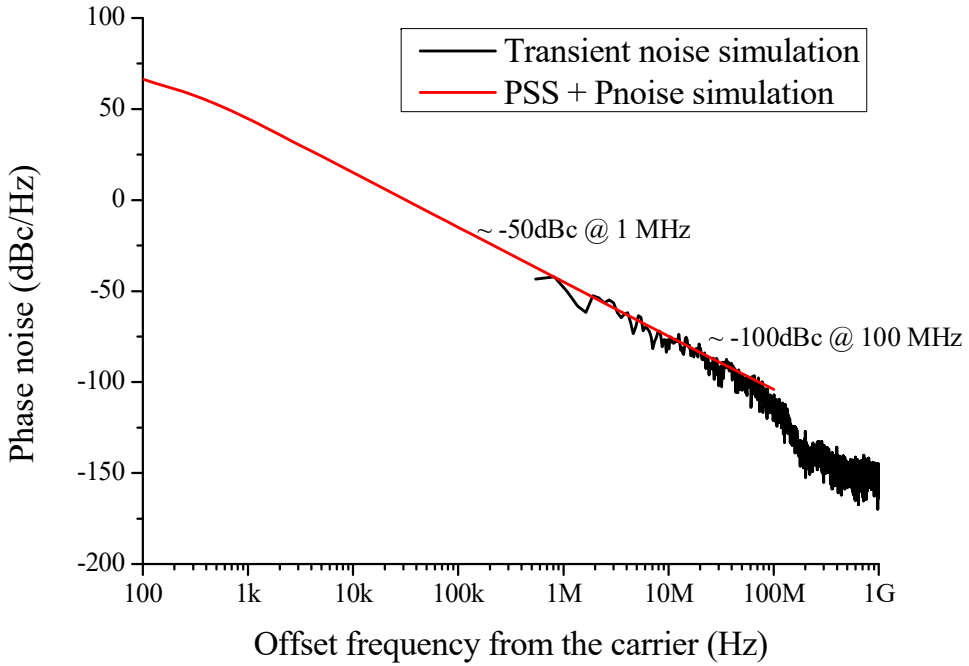
PLL frequency tuning via the backgate

K_{VCO} ~100 MHz/V

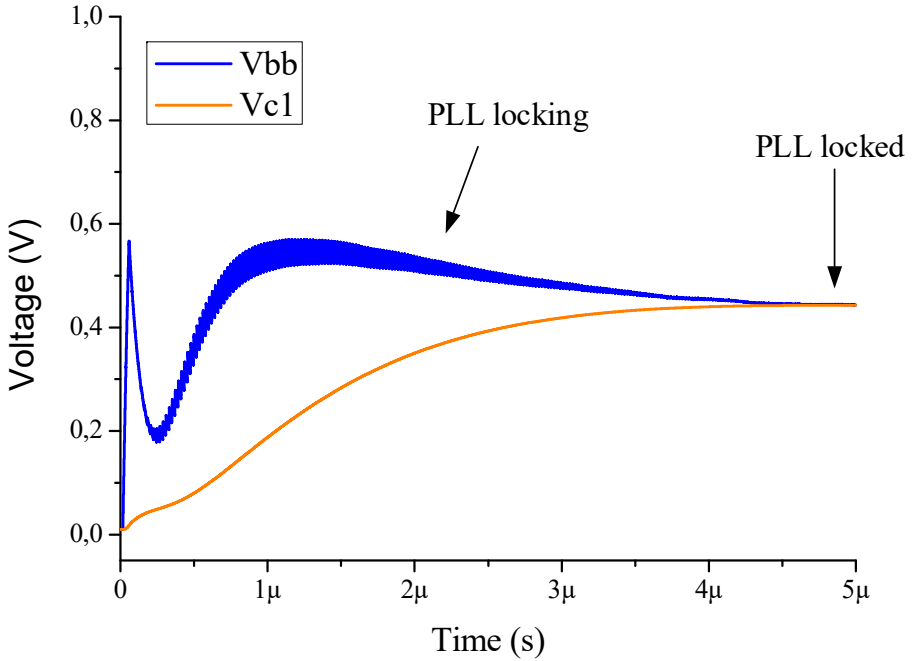


2.45-2.55 GHz
RF output

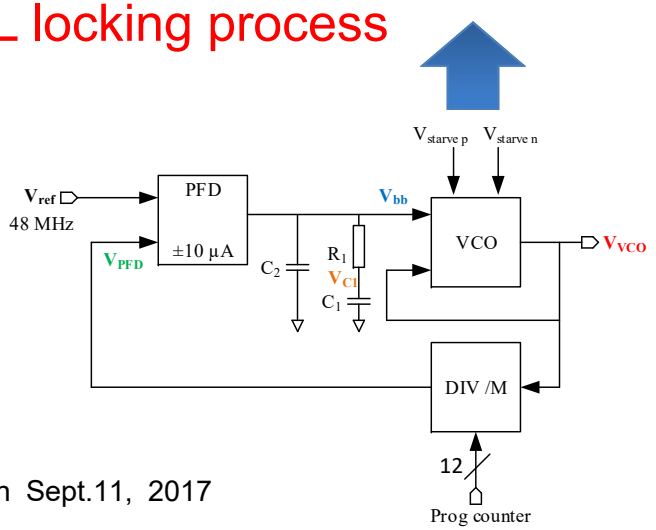
Post Layout Simulation results



Free running VCO



PLL locking process



Observed Phase Noise - PLL
PN @ 100 KHZ (locked) = -70 dBc/Hz

Power budget

	Block	Consumption (µW)
DLL	Delay line	29
	PFD + CP	1
	Current starver	18
Mutualized	CP current reference	10
PLL	VCO	11
	PFD+CP	1
	Divider	25
TOTAL		**96**

➡ Sub-100 µW power consumption

Performance summary – 28nm FD-SOI CMOS

VCO Topology	Ring oscillator
Synthesizer architecture	DLL-enhanced PLL
Center frequency f_0	2.5 GHz
Tuning range	100 MHz
Phase Noise @ Δf=100 kHz	-70 dBc/Hz
Locking time	5 µs
Power	100 µW
FoM	-175 dB

$$FoM = PN(\Delta f) - 20.\log(f_0/\Delta f) + 10.\log(\text{Power}/1\text{mW})$$

State-of-the-art PLLs exhibit FoM in the range [-169 dB ; -180 dB]

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Conclusion

- High data rate connectivity requires high performances
  - High performance technologies are welcome (FinFET)
    - However FD-SOI too has demonstrated its capabilities
  - High performances topologies
    - Smart circuit design is required – revisited and novel architectures
  - Power consumption is not (yet) critical
    - Reliability issues might appear while ageing
- Low data rate connectivity requires ultra-low power capability
  - Battery operated devices with long lifetime are mandatory
    - Design optimization as well as optimal architectures
  - Performances are lowered as a tradeoff w.r.t. ultra-low power
    - Standards have to take this point into account

Conclusion

- Connectivity is a mass market
  - Designing low cost devices is of tremendous importance
    - Low cost technologies are preferred, but a tradeoff with time-to-market is also to be considered
  - Robustness is required
    - Optimization (for either power or performance) should be constrained to ensure robust devices
  - Reliability and test are major issues
    - Novel approaches are expected to counteract technological bottlenecks, but novel approaches yield to a lack of maturity