

SiNANO-NEREID Workshop:

Towards a new NanoElectronics Roadmap for Europe

Leuven, September 11th, 2017

WP4/Task.2



Introduction: Technologies/concepts covered by the Roadmap SMART Energy

- Power semiconductors
 - > SiC
 - ≻ GaN
 - > Si
- Packaging and passives for advanced power semi-conductors (high power & speed)
- System-level: Topologies for power conversion & control



Summary

- ✤ 1. Introduction
 - Societal challenges
 - Potential for power semi-conductors
 - General trends in power electronics
 - Technologies & applications
- 2. Selection of technologies & applications
- ✤ 3. Key figures of merit of devices
- ✤ 4. Challenges & issues
- 5. Roadmap
- ✤ 6. Current trends
- 7. Conclusions



SiNANO-NEREID Workshop-Leuven Sept.11, 2017

WP4/2 - Steve Stoffels



- These technologies, falling under the denomination of "More than Moore", do not scale simply with geometrical size, and are widely diversified; therefore new metrics will have to be identified for the roadmap. It includes two main Tasks:
- T4.1 Smart Sensors
- T4.2 Smart Energy
 - Europe has a lead in this area. Two of the three leading power companies are European
 - Infineon (#1), STM (#3)
 - **O On-Semi (#2) has branches in Europe**

The story...





B.J. Baliga, Advanced High Voltage Power Device Concepts, Springer

NEREID WORKSHOP BERTINORO OCT 2016

Introduction

- Global challenges require a rethinking of the energy infrastructure
- Integration of renewables on the grid
- Electrification of transport sector
 - Smart control of power supply & demand to integrate renewables in the grid
 - > Tighter integration of control logic with power electronics
 - Increase overall efficiency of our energy distribution system





Energy conversion and management...





The potential ...



Fraunhofer Gain Power Density by WBG IISB 143 kW/dm³ Galvanic coupled bidirectional DC-DC 2014: Full SiC Mosfet and @ 98-99 % Ceramic Link Design converters 200 kW Gain power and power density by DC-Converter component integration and newest component technology Wide Band Gap and high voltage for todays and future DC-DC Converters 2013: GaN Test Converter 2010: Full Unipolar Mosfet Design 2004: High Speed 2007: IGBT3 and IGBT3 SiC Diodes 100 kW/dm3 99 % 40 kW/dm³ 98 % 70 kW @ 5 kW/dm3 100 kW @ 25 kW/dm3 Departement Vehicle Electronics

C Fraunhofer IISB

Page 3

System benefit ...



Mobile Systems: Automotive

- Any mobile system should benefit
 - Higher efficiency is higher range or smaller storage
 - Smaller volume and lower weight of the converter and cooler
 - By leverage effect even smaller volume and lower weight of the storage

Good example is Toyota

- 10% fuel savings targeted, 5% achieved on prototypes already
- Power control unit down to 20% of volume, weight from 18kg down to 4kg
- On the market in 2020









Source: Toyota

Source: ECPE Roadmap Workshop 'Power Electr. 2025', Munich, 26.03.2015



Trends...





2. Selection of Technologies

- WideBandGap semiconductors will partly replace and extend the market for Si power components
 - SiC & GaN
 - Enablers for breakthrough efficiencies & novel applications



Potential for application



Lead Applications for SiC & GaN



WBG MARKET SEGMENTATION AS A FUNCTION OF VOLTAGE RANGE

Current status and Yole's vision for 2020*



Potential for application (GaN)



What? How? Why? Where? EMode 600V, DSO-20: > **Efficiency**: very high Example: >2.5kW SMPS in > > > 100V and 600V efficient SMPS sampling prototypes with where op. cost matters Enhancement (E) mode NDA Measured Efficiency - PFC, VIN=230VAC GaN HEMT 99.4 99.2 \$ 99.0 > Single chip, normOFF 98.8 98.6 45kHz 65kHz transistor 98.4 98.2 3000 > Robust, reliable P-POUT (W) Bottom/Top side Cooling Highest efficiency PFC Data centers Gate concept Emode 600V, TOLL: > **Density**: very compact > Example: **OLED TV** or other P-Gate sampling prototypes with 200-800W SMPS SMPS Enhancement mode NDA GaN HEMT 9mm Fastest normOFF Ultra-thin SMPS Low profile, small footprint Ultra-thin TV concept available > Can be tailored for high efficiency or high

100V-200V Emode GaN for Efficiency and Density

level

frequency operation

 Key for integration at chip and/or package

3. Key figures of merit devices :



Device level

- Normally off Vth > 2V
- Low gate leakage at maximum gate voltage
- Breakdown Voltage 650 V, 1200 V devices
- Ron vs Qg (efficiency vs speed)
- Dyn R_{DS,ON} < 20% at maximum voltage</p>
- Reliability/robustness > 20year
- Maximum operating channel temperature

System level point of view:

- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)
- Gate drivers

4. Research questions & issues



Technological and **material** issues that need to be solved in order to guarantee a large market penetration of these devices;

Technological and material issues

- Material (substrates, quality, reproducibility, supply chain, wafer size, maximum thickness for heteroepitaxial growth)
- Processing issues (contacts, gate, isolation)
- Normally off operation (hybrid or intrinsic)
- Isolated gate (MIS) devices
- Sustainable breakdown, Operational (rated) voltage
- Robustness (UIS, short circuit) & Reliability
- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)
- Gate drivers
-

4. Technology challenges



- Customers want cost parity <u>at the device level</u>
 - Replace e.g. Si SJ device by a GaN device that yields at par or better system efficiency
- GaN-on-Si wafer cost is (too) high
 - Multi-wafer reactors/New concepts
 - Growth on CTE matches substrates (poly-AIN, ...)
 - Others....to reduce growth time and Defect Density
 - 150mm versus 200mm (vs 300 mm ?)
- GaN Reliability is different from Si (JEDEC) and is not well enough understood—Need standardisation
 - JEDEC is a minimum requirement, but we need more (GaN specific testing like Dyn Ron, hard switching testing, surge current capability etc)

5. Roadmap for power components





- Roadmap Materials
 - GaN-on-Si

5. Roadmap for power components





SiC Device Roadmap

Y	ears	Si 4.5 kV IGBT or BIGT	4H-SiC 1.2 - 1.7 kV MOSFET JFET/BJT	4H-SiC 3.3 kV MOSFET	4H-SiC 6.5 kV MOSFET IGBT	4H-SiC 10.0 kV MOSFET IGBT	4H-SiC 15.0 kV IGBT	4H-SiC 20 – 30 kV IGBT GTO	AIN/ Diamon 30 – 50 kv IGBT/GTC
2	016	VVV	٧v	٧	x	х	х	x	×
2	018	VVV	VVV	٧v	٧	х	х	x	×
2	020	VVV	VVV	٧V	٧	٧	х	x	×
2	022	vvv	VVV	VVV	v٧	vv	v	٧	×
2	024	VVV	VVV	VVV	VVV	٧VV	٧VV	٧v	V

Source: Dr. Muhammad Nawaz, ABB, ESCDERC 2016 but modified

NEREID WORKSHOP BERTINORO OCT 2016

Trends... SiC Packaging

Technical Trends in SiC

Innovative Modul Design

- Full Bridge Busbar SiC-Modul
- Technologies
 - Chip on Busbar
 - Double Side Silver Sintering
- Module Data
 - max. 80A / 600V (1200V)
 - SiC-FETs
 - Silicium Puls Capacitors
 - Ultra Low Inductance

Concept

- Modular: H-/Half Bridge
- Double Side Cooling
- Small Dimensions







Current trends in industry (Infineon)



GaN HEMTs available configurations

CASCODE GaN

- Suitable for standard gate drivers
- Low Vf body diode
- Not ideally suited for multi-chip solutions
- Not scalable to low voltage
- Complex balance between the two chips



ENHANCEMENT MODE GaN

- Excellent for hard and soft switching topologies
- TurnON and TurnOFF optimized
- Needed for LV applications
- Key for integration at chip and/or package level



Infineon is focusing on Emode GaN for all consumer and industrial applications, with the most robust and performing concept in the market

Current trends R&D (imec GaN Program)



HIGH LEVEL PLAN OF GAN TECHNOLOGY AT IMEC TARGETING SHORT AND LONG TERMS NEEDS OF GAN



Current trends R&D (imec GaN Program)



NOVEL CONCEPTS

RewerBase

Advanced substrates	Higher level of integration	Novel device concepts
 Advanced substrates Increased yield Reduced defect density Increased buffer thickness E.g. CTE matched poly-AIN substrates Thinner substrate Equivalent GaN buffer strength 	 Integration of high side and low side switches Further cost reduction of the GaN technology Reduction of interconnect parasitics (enable higher switching speed) High-side/low-side isolation achieved by trench isolation. 	 Novel device concepts to improve device performance or enable novel applications for next generation GaN devices. E.g. 200mm (semi-)vertical devices. Preparation of vertical device technology and process modules in a CMOS compatible fab
10° 200 400 600 800 1000 1200 Lateral Voltage [V]	$\frac{GaR}{Si (111)} \frac{10^{-3}}{Si (100)} \frac{10^{-3}}{V_{G}} \frac{10^{-4}}{V_{G}} 10^{-4$	pGaN (channel) n- GaN (drain)



UWBG--Ga₂O₃ : $E_c = 8MV/cm$

- Substrates by Edge Fed Growth idem to Sapphire. The only WBG material that can be grown from the melt (low cost, DD<10⁴ cm⁻²). Low thermal conductivity. No p-type doping.
- Epi by HVPE, MOCVD, MBE (β-Ga2O3) or MIST epitaxy (α-Ga2O3)
- Currently at 2" (cots). Expected 4" in 2018, 6" in 2022.
- Very good n-type doping control with very low resistivity.
- Publications on first 600V <u>Schottky</u> diodes and Transistors



3), \$44,0, \$44,0, \$54,0, \$54,0, \$54,0, \$54,0, \$54,0, \$54,0, \$54,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0, \$56,0

4 in. (201)





FIG. 5. The breakdown voltages of Ga₂O₃ finFETs with $L_G = 2 \mu m$ and $L_{GD} = 16$, 21 μm while biased in the off-state at $V_{GS} = 0$ V. The inset shows the transfer characteristics of the same device indicating a $V_{TH} = +0.8$ V.





- Widebandgap semiconductors will cause a paradigm shift in power electronics design
 - SiC is the main contender for high voltage applications
 - GaN for medium voltage (600-1200V)
- System level will need to adapt
 - Novel, low inductive packages with excellent cooling properties
- Higher level of integration of power electronics with control logic
 - Co-integration