SiNANO-NEREID Workshop:

Towards a new NanoElectronics Roadmap for Europe

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WP3/Task 3.1: Nanoscale FET

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Introduction: technologies/concepts covered by the Roadmap

Nanoscale FET challenges defined by application needs:

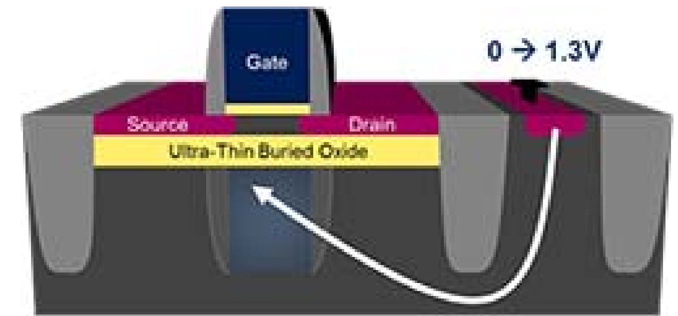
- High performance
- Low/very low static and dynamic power consumption
- Device scalability
- Variability
- Low cost

Technologies & concepts covered by the roadmap so far:

- Fully Depleted SOI FETs
- FINFETs
- Gate-All-Around (GAA) FETs
- Sequential 3D integration
- Non-charged based memories
- Modeling techniques
- Characterization

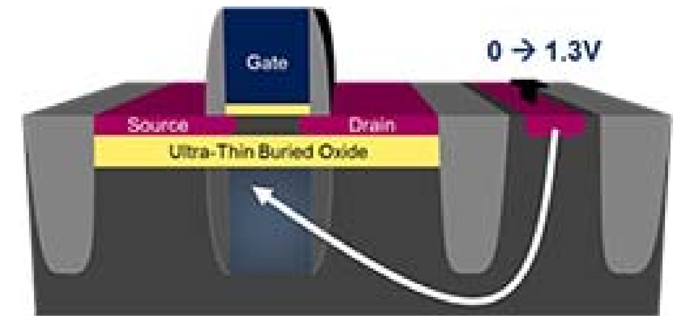
Scientific/technological highlights: FDSOI FETs

- Key research areas
  - Improving performance sub 14nm node
  - Improving electrostatic control for sub 14nm node
  - Evolution to multi-gate structure (e.g. nanosheet)
  - Design evolution exploiting back-bias techniques
  - Evolution to new materials (Ge and III-V on insulator)
  - FDSOI logic & embedded flash memories for micro-controller & automotive applications
  - Electrical characterization of small scale devices (transport, capacitances, local strain impact)



- Potential for application needs and impact for Europe
  - Ultra-low power devices for IoT
  - Harsh environment-resistant devices
  - FDSOI Logic & embedded flash memories for micro-controller applications / Automotive applications
  - FDSOI development for Analog and RF applications and integration with bipolar devices for high speed devices
  - Application of FDSOI for Innovative sensors (use of FDSOI design for sensing)
  - Beyond CMOS devices co-integration w/ CMOS (Quantum devices – eg: Qbit)
  - FDSOI for neuromorphic circuits design challenges

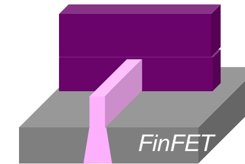
Scientific/technological highlights: FDSOI FETs



- Technology and design challenges
  - Integration of Strained SOI substrates: processing of tensile strain for NMOS & compressive strain for PMOS
  - Compatibility with flash memories process (as e.g. in BEOL)
  - FDSOI design for ultra-low power (Vdd<0,4V)
  - Evolution of FDSOI co-integrated with Tunnel FET option
  - Thermal management/self-heating mitigation incl. with 3D integration
  - Integration with new materials (SiGe, High Ge content) and future III-V materials (logic applications)
  - New material for differentiator: III-V OI for photonics
- Figures of merit
  - Ieff/Ioff (differentiated through options)
  - Variability /Avt (,0.8 mV um)
  - Vdd (<0.6V)
  - Subthreshold slope (<65mV/dec)
- Other issues and challenges, and interaction with other Tasks/WPs.
  - Link with WP2: enabler for neuromorphic computing/quantum computing
  - Link with WP4: sensors+ cmos co-integration enabler
  - Link with WP5: need for understanding system level benefit of 3D sequential options
  - Link with WP6: development of strain silicon layers, low T processes, wafer bonding for new material on insulator, low temperature epi, gate stack materials/interfaces development for low T for 3D technologies and new materials integration

Scientific/technological highlights: FINFETs

Key research areas



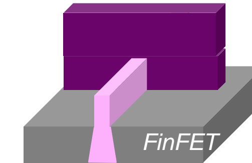
- subthreshold slope control to less than 70mV/dec at very short gate length (<14nm)
- improved device performance (Ion/Ieff at given Ioff) while scaling the gate length and pitch
- control of parasitic capacitances and resistances at scaled dimensions
- Variability control at very scaled dimensions
- innovation needs to continue in the following areas: contact resistivity, conformal doping, dopant activation above solid solubility limit, low k or air spacer; HKMG scaling and multi-Vt; high mobility channels; channel strain enhancement; integration of taller fins;
- understand under what conditions GAA will outperform finfets;
- Co-integration with other device architectures or between 2 channel materials
- 3D sequential integration with other devices

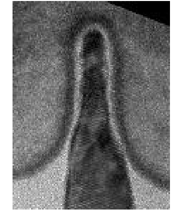
Potential for application needs and impact for Europe

- Current workhorse device for Si CMOS technologies
- Current best option for high performance space
- Currently can cover part of the low power/low cost space
- Considered for quantum computing as qbits
- Specialty sensors

Scientific/technological highlights: FINFETs

- Technology and design challenges
  - No single device/material able to replace Si CMOS; Co-integration of finfet with other device architectures or between different channel materials will be key
  - Improve finfet analog performance

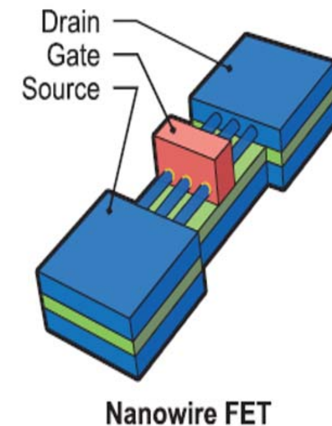




- Figures of merit
  - I_{on}, I_{eff}, CV/I (20% improvement every 2-3 years)
  - Subthreshold slope (< 80 mV/dec)
  - min achievable $I_{off,}$, GIDL (< 10 pA/um)
  - Avt (< 0.8 mV um)
- Other issues and challenges, and interaction with other Tasks/WPs.
  - Link with WP6: manufacturing processes and integration will become very complex; working with increased aspect ratios will be key; see key research areas
  - Link with WP5: system level studies to decide what are the best devices to be co-integrated and in what way, for a given application

Scientific/technological highlights: NW FETs

- Key research areas
  - What performance (I_{on}, I_{off}, g_m, f_t/f_{max}, NF) can be achieved in different materials and geometries?
  - How can different materials/geometries be manufactured at large scale?
  - Evaluation of interface and dielectric quality from HCI and PBTI measurements
  - Investigations of variability for sub - 10 nm nanowire diameter/gate length transistors
  - Circuit/technology co-design (DTCO) in 3D transistor architectures

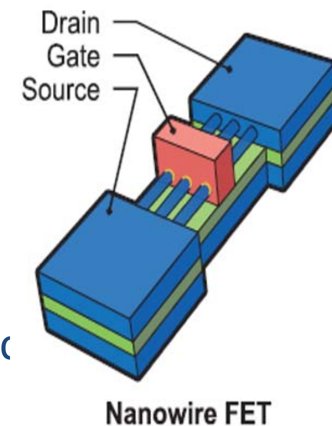


- Potential for application needs and impact for Europe
  - Extend the roadmap for CMOS scaling based on improved electrostatic control and increased drive current
  - Meeting the low-power demand for IoT applications
  - Enhance the CMOS RF-properties by (III-V) materials integration
  - Increase performance in mixed-domain by increase in f_t/f_{max}
  - Provide opportunity for efficient mm Wave front-ends combined with high-speed digital logic
  - Electrostatic control provided by nanowires/nanosheets architecture critical for TFET implementation

Scientific/technological highlights: NW FETs

❖ Technology and design challenges

- Challenges in terms of 3D processing in complex geometries at ~10 nm L_g
- Evaluation and reduction of parasitics in 3D transistors at ~10 nm L_g
- Understanding and reduction of thermal effects in 3D transistors at 10 nm L_g (heating, reliability …)
- Strain engineering (processing, characterization etc) at the 10 nm length sc
- 3D vertical transistor stacking to reduce area (vertical/lateral channels)
- Strategies for co-integration of various types of transistors (Si, Ge, III-V, CNT) in manufacturable CMOS processes
- Transistor and circuit co-design and optimization (DTCO) in complex 3D structures



❖ Figures of merit

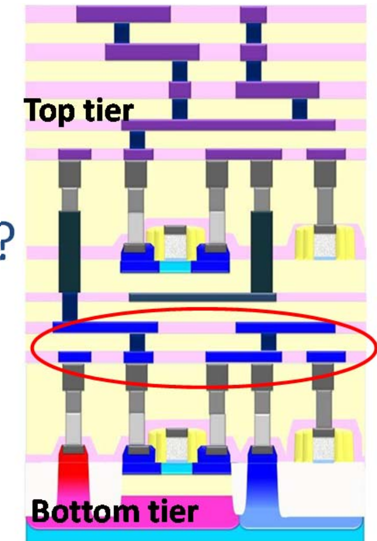
- I_{on}, I_{off}, gm, ft, fmax
- Subthreshold slope
- Avt

❖ Other issues and challenges, and interaction with other Tasks/WPs.

- Link with WP6: manufacturing processes and integration will become very complex; working with increased aspect ratios will be key;

Scientific/technological highlights: Sequential 3D

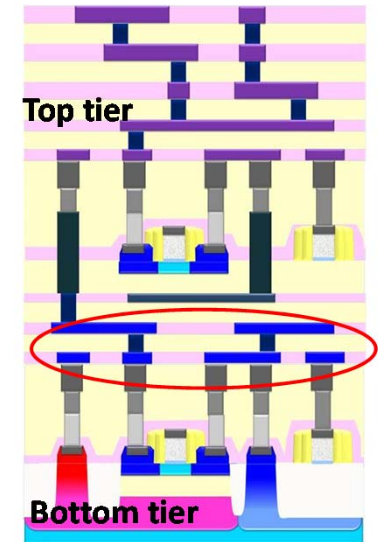
- Key research areas
  - Which application will benefit from very high density interconnections?
  - How to enable ultra-fine grain interconnections between layers?
  - Thermally stable metallization, with low resistance
  - Reliability for low T gate stacks
  - Low thermal cycle device performance
  - Test methodology



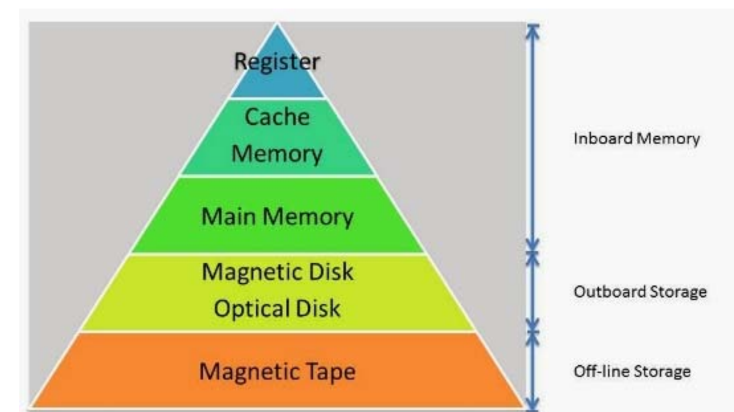
- Potential for application needs and impact for Europe
  - CMOS-on CMOS for area scaling
  - Imagers co-integrated with Logic
  - Compute in memory
  - Sensors on CMOS for IOT
  - Beyond CMOS devices co-integrated with CMOS

Scientific/technological highlights: Sequential 3D

- Technology and design challenges
  - Design tools optimized for Sequential 3D not available
  - Reducing parasitics in each implementation
  - Thermal management/selfheating mitigation
  - Manufacturing challenges
- Figures of merit
  - Top tier/bottom tier device performance and reliability
  - Contamination management
  - System level performance vs. 2D & 3DTSV
  - System level area vs 2D or 3DTSV
  - System level cost comparison vs. 2D or 3DTSV including yield
  - Multi tier stacking
- Other issues and challenges, and interaction with other Tasks/WPs.
  - Link with WP2: enabler for neuromorphic computing/quantum computing
  - Link with WP4: sensors+ cmos co-integration enabler
  - Link with WP5: need for understanding system level benefit of 3D sequential options
  - Link with WP6: development of low resistance, thermally stable BEOL materials; low T processes: wafer bonding, epi, gate stack materials/interfaces development for low

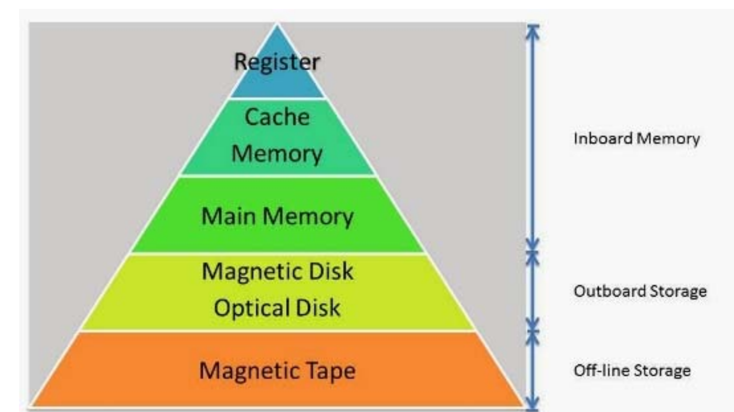


Scientific/technological highlights: Non-Charge based memories



- Key research areas
  - OxRAM:
    - HRS distribution reduction
    - Operation energy reduction
  - CBRAM:
    - Increase of endurance
    - Increase of data retention
  - MRAM:
    - complex magnetic stack integration
  - PCRAM:
    - reduce erase current
    - increase data retention
  - FeRAM (FeFET)
    - Increase of Vt
- Potential for application needs and impact for Europe
  - Embedded:
    - integration at scaled node <28nm
    - scaled SoC
    - automotive application(but spec needs to be demonstrated)
    - IoT
  - Security applications (embedded security)
  - SCM:
    - Applications on PC, tablet, phones, consumer markets
    - High speed computation
    - Fast boot
    - Recovery after power loss
    - Computing in memory

Scientific/technological highlights: Non-Charge based memories



Technology and design challenges

- MRAM:
  - Scalability is main challenge. 14nm can be reached with material engineering. Below 14nm , a new cell structure is required. Increasing the number of interfaces to stabilize the magnetic polarization.
- OxRAM and CBRAM
  - Need to confine CF. work on the cell encapsulation and interfaces.
  - New designs on system level can open new (niche) market. Ex: IoT (this can be a mainstream), neuromorphic, TCAM, NV-DRAM, memory computation…
- PCM
  - Need for cell thermal confinement→ GST etching required. 2 research axes: 1. Materials improvement for quicker write/erase and 2. Improvement for higher thermal stability (for embedded applications, 150C
  - However, crossbar will be necessary for density→ need for BEOL access diode

Figures of merit

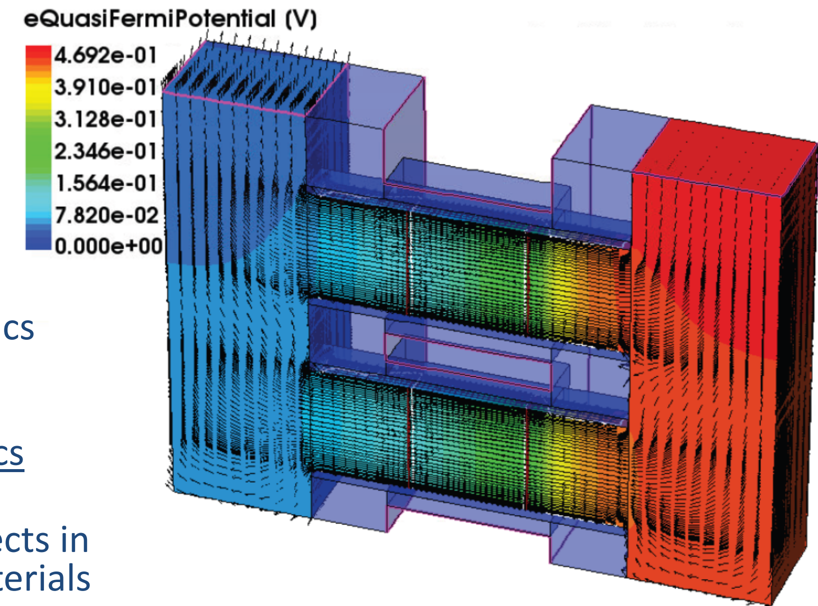
- SCM:
  - High Endurance
  - low Voltage
- Embedded:
  - Scalability
  - Low voltage and current
  - High retention

Other issues and challenges, and interaction with other Tasks/WPs.

- Link with WP3,4,5,6

Scientific/technological highlights: Modeling

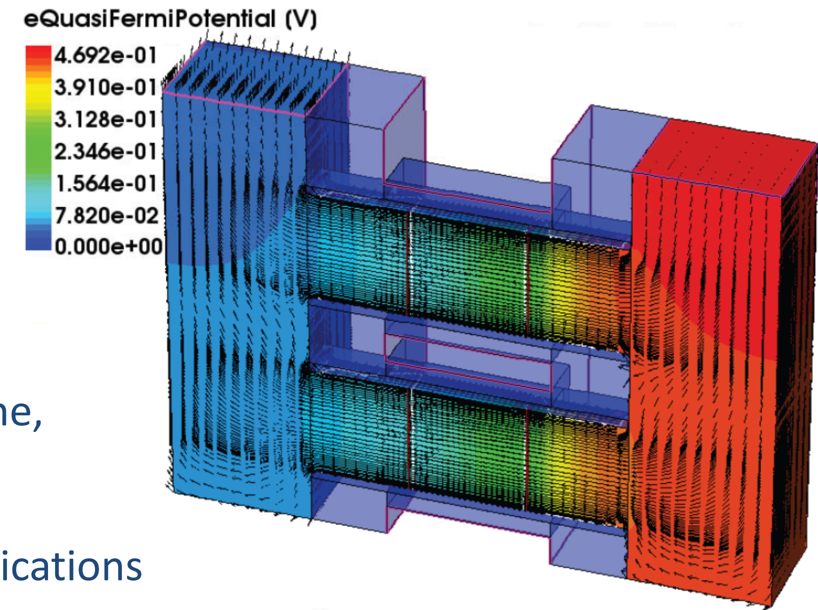
- Key research areas
  - Modelling full band structure of confined (2D, 1D) materials of interest to enable electrostatics and transport studies
  - Models suited to steer the selection of device architectures and of channel materials (FDSOI, FinFET, UTBB DG, GAA, NW, NSH, stacked NW, etc.)
  - Models of novel steep-slope device concepts for ULP electronics integrating new materials and suited for the selection of most promising options (attn: leakage)
  - Models for 3D vertical transistor stacking and related parasitics (resistances and capacitances)
  - Simulation of variability, fluctuations, impact of traps and defects in nanoscale devices in Silicon and in new channel/dielectric materials
  - Reliability modeling in new material systems (HCI, BTI, …)
  - Process modeling for new materials, support to DTCO



- Potential for application needs and impact for Europe
  - Accelerate development and strengthen competitive advantage in the field of ULP technologies
  - Modeling and simulation SMEs in Europe form a small but healthy ecosystem (GSS, GlobalTCAD, TiberTCAD, NextNano, Quantavis, QuantumWise, MDlab, etc.)
  - Modeling technology knowledge transfer from academia to llarge research laboratories and industry

Scientific/technological highlights: Modeling

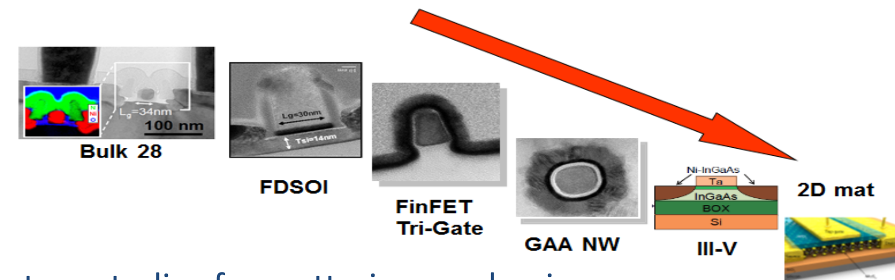
- Technology and design challenges
  - Model verification and experimental calibration at different levels of physical detail
- Figures of merit
  - Physical device dimensions and computational dimensionality of manageable problems (e.g.: length, cross section, volume, no. of materials, regions, atoms, number of eigenstates, number of particles, wall clock time, CPU time)
  - Ability to incorporate all relevant physics
  - Ability to achieve the degree of accuracy required by applications (device design, benchmarking of technologies, etc.)
  - Computational resources accessible to academic, research institute and industrial environments



- Other issues and challenges, and interaction with other Tasks/WPs.
  - Memory modelling
  - Automotive and Energy: Verified and calibrated models down to TCAD level for large bandgap materials (e.g. SiC, GaN, etc.)
  - Sensors: dependable simulation of analyte diffusion and transduction processes including statistical aspects

Scientific/technological highlights: Characterization

- Technology and design challenges
  - Specific test structures with multifingers necessary for increase device area especially for vertical NW with short channel features
  - In III-V gate stack, issue with border trap characterization by CV & Gw techniques on large area, LF noise proves efficient even on small area devices…
  - III-V & 2D materials channel transport properties: Hall effect test structure- Hall mobility vs effective mobility, low temperature studies for scattering mechanisms identification, LF noise, CV & Gw techniques, current DLTS, Fast IV for hysteresis analysis
  - Ferrolectric and negative capacitance MOSFET: challenge in polarisation assessment using specific test structure (conducting layer in between Cox and Cfe capacitance, cf Rusu 2012) or using standard Sawyer-Tower circuit providing polarization vs field characteristics, associated strain measurements should be desirable for piezo-Ferro materials…Intrinsic and parasitic Capacitances of nano MOSFETs: Challenge due to small capacitance values, solutions: use of multifinger MOSFET structures, use of RF CV technique based on S parameter measurements…
  - Strain/stress in nano MOSFETs: Challenge due to nanoscale probing along the channel for correlation to mobility enhancement using holographic TEM, HRTEM, NBED, PED, CBED techniques…
  - Interface quality and reliability related to initial and stress induced traps: Challenge due to small area of nano MOSFETs, device-to-device stochastic variations, solutions: use of multifinger MOSFET structures, use of dedicated techniques applicable to small area such as LF noise, AC transconductance, drain current DLTS, requirement for statistical measurements…
  - Variability in nano MOSFETs: Challenge due to requirement for statistical measurements, discrimination of local vs global variability sources, time dependent instability and dynamic variability measurements at µs to ns time scale, solutions: use of specific methodologies based on DC drain current variance analysis vs bias, use of addressable array structures for enhanced statistics, use of ultra-fast I-V measurements with specific test structures …
  - Self heating effect (SHE): Challenge due self heating arising from BOX, need for test structures for measuring channel temperature, discrimination of SHE impact on reliability…



Overall recommendations for T3.1

- Large gap in pipeline between manufacturable devices and emerging devices – identify new devices to fill the pipeline!
- For Nanowires, identify the best material and geometry options for logic (high-speed as well as low-power), develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar), and consider the 3D aspects of processing
- For FD SOI, develop differentiated options (RF, Embedded Memories, Imaging or molecules sensors) on FDSOI (applications for automotive, IoT, smart sensors…), ULP design (Vd<0,4V) for IoT market (wearable, medical…), and 3D integration for future neuromorphic and quantum computing approaches
- For FinFET, develop co-integration of different channel materials, low contact resistivity and high strain solutions, improve finFET analog performance
- For non-charge-based Memories, overcome the HRS broadening for OxRAM, improve the process for GST patterning for PCRAM, develop new materials enabling horizontal scaling
- For 3D sequential integration, define which applications will benefit from very high density interconnections (IOT, neuromorphic…), and develop a 3D place and route tool
- For Modelling/Simulation and Characterization, develop new tools taking into account all the new materials, technologies and device architectures in order speed-up technology optimization and reduce the cost of technology development.

Thank you!

Questions?