NanoElectronics Roadmap for Europe: Identification and Dissemination

3rd General Workshop

Sardinia, June 14-15, 2018

WP6

NEREID WP6

Task 6.1 Equipment and Materials

- **Processing tools and high quality materials** have been the **key enabling factors** in the evolution of Nanoelectronics. One of the major successes of ITRS has been the capability to insure the **timely availability of equipment and materials for the next technology node**, by insuring to manufacturers the long term visibility needed to allocate the R&D investments to guarantee the continuation of the Moore's Law.

- The objective of this task is to extend this benefit to the increased complexity and variety of technologies developed **not only for 'More than Moore' but also for nanoscale FET and Beyond CMOS**, covered in this European roadmap

- A close cooperation will be established between device and process developers, on one side, and equipment and materials supplier on the other side.

NEREID WP6

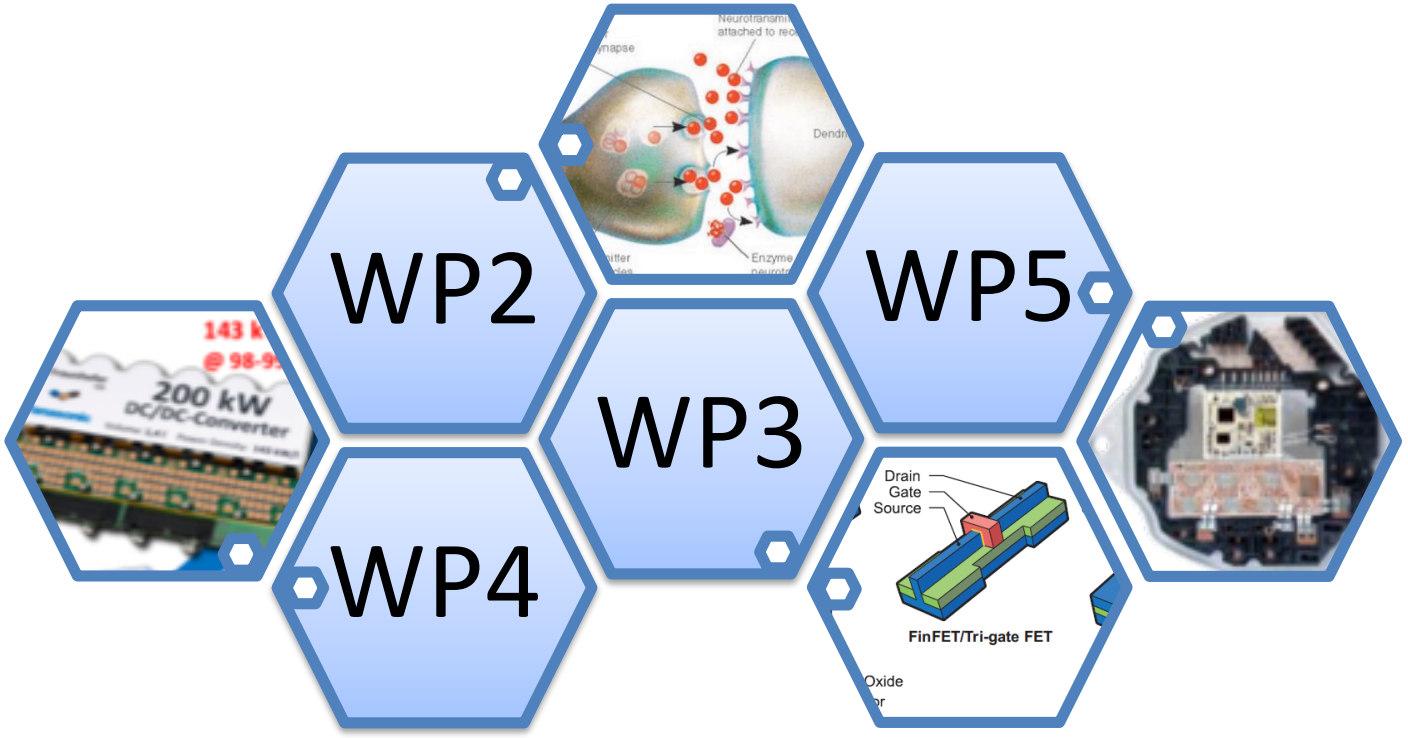
Task 6.2 Manufacturing Science

- The **scaling** down of the MOS transistor has driven the progress in the ICs **performance** and the **cost per function** of the devices has dropped accordingly.

- For complex devices, the **decrease of the cost per functions** is achieved by the **development of derivative options** on top of the core processes and the **integration of heterogeneous processes**. This leads to increasingly complex line management driven by **many process generations, multiple products with short life cycle and high variability** in terms of demand.

- The roadmap aims to activate a converging network of experience and competency involving the academic community for the development of new tools and methods for **fab productivity** needed to **increase efficiency** in the fab by managing **cycle time**, **advancing equipment and process control and yield enhancement** by providing a reference schedule.

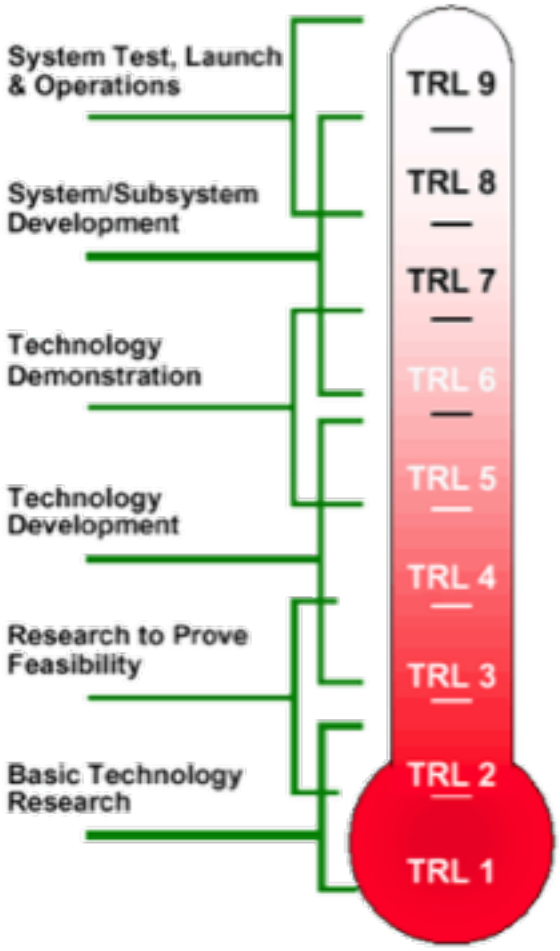
Before we start: WP6 working model



➔ WP6

Equipment & Manufacturing
(TRL over time)

Before we start: Technology Readiness Level



Source: NASA

European Commission

Technology Readiness Levels

TRL 0: **Idea**. Unproven concept, no testing has been performed.

TRL 1: **Basic research.** Principles postulated and observed but no experimental proof available.

TRL 2: **Technology formulation**. Concept and application have been formulated.

TRL 3: **Applied research**. First laboratory tests completed; proof of concept.

TRL 4: **Small scale prototype** built in a laboratory environment ("ugly" prototype).

TRL 5: **Large scale prototype** tested in intended environment.

TRL 6: **Prototype system** tested in intended environment close to expected performance.

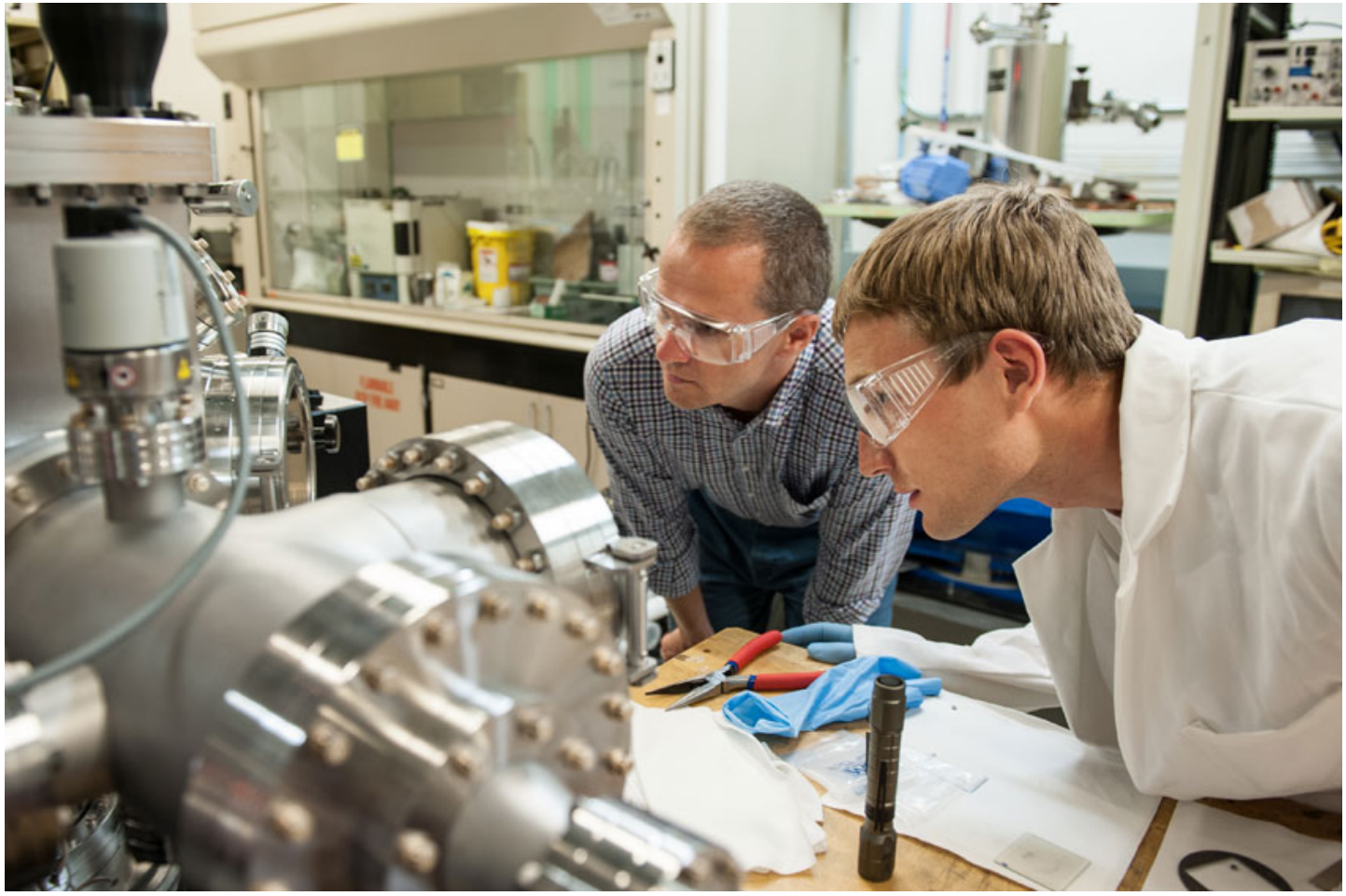
TRL 7: **Demonstration system** operating in operational environment at pre-commercial scale.

TRL 8: **First of a kind commercial system**. Manufacturing issues solved.

TRL 9: **Full commercial application**, technology available for consumers.

Source: European Commission

Before we start: Labratory Equipment



Source: NREL

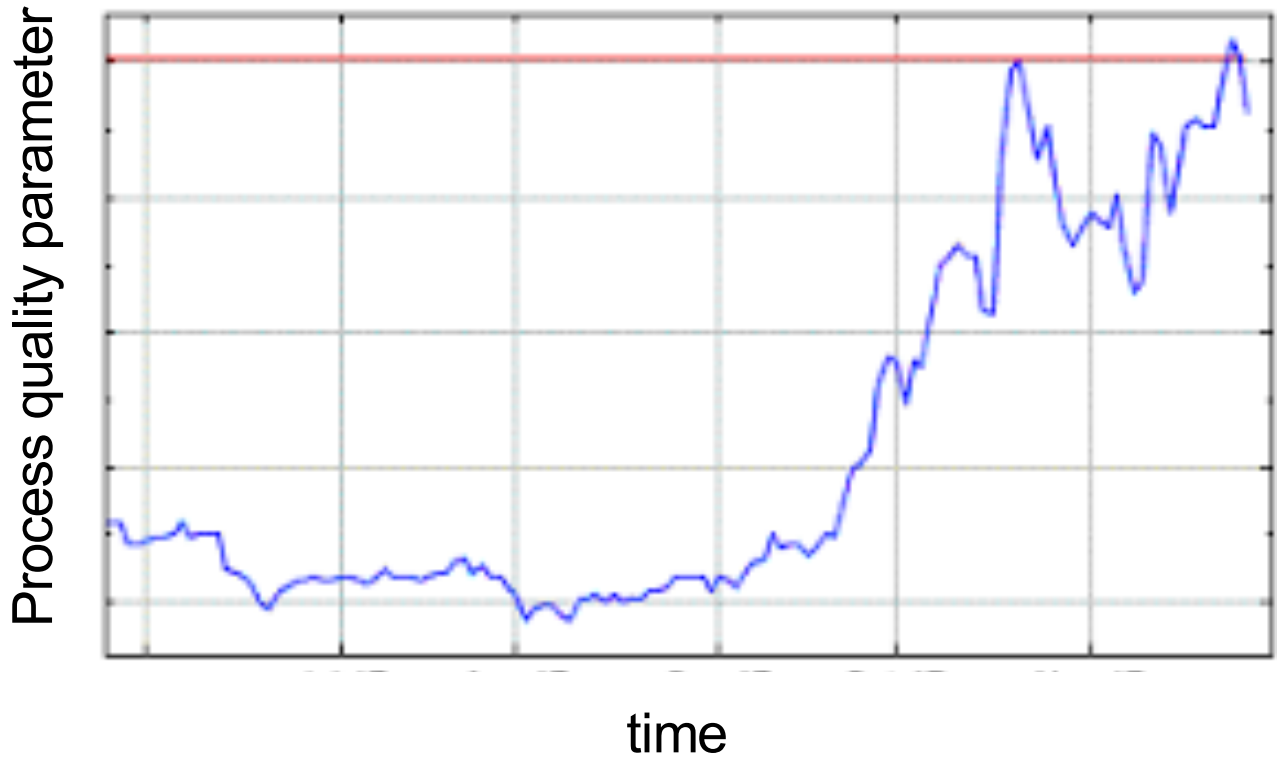
- TRL 4-6

Before we start: HVM Equipment

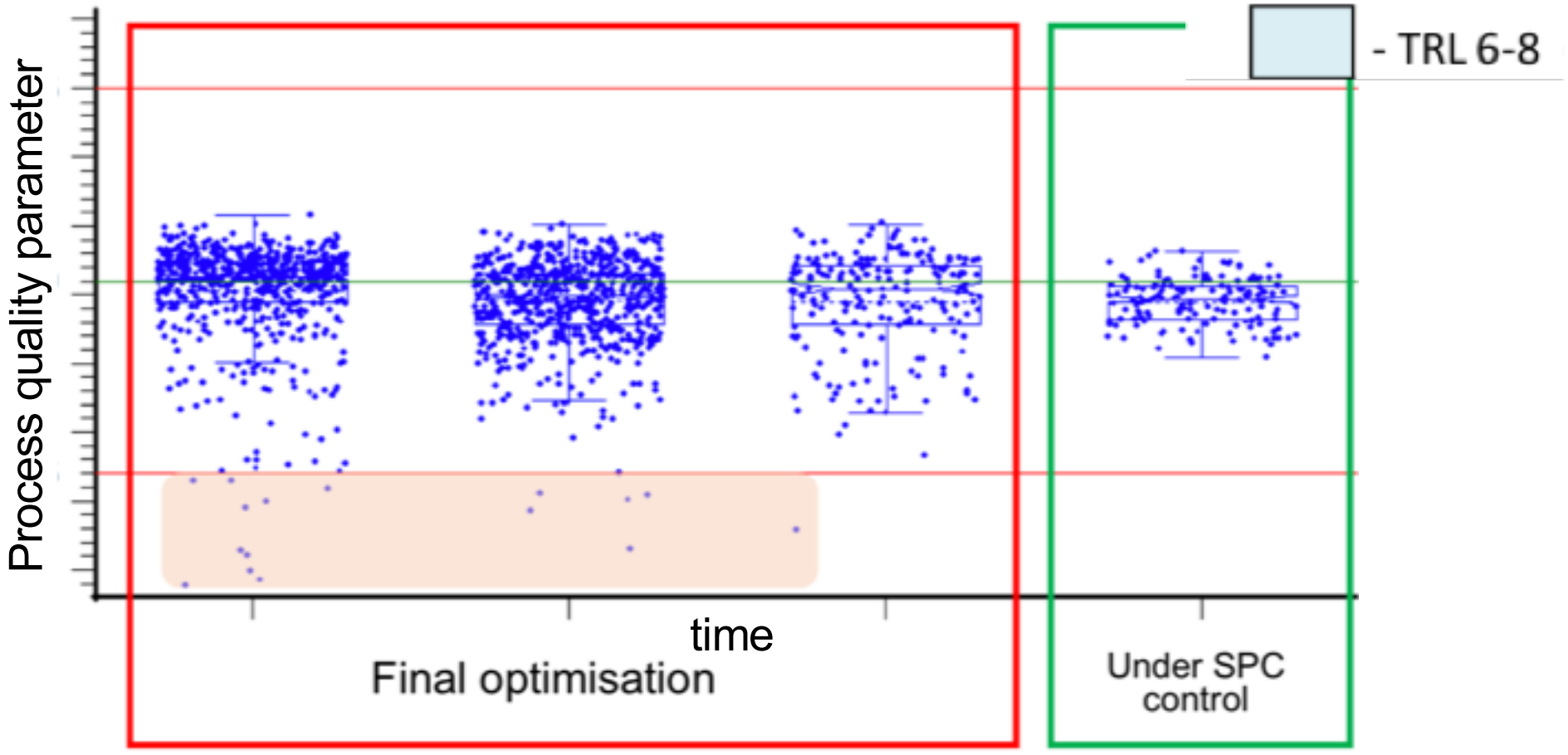
- TRL 6-8

Before we start: Proof of Concept

- TRL 2-4



Before we start: High Volume Manufacturing



Task 6.1 Equipment and Materials

NEREID WP6

Equipment, Materials and Manufacturing Science

	2023	2026	2029	2033
More Moore				
Conventional technology node semiconductor device & systems (WP3)				
Equipment & Materials for 7 nm node°				
• FinFET implementation >N7 / 12 nm FDx (Strained CMOS) in situ doped RSD (Gen2), dual STI				
• <N7 horizontal Gate-All-Around NW				
Equipment & materials for 5nm node°				
• <N5 Vertical GAA				
Equipment & materials for 3nm node °				
Equipment & materials for sub 3nm node °				
Technologies				
Si based technology				
Si(Ge) to Ge				
III/V				
FDSOI				
Nanowires				
3D Sequential				
Advanced Surface Passivation / defect passivation (new materials, scaled technologies)				
Interconnects				
Advanced low-k to airgap				
Cu based (including liner / barrier)				
Beyond Cu metallization				

- TRL 2-4 (Technology Readiness Level; applied research - validation in laboratory environment)

- TRL 4-6 (validation in laboratory ennvironment - demonstration in relevant environment)

- TRL 6-8 (demonstration in relevant environment - prototyping in an operational environment qualified)

NEREID WP6

Equipment, Materials and Manufacturing Science

	2023	2026	2029	2033
More Moore				
Material / thin film growth				
Conventional semiconductor technologies				
2D materials				
Spin based materials / stacking				
Patterning				
Area Selective Deposition				
Area Selective Etching				
EUVL				
DSA based lithography				
Metrology				
Materials and contamination analysis				
CD and overlay				
3D metrology (physical and chemical parameters)				
Film thickness				
Metrology requirements for system integration				

- TRL 2-4 (Technology Readiness Level; applied research - validation in laboratory environment)

- TRL 4-6 (validation in laboratory ennvironment - demonstration in relevant environment)

- TRL 6-8 (demonstration in relevant environment - prototyping in an operational environment qualified)

NEREID WP6

Equipment, Materials and Manufacturing Science

2023	2026	2029	2033

More Moore

Beyond CMOS & new compute paradigm options down-select and implement (WP2)

- Spin transistors, Steep sub-Vt slope (FeFET, TFET, NEMS) alternative materials: TMD's, others
- Neuromorphic and quantum computing

Equipment, Materials, Metrology & inspection for Beyond CMOS & new compute paradigm options

- Tunneling FET (conventional materials)
- Tunneling FET (2D materials)
- from charge based to spin based

Memory systems incl. new storage architecture for smart systems, IoT and new compute paradigm

- STT- MRAM/ ReRAM/ PCM / other

- TRL 2-4 (Technology Readiness Level; applied research - validation in laboratory environment)
- TRL 4-6 (validation in laboratory ennvironment - demonstration in relevant environment)
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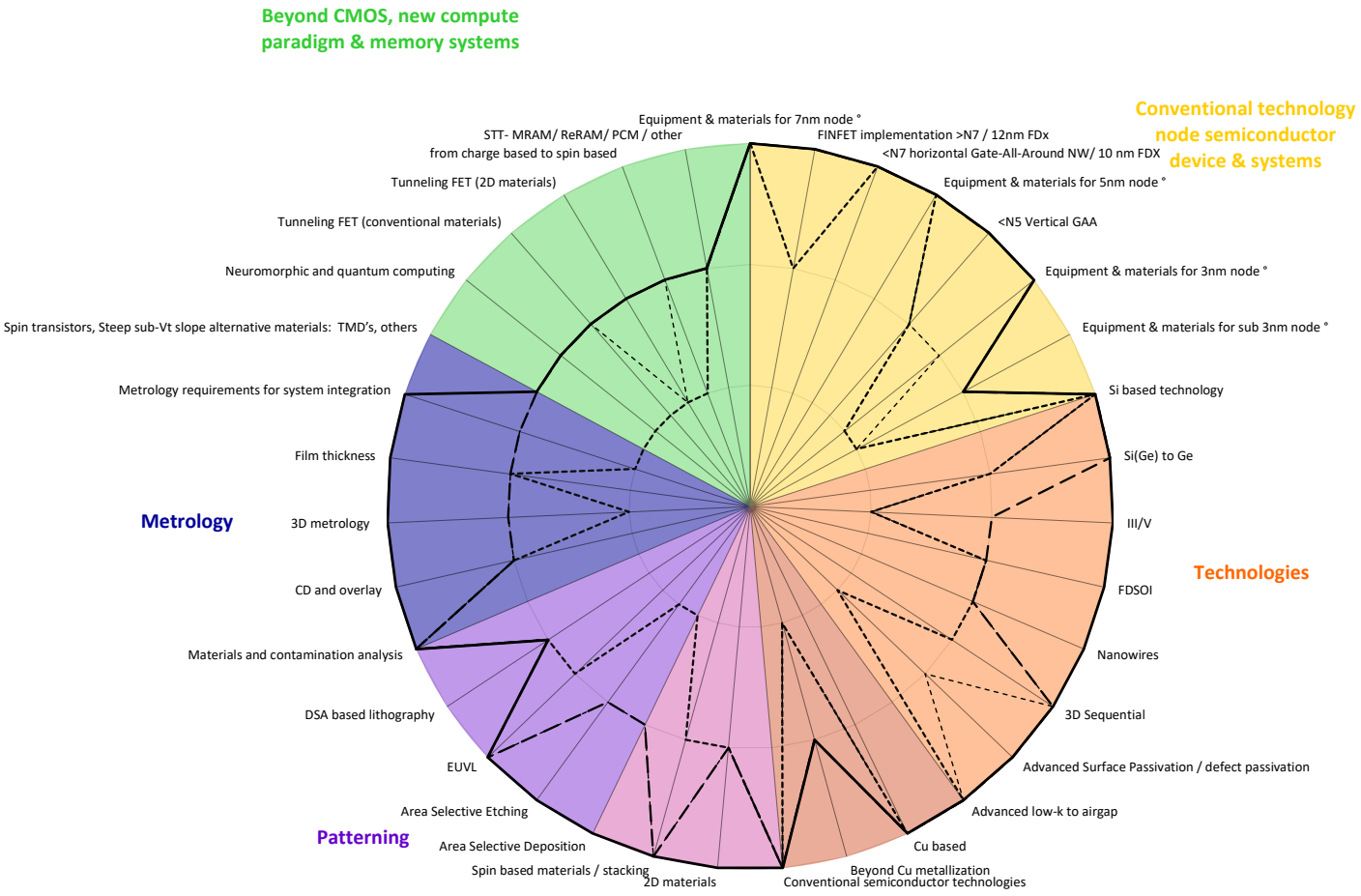
NEREID WP6


Beyond CMOS, new compute paradigm & memory systems
Conventional technology node semiconductor device & systems
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FINFET implementation >N7 / 12nm FDx
<N7 horizontal Gate-All-Around NW/ 10 nm FDX
Equipment & materials for 5nm node °
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Si(Ge) to Ge
III/V
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from charge based to spin based
Metrology
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Technologies
Material / thin film growth
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2023
2026
2029
2033

NEREID WP6

Equipment, Materials and Manufacturing Science

2023	2026	2029	2033

More-than-Moore

Process technology for the applications (WP4)

Technology platform for integrated application defined sensors, including packaging
CMOS integration, compatibility and readout circuit
Multi-parameter sensing
Manufacturability /sensing functionality and micro-pumps
Autonomous sensor systems
Role of new materials and nanostructures in sensing (vs. Mature CMOS sensors)
System-in-package (SiP) sensors
Energy harvesting
Equipment & Materials for integrated application defined sensors, including packaging
Assembling testing, metrology and calibration
Materials and contamination analysis
Equipment & Materials for biomedical devices for minimally invasive healthcare
Maturity level
Packaging
Safety / Security
Miniaturization / form factor
Biocompatibility
Enhanced process technology platforms for power electronics

- TRL 2-4 (Technology Readiness Level; applied research - validation in laboratory environment)

- TRL 4-6 (validation in laboratory ennvironment - demonstration in relevant environment)

- TRL 6-8 (demonstration in relevant environment - prototyping in an operational environment qualified)

NEREID WP6

Equipment, Materials and Manufacturing Science

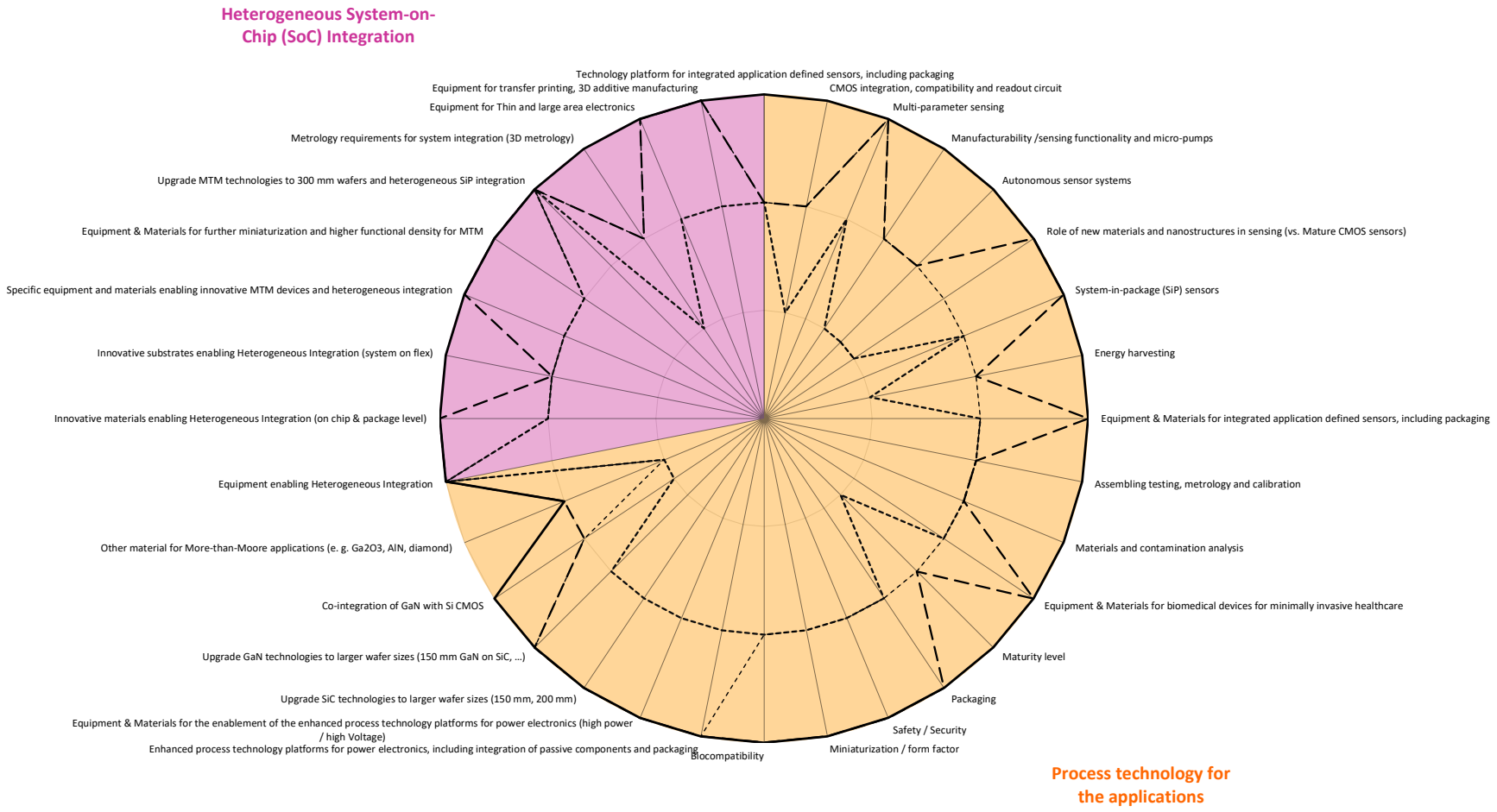
	2023	2026	2029	2033
More-than-Moore				
Process technology for the applications (WP4)				
Equipment & Materials for the enablement of the enhanced process technology platforms for power electronics				
Upgrade SiC technologies to larger wafer sizes (150 mm, 200 mm)				
Upgrade GaN technologies to larger wafer sizes (150 mm GaN on SiC, …)				
Co-integration of GaN with Si CMOS				
Other material for More-than-Moore applications (e. g. Ga2O3, AlN, diamond)				
Heterogeneous System-on-Chip (SoC) Integration (WP5)				
Equipment enabling Heterogeneous Integration				
Innovative materials enabling Heterogeneous Integration (on chip & package level)				
Innovative substrates enabling Heterogeneous Integration (system on flex)				
Specific equipment and materials enabling innovative MTM devices and heterogeneous integration (e. g. 3D handling, flip chip accuracy, etc.)				
Equipment & Materials for further miniaturization and higher functional density for MTM				
Upgrade MTM technologies to 300 mm wafers and heterogeneous SiP integration				
Metrology requirements for system integration (3D metrology)				
Equipment for Thin and large area electronics				
Equipment for transfer printing, 3D additive mnufacturing				

- TRL 2-4 (Technology Readiness Level; applied research - validation in laboratory environment)

- TRL 4-6 (validation in laboratory ennvironment - demonstration in relevant environment)

- TRL 6-8 (demonstration in relevant environment - prototyping in an operational environment qualified)

NEREID WP6


Heterogeneous System-on-Chip (SoC) Integration
Technology platform for integrated application defined sensors, including packaging
CMOS integration, compatibility and readout circuit
Multi-parameter sensing
Manufacturability /sensing functionality and micro-pumps
Autonomous sensor systems
Role of new materials and nanostructures in sensing (vs. Mature CMOS sensors)
System-in-package (SiP) sensors
Energy harvesting
Equipment & Materials for integrated application defined sensors, including packaging
Assembling testing, metrology and calibration
Materials and contamination analysis
Equipment & Materials for biomedical devices for minimally invasive healthcare
Maturity level
Packaging
Safety / Security
Miniaturization / form factor
Biocompatibility
Enhanced process technology platforms for power electronics, including integration of passive components and packaging
Equipment & Materials for the enablement of the enhanced process technology platforms for power electronics (high power / high Voltage)
Upgrade SiC technologies to larger wafer sizes (150 mm, 200 mm)
Upgrade GaN technologies to larger wafer sizes (150 mm GaN on SiC, ...)
Co-integration of GaN with Si CMOS
Other material for More-than-Moore applications (e. g. Ga2O3, AlN, diamond)
Equipment enabling Heterogeneous Integration
Innovative materials enabling Heterogeneous Integration (on chip & package level)
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Specific equipment and materials enabling innovative MTM devices and heterogeneous integration
Equipment & Materials for further miniaturization and higher functional density for MTM
Upgrade MTM technologies to 300 mm wafers and heterogeneous SiP integration
Metrology requirements for system integration (3D metrology)
Equipment for Thin and large area electronics
Equipment for transfer printing, 3D additive manufacturing
Process technology for the applications
2023
2026
2029
2033

Task 6.2 Manufacturing Science

NEREID WP6

Equipment, Materials and Manufacturing Science

2023	2026	2029	2033

Manufacturing Science

Environment, Safety, Health (ESH)

- Replacement materials (e.g. not based on Bi2Te3)
- Implementation of capabilities for utility reduction, such as support idle mode, improved scheduling and specific communication between host and equipment for energy savings

Productivity

- Improvement of fab productivity (cycle time, percentage NPW wafers, equipment availability, equipment utilization, yield enhancement, etc.)
- Supply chain integration

Automation

- Smaller lot sizes, mixed lots and single wafer factory operations
- Upgrade automation, APC and integration of new sensors and hybrid solutions
- Control of variability in manufacturing
- Advanced diagnostic and decision support systems (supervision, scheduling, agility, augmenting reactive with predictive, big data analytics)
- Real-time simulation support for optimized fab operations
- Knowledge management (inter fab flows, fast diagnosis)
- FICS migration towards distributed architecture BYOD/Apps
- Manufacturing data security considerations
- Manufacturing technology exploration for functional integra tion of novel materials (e.g. Graphene, TMD's, FerroElectric, e.a.) Implemented in existing pilot

YIELD

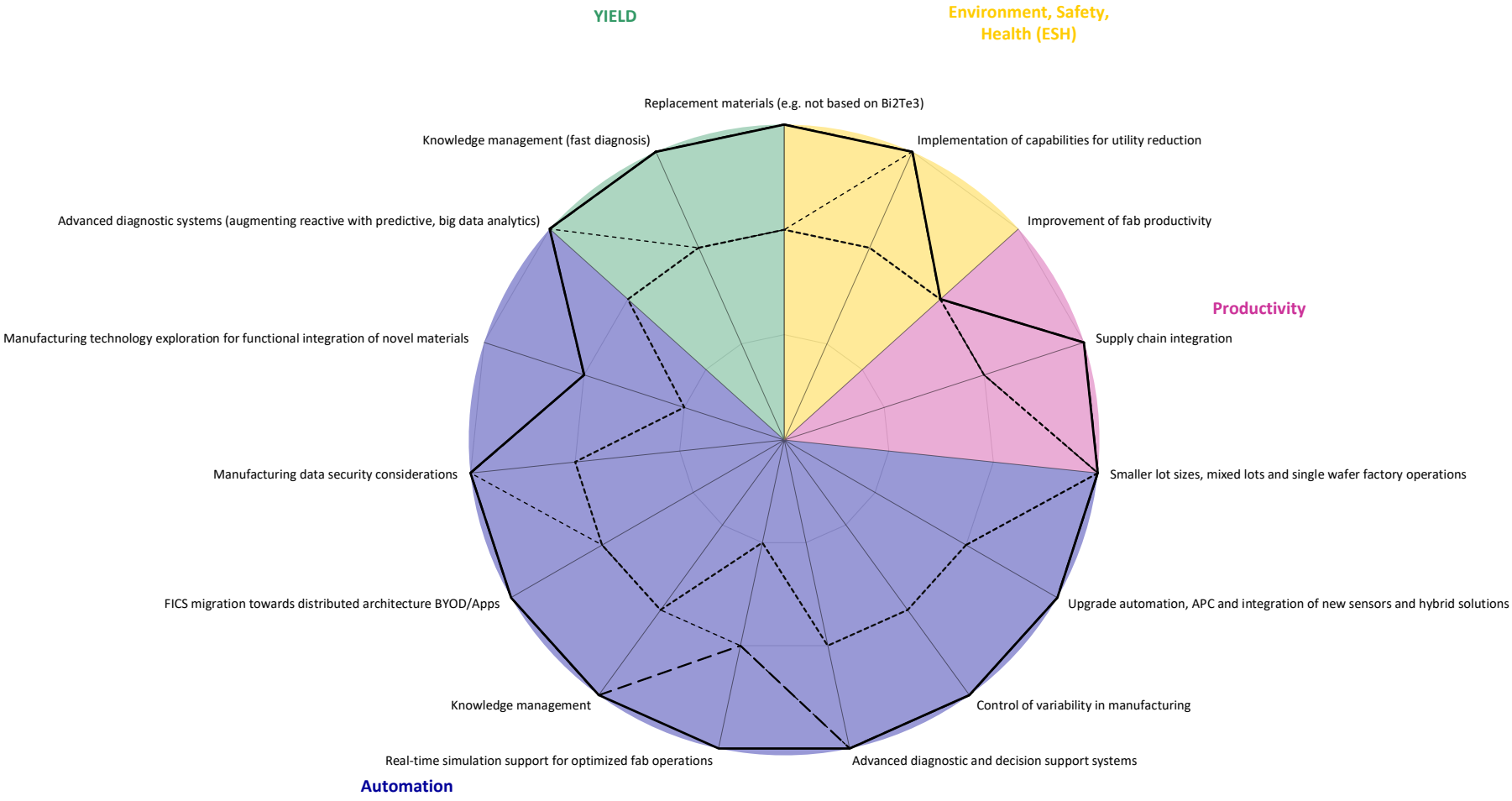
- Advanced diagnostic systems (augmenting reactive with predictive, big data analytics)
- Knowledge management (fast diagnosis)

- TRL 2-4 (Technology Readiness Level; applied research - validation in laboratory environment)

- TRL 4-6 (validation in laboratory ennvironment - demonstration in relevant environment)

- TRL 6-8 (demonstration in relevant environment - prototyping in an operational environment qualified)

NEREID WP6


YIELD
Environment, Safety, Health (ESH)
Replacement materials (e.g. not based on Bi2Te3)
Knowledge management (fast diagnosis)
Implementation of capabilities for utility reduction
Advanced diagnostic systems (augmenting reactive with predictive, big data analytics)
Improvement of fab productivity
Productivity
Manufacturing technology exploration for functional integration of novel materials
Supply chain integration
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Upgrade automation, APC and integration of new sensors and hybrid solutions
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Real-time simulation support for optimized fab operations
Advanced diagnostic and decision support systems
Automation
2023
2026
2029
2033

Conclusion: Main recommandations (1/2)

- Concurrent WP's (WP2 – WP5) were analyzing their domains in view of the presented applications and derive immediate and long-term requirements in terms of materials, processes and manufacturing needs.

- The feeling exists, that with the worldwide effort on materials, processes and manufacturing in the domain of More Moore, the imminent needs of European application domains is covered. However, more specific needs in the other NEREID domains were identified.

- In the WP6 roadmap activities were covered, where Europe is leading in terms of materials, processes and manufacturing, but where the demand from application side is stronger outside of Europe (e.g. EUV lithography equipment).

Conclusion: Main recommandations (2/2)

- Cover activities in WP6 where application wise Europe is leading, but where specific needs for materials, process and manufacturing require continued attention

- Synergies with ITRS/IRDS activities whenever possible, in particular for the section manufacturing science.

Acknowledgement

- Co-Leader: Stefan De Gent

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