NanoElectronics Roadmap for Europe: Identification and Dissemination

Sardinia, June 14-15, 2018

WP2 Beyond CMOS

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Outline

- **Introduction**
- **Methodology**
- **Beyond CMOS Technologies for the NEREID Roadmap**
- **Conclusions**
- **Recommendations**

Introduction

Objectives of WP2 'Beyond CMOS'

- To map the potential of Beyond CMOS devices for data processing.
- To perform case studies to identify potential designs and architectures for non-conventional approaches.
- To organise two Domain workshops to bring together experts and stake holders for discussions and conclusions.
- To carry out a survey on the integration potential, power consumption, speed, etc. of the selected case-study devices.
- To provide input to the road map and a chapter on Beyond CMOS.

Introduction

Areas of the current EU portfolio on Alternative Computing.

Category	Coverage
Quantum computing	Technologies to build qubits and transport information between them, including algorithmic and architecture
Molecular electronics	Solid-state information processing functions built on organic molecules including biomolecules; molecular spintronics
Spintronics	Spin-based electronics and related materials
2D materials	Carbon-based and transition metal dichalcogenides, as well as electronic and spintronic functions based on these
Extended & beyond CMOS	Non mainstream semiconductor transistors, including III-V materials, steep-slope devices, single electron transistors, etc.
Neuromorphic computing	Hardware implementation of neural networks, analogue and digital, architectures and applications

(From the presentation of Mr Eric Fribourg-Blanc in the second Beyond CMOS Workshop in May 2017)

Methodology

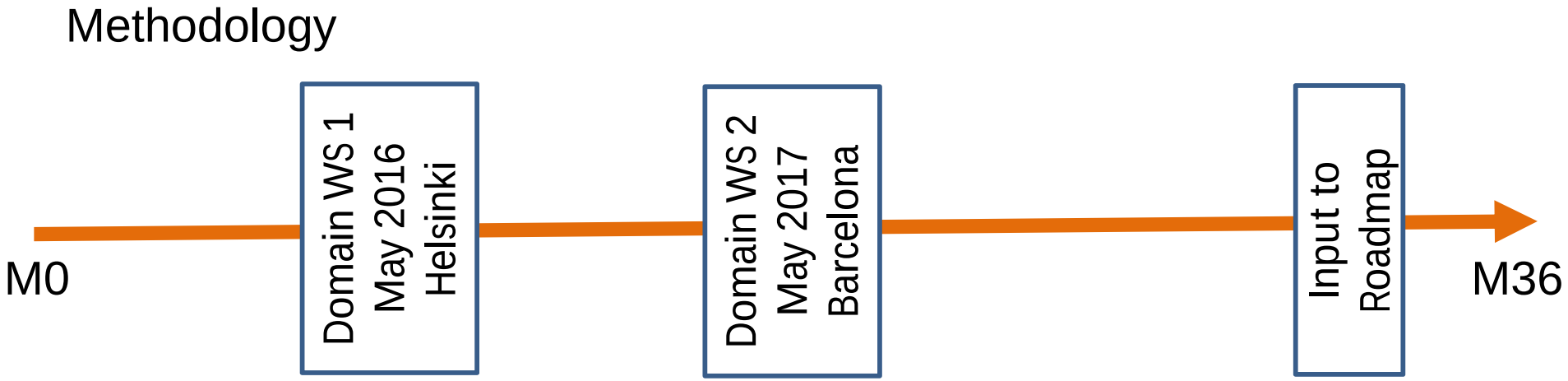
Deliverables

D2.1 Report on Domain Workshop 1 with emphasis on new physical state variables (M7)

D2.2 Report on selection of case studies for Domain Workshop 2 (M15)

D2.3 Report on outcome of Domain Workshop 2 (M18)

D2.4 Input to the Roadmap in the form of a Chapter for Beyond CMOS (M33)



1st WP2 Domain Workshop; Mapping of Technologies
16-17 May, 2018, Helsinki

Speakers and topics:

H. Riel, IBM: The future of computing
M. Esposito, U Luxembourg: Information thermodynamics
M. Heyns, IMEC: III/V and deep subthreshold devices for next generation CMOS technologies
M. Graziano, Polytechnica di Torino: A quantitative approach to Beyond CMOS potentials analysis
J. Åkerman, KTH,U Gothenburg: Spintronics meets magnonics-towards spin wave based neuromorphic computing
S. Thorpe, CNRS: Neuromorphic computing with spikes
B. Li, U Colorado: Phononics: prosessing information & computing with phonons
L. Colombo, U Gagliari: Some issues on thermal transport in 2D materials: the paradigmatic case of graphene
M. Costache, ICN2: Topological insulators and magnon spintronics
S. Volz, CNRS: Heat transport at nanoscale
A. Martinez, UP Valencia: Nano-optomechanics: playing with light and sound at the nanoscale
R. Enrstorfer, Max Plank Fritz Haber Institute: Dynamics of electrons, spins and phonons in transition metal dichalcogenides
M. Calame, U Basel: Does molecular electronics compute?

2nd WP2 Domain Workshop; Alternative Computing Paradigms
11-12 May, 2017, Sitges

Speakers and topics:

J. Barreto, U Bristol: Integrated quantum photonics for computation

W. Pernice, U Münster: Nanophotonics circuits for unconventional computing

J. Thigna, U Luxembourg: Thermoelectrics of quantum NEMS systems

B. Dieny, SPINTEC: Spintronics for low power computing

M. Costache, ICN2: Computation approaches with magnonics

M. Duranton, CEA: NeuRAM3 project Neuromorphic computation

S. Vassanelli, U Padova: RAMP project Real neurons-nanoelectronics Architecture with Memristive Plasticity

J. Åkerman, U. Gothenburg, KTH: Spin Hall nano-oscillator networks for neuromorphic computing

M. Rubi, U Barcelona: Heat transfer in small scales

S. Cotofana, TU Delft: Design of Brownian circuits

S. de Franceschi, CEA: MOS-QUITO project CMOS-based qubits

A. Ionescu, EPFL: Steep slope devices

Beyond CMOS Technologies

Criteria:

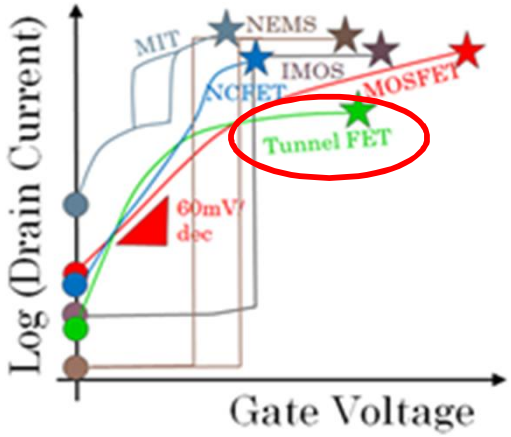
- **Potential for data processing**
- **Time scale ~10-15 years**

- Tunnel FETs
- Neuromorphic computing
- Spintronics
- Quantum photonics
- Thermal computing

Tunnel FETs

Opportunities

Various categories of Steep Slope Switches. (Courtesy of Prof. Adrian Ionescu, EPFL).

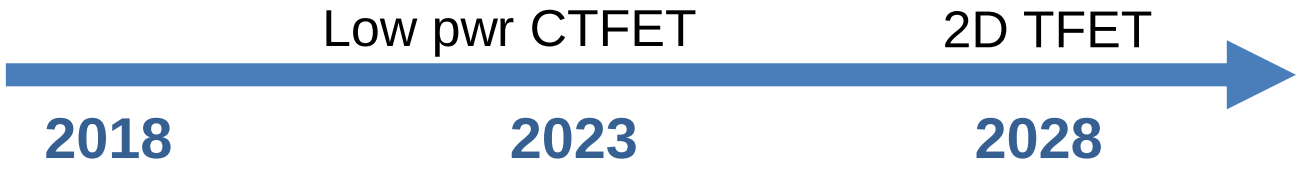


- Operation based on band-to-band tunneling
- Sub-thermionic subthreshold slope, S<60 mV/dec at RT
- Supply voltage scaling -> 0.2-0.3 V
- Low power consumption
- Von Neumann architecture applies -> compatible with current circuit designs
- 2D/2D TFET architecture
- Analog gain at low I/V

Tunnel FETs

Challenges

- Low I_{ON} -> Low operation speed
- Materials and interfaces (traps degrade the operation)
- Scaling may be an issue
- Design tools for TFET circuitry are missing



Neuromorphic Computing

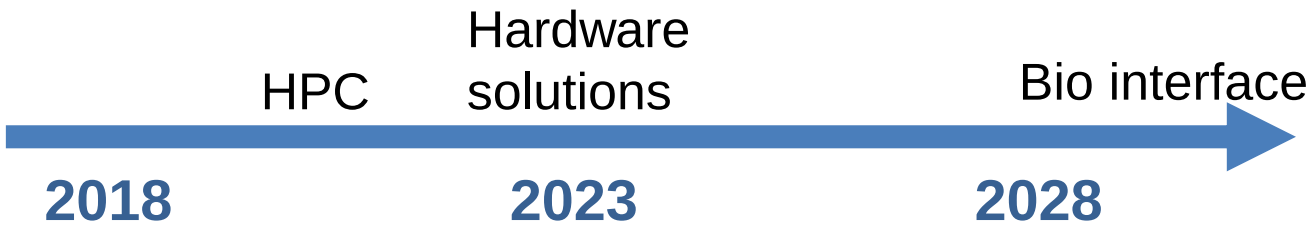
Opportunities

- Two approaches:
  - HPC + algorithms, pattern recognition, data mining
  - Specific hardware (digital, analog, mixed) with memory nodes
- Application specific operation
- Integration with CMOS platform, non-von Neumann architecture
- Low power, high efficiency (sub-fJ energy per bit possible)
- Supervised/unsupervised learning
- Fast pattern recognition (images, text, medical etc.)
- Photonic synapses (optical fibres + PCM synapses)
- Degrees of freedom: Weighting of input can be multilevel, parallel or serial
- AI and IoT

Neuromorphic Computing

Challenges

- Hardware development (CMOS neurons and PCM synapses, photonic synapses, spintronics, ...)
- Material issues, CMOS compatibility
- Non-von Neumann architectures, algorithms…
- Interfacing with current technology, protocols, programming…
- Understanding the information processing of biological entities



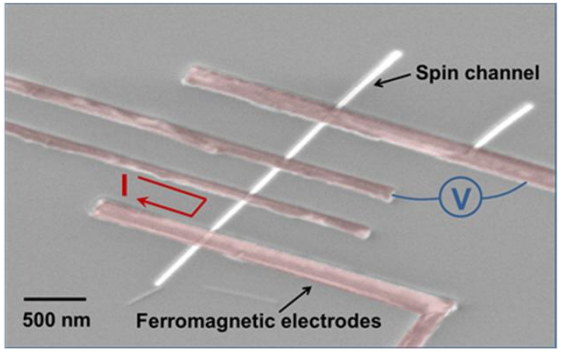
Spintronics

Opportunities

- Established technology for memories, STT-MRAM market growing
- Spins can be extra degrees of freedom in information processing
- Spin waves/magnons: No Joule heating, potential for THz operation
- Logic circuits have been demonstrated (switches, XNOR, majority gates)
- Fewer components, smaller footprint, low power consumption
- Neural networks have been demonstrated
- Tens of GHz microwave oscillators based on spin torque and spin Hall effect
- Topological insulators have potential for robust interconnects

Challenges

- Materials, interface and processing issues challenging
- Spin injection and read-out in spin FETs
- Magnetic field required in some cases
- Quantum resistance (25.8 kΩ) of topological insulators (parallel channels?)



SEM image of a spin-valve device in which the charge and spin currents are separated (Courtesy of Dr. Marius Costache, ICN2).

Quantum Photonics

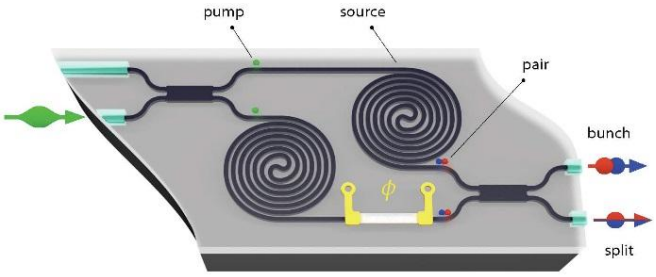
Opportunities

- Photons do not suffer from decoherence
- Silicon and III-V semicondutor technology platform exists
- 8-qubit processor demonstrated
- Secure data transfer (Quantum Key Distribution)
- Quantum Technology Flagship initiated in Europe
- Potential for photonic neuromorphics

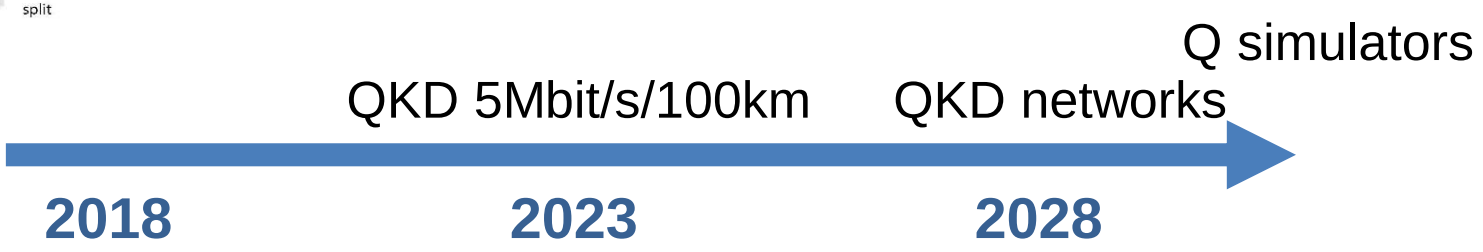
Quantum Photonics

Challenges

- Single photon detectors (APD, superconducting wires)
- Data transmission speed (~Mbit/s)
- Attenuation in optical fibres limit transfer distance (~100s of km)
- Development of repeaters
- QKD networks



Identical spontaneous four-wave mixing (SFWM) photon sources for quantum photonics (Courtesy of Dr. Joshua W. Silverstone, University of Bristol).



Thermal Computing

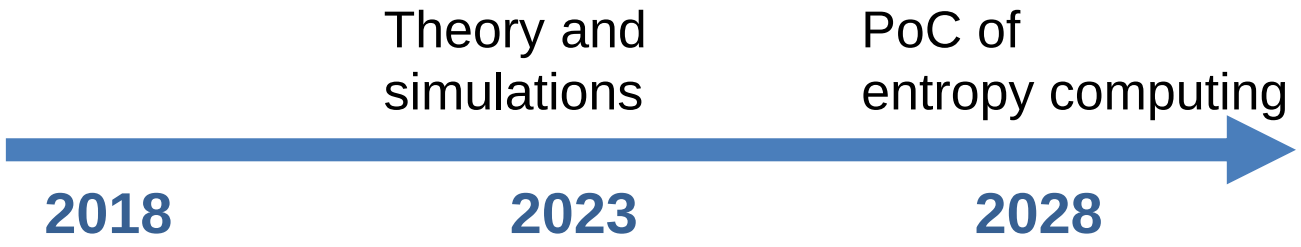
Opportunities

- Addressing the issues in thermal management of nanoelectronics (the “heath death”, “dark silicon”)
- Potential for low power computing (~$k_B T$)
- There are several approaches:
  - Optomechanics
  - NEMS based computing
  - Heat computing
  - Brownian/entropy computing (power from the environment)

Thermal Computing

Challenges

- How to implement the current nanophononics understanding to thermal management of nanoelectronics circuit design/architectures and materials
- Large part of the experimental work is still at low temperatures
- Need to develop the device structures and algorithms to control the energy/information flow
- Experimental proof of concept of Brownian/entropy computing



Conclusions

- There are several potential Beyond CMOS technologies suitable for information processing
- Many of these have also potential in sensor applications
- Most of the technologies are still in academic laboratories
- Europe is in good position to exploit the emerging technologies: Theoretical background is strong, experimental work at the highest level
- The ties between academia and industry have to be strengthen to make the best out of the strong academic potential
- There is a gap between the new ideas developed at universities and RTOs, and the European nanoelectronics industry, partially created by the division between the ERC (single PI, “science”) and “innovative” R&D (TRL mismatch, consortium-based)

General Recommendations

- Nanofabrication affects most of the emerging technologies impacting variability of critical dimensions and processing defects. Novel approaches are required for dimensional and compositional *nanometrology,* accompanied by a traceable measurement protocol and to-be-developed instrumentation.
- A critical issue for Europe with the majority of the Beyond CMOS and alternative computing concepts is the *low uptake or interest shown by industry*.
- One potential solution to enhance the interaction between academic and industrial actors towards improving communication, identification of gaps and priorities in emerging ICT technologies could be to add a significant bonus (funds or marks) to proposals which include TRL 2 to 3 research actions.
- The funding for TRL 1-2 level research should be doubled in LEIT ICT, given the large reduction of nanoelectronics TRL1-2 funding in FET.
- Look for alternative, more application-driven routes to capitalise the potential of Beyond CMOS ideas, structures and devices.

Feedback From the GW3 & Advisory Board

- To set up an ecosystem of universities and RTOs to identify the research priorities in TRL1-3 (foresight exercise) and find a way to discuss them with industry on regular basis (projects to establish a link with the SCC and meet more often?).
- To create instruments that support building an ecosystem of ICT-oriented projects which bridge the interests of academia and industry in Europe (a combination of MEL-ARI like project clusters of the ESPRIT program and the annual EFECS meetings?).
- To address the role of memories (the NEREID chapter complements the IRDS on Beyond CMOS which has extensive sections on memories and switches, a link between industry and academia?).

Acknowledgements

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- All the speakers, discussants and rapporteurs in the Barcelona Workshop