NanoElectronics Roadmap for Europe: Identification and Dissemination

3rd General Workshop

Sardinia, June 14-15, 2018

WP4 Functional diversification
Task 4.2 Smart Energy

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Task 4.2 Smart Energy

Industrial Co-Leader			
WP4	4.2 Smart Energy	W. Dettmann	Infineon
General and Domain Workshops			
WP4	4.2 Smart Energy	Mikael Östling	KTH
WP4	4.2 Smart Energy	Steve Stoffels	IMEC
Domain Workshops			
WP4	4.2 Smart Energy	Gaudenzio Meneghesso	UniPD
WP4	4.2 Smart Energy	Peter Moens	On Semi
WP4	4.2 Smart Energy	Joff Derluyn	EpiGaN
WP4	4.2 Smart Energy	Anton Bauer	Fraunhofer IISB
WP4	4.2 Smart Energy	Thomas Harder	ECPE Directoe
WP4	4.2 Smart Energy	Thomas Detzel	Infineon Villach
WP4	4.2 Smart Energy	Peter Steeneken	NXP
WP4	4.2 Smart Energy	Giuseppe Croce	STMicroel
WP4	4.2 Smart Energy	Braham Ferreira	TU DELFT

Two workshops have been organized:

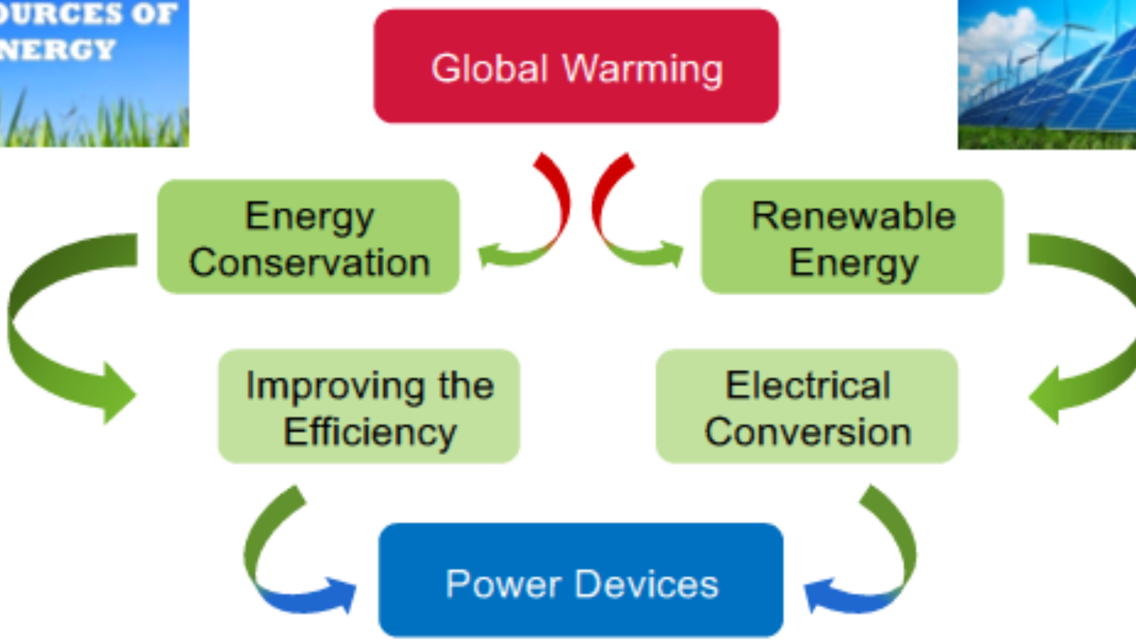
1st Domain Workshop

Bertinoro, October 20, 2016

2nd Domain Workshop Barcelona,

December 14, 2017

The story…



At least 50 % of the electricity used in the world is controlled by Power Devices.

B.J. Baliga, Advanced High Voltage Power Device Concepts, Springer

Lead Applications for SiC & GaN (CLINT/ECPE Roadmap Workshop, 4/10/16)

World-wide Market for Medium-Voltage Power Electronics due to the Energy Transition

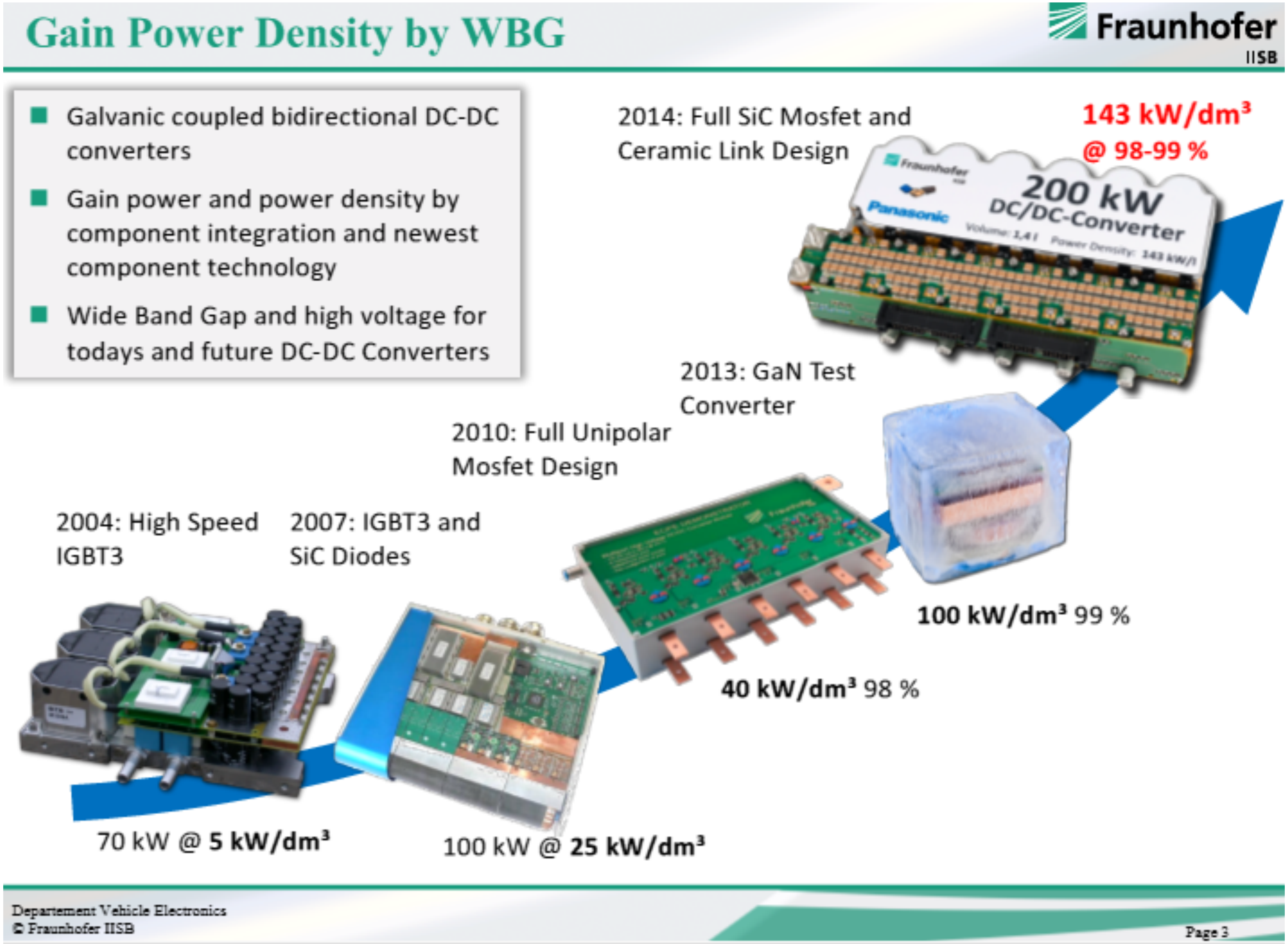
Source	Cumulated installed power until 2050	Annual replacement in 2050
Solar (50% MV)	2.500 GW	250 GW
Wind on-shore (50%)	2.500 GW	250 GW
Wind off-shore (100%)	500 GW	50 GW
Battery power (50%)	1.000 GW	125 GW
Elektrolysers (100%)	500 GW	75 GW
HVDC (100%)	250 GW	30 GW
Over all	7.250 GW	780 GW

- Figures based on internal studies

Source: B. Burger, Fraunhofer ISE, Industriearbeitskreis Mittel-spannungs-Leistungselektronik, 19.09.2016 in Berlin

Fraunhofer ISE

The potential …



System benefit …

Mobile Systems: Automotive

IALB

- Any mobile system should benefit
  - Higher efficiency is higher range or smaller storage
  - Smaller volume and lower weight of the converter and cooler
  - By leverage effect even smaller volume and lower weight of the storage
- Good example is Toyota
  - 10% fuel savings targeted, 5% achieved on prototypes already
  - Power control unit down to 20% of volume, weight from 18kg down to 4kg
  - On the market in 2020

Si

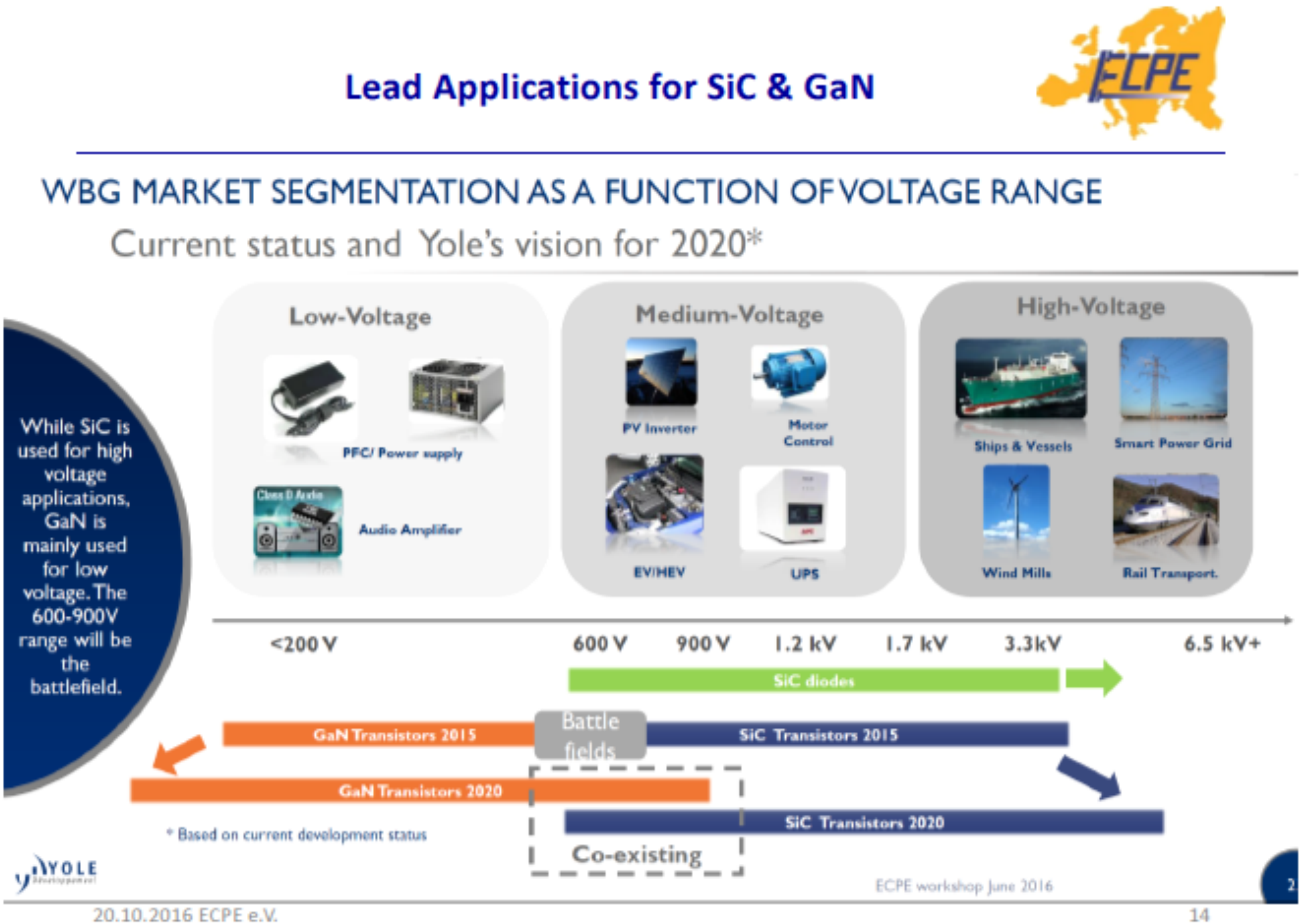
SiC

Source: Toyota

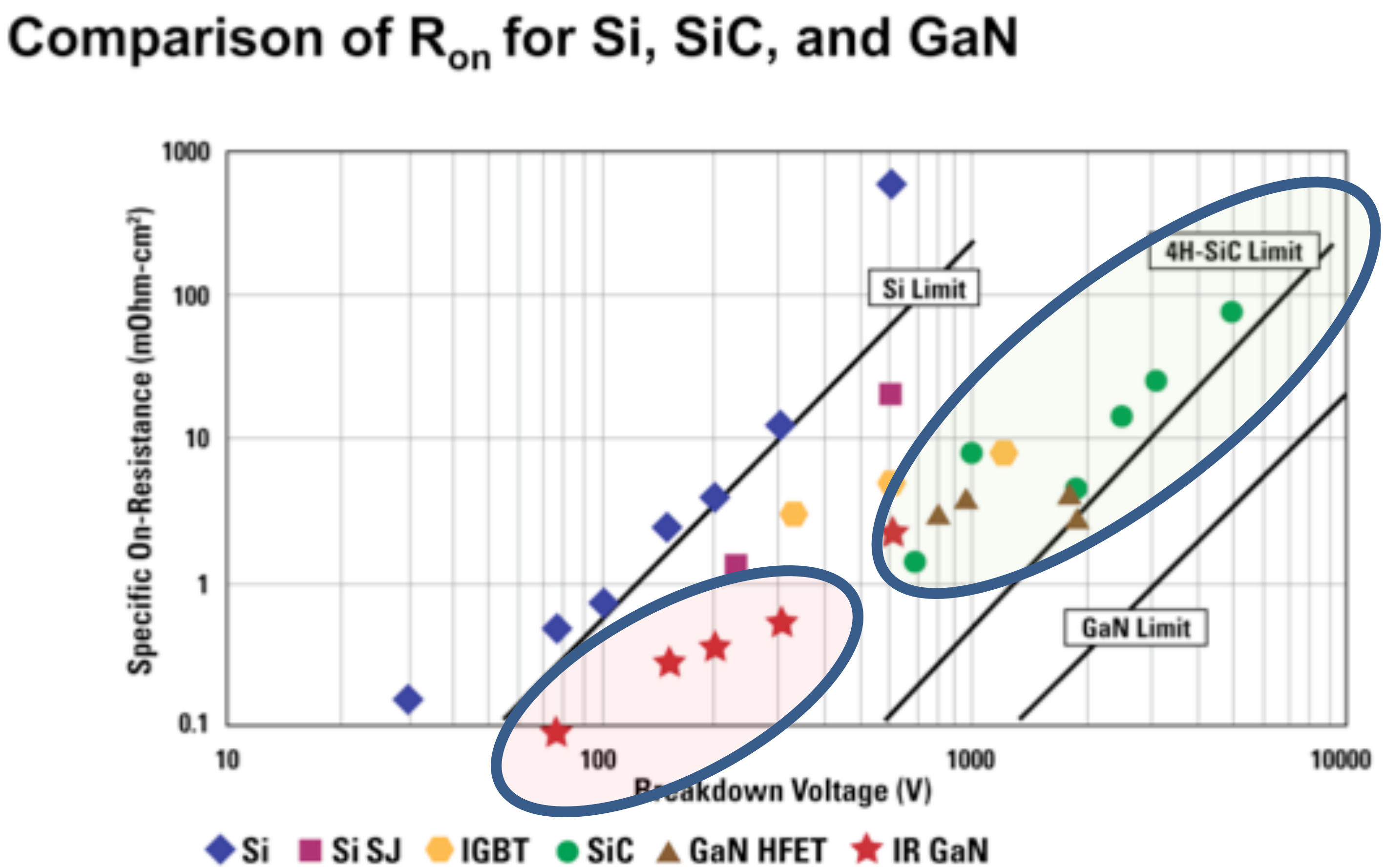
Universität Bremen

Source: ECPE Roadmap Workshop 'Power Electr. 2025', Munich, 26.03.2015

Co-existing & dedication…



Co-existing & dedication…



SiC is the semiconductor for very high voltages (> 1 kV)

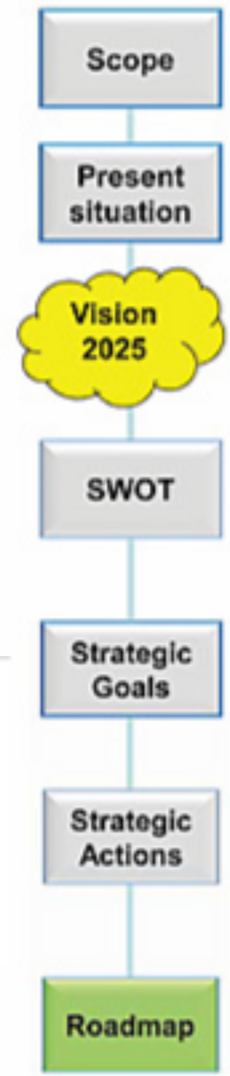
GaN is the semiconductor for very low on-resistance (<1mOhm –cm²)

Roadmaps...

ECPE Roadmap Programme 'Power Electronic 2025'

Objectives:

- Provide input and industrial guidance to research programmes on European and on national Level
- ECPE Member companies will reflect their own company roadmap vs. the ECPE Roadmaps
- ECPE Competence Centre will use the roadmaps when they define new research directions



Structure: three application-related roadmapping Teams

- **Power Supplies** (low power)
- **Automotive & Aircraft** (medium power)
- **Electronic Power Grids** (high power)

Roadmaps…

POWERAMERICA

PowerAmerica Strategic Roadmap for Next Generation Wide Bandgap Power Electronics

This roadmap outlines **key markets and application areas for SiC and GaN** PE, the **performance targets GaN and SiC technologies** are expected to meet over time, technical barriers to achieving those targets, and activities needed to overcome those barriers. The roadmap activities will guide PowerAmerica's strategic decisions for demonstrating the benefits of SiC and GaN, **improving WBG semiconductor device performance, and increasing commercial use of SiC and GaN** PE.

Roadmaps...

IEEE POWER ELECTRONICS SOCIETY
Powering a Sustainable Future

IEEE
Advancing Technology for Humanity

Wide Band-Gap Devices: the Driving Force To the Next Electronic Industry

The International Technology Roadmap for Wide Band-gap Power Semiconductor (ITRW) **fosters and promotes the research, education, innovations and applications** of WBS technologies global/y,

WP4 Energy diversification

- WP4 will define the **strategy** for a roadmap for those **technologies** that **extend the field of application** of semiconductor technologies by **adding new functionalities or extend application range**.
- These technologies, falling under the denomination of "More than Moore", do not scale simply with geometrical size, and are widely diversified; **therefore new metrics will have to be identified for the roadmap**. It includes two main Tasks:
- T4.1 Smart Sensors
- **T4.2 Smart Energy**

Task 4.2 Smart Energy : WBS

- **Fast switching** is the key for **size and weight reduction** with WBG power semiconductors **leading to several issues**: **EMC, low parasitic inductances of the packaging and interconnection technologies, power losses related to passive components, need for system integration solutions, optimised switching cell, integrated drivers**, ...
- As a consequence, the extreme miniaturization of power electronic systems leads to **higher power density** which requires **new improved cooling techniques**, but also leads to higher operation (and junction) temperature.
- **Issues related to high temperature power electronics**: advanced materials and processes for **packaging** and **interconnection** (chip level and system level), **polymer moulding & encapsulation**, substrates, **temperature range for passive components**, **robustness and reliability**, ...

Task 4.2 Smart Energy: Objectives

- To identify the **best application of Power Si and wide band-gap semiconductors** devices (WBS) and provide a clear indication on **where these devices will be disruptive** in their applications;
- Highlight all the **technological** and **material** issues that need to be solved in order to guarantee a large market penetration of these devices;
- To provide a roadmap for the “standard” Si-based technology and the market penetration of WBS devices taking into account **cost/benefit analysis**, the degree if maturity and its expected evolution.

Task 4.2 : Issues

Highlight all the technological and material issues that need to be solved in order to guarantee a large market penetration of these devices;

Technological and material issues

- Material (substrates, quality, reproducibility, supply chain, wafer size, maximum thickness for heteroepitaxial growth)
- Processing issues (contacts, gate, isolation)
- Normally off operation (hybrid or intrinsic)
- Isolated gate (MIS) devices
- Sustainable breakdown, Operational (rated) voltage
- Robustness (UIS, short circuit) & Reliability
- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)ù
- Gate drivers
- ....

Task 4.2 : Roadmap

- To provide a roadmap for the standard Si-based technology and the market penetration of WBS devices taking into account **cost/benefit analysis**, the degree of maturity and its expected evolution.

Roadmap and cost/benefit for WBS

- Large wafer sizes, multi-wafer reactors
- New circuit topologies
- Novel device topologies (lateral vs vertical)
- Novel substrates (bulk GaN/alternative carriers)
- Reliability and stability of WBS
- New technologies at the interfaces for lower costs and higher reliability

Key figures of merit devices :

Device level

- Normally off – Vth > 2V
- Low gate leakage at maximum gate voltage
- Breakdown Voltage 650 V, 1200 V devices
- **Ron vs A (absolute performances)**
- Ron vs Qg (efficiency vs speed)
- Dyn $R_{DS,ON}$ < 20% at maximum voltage
- Reliability/robustness > 20year
- Maximum operating channel temperature

System level point of view:

- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)
- Gate drivers

SiC Roadmap

SiC Device Roadmap

Going for more compactness for power converters

Going for more technological maturity

Years	Si 4.5 kV IGBT or BIGT	4H-SiC 1.2 - 1.7 kV MOSFET JFET/BJT	4H-SiC 3.3 kV MOSFET	4H-SiC 6.5 kV MOSFET IGBT	4H-SiC 10.0 kV MOSFET IGBT	4H-SiC 15.0 kV IGBT	4H-SiC 20 – 30 kV IGBT GTO	AlN/ Diamond 30 – 50 kV IGBT/GTO
2016	√√√	√√	√	x	x	x	x	x
2018	√√√	√√√	√√	√	x	x	x	x
2020	√√√	√√√	√√	√	√	x	x	x
2022	√√√	√√√	√√√	√√	√√	√	√	x
2024	√√√	√√√	√√√	√√√	√√√	√√√	√√	√

- x Fundamental potential exist but technological solution is not ready yet
- √ Engineering die samples available. Probably not qualified chip. Complete package solution may not be ready yet.
- √√ Qualified chip ready. Complete package solution probably ready to be tested in the field.
- √√√ Fully mature and qualified chip is available along with qualified packaged power module to be tested in the field.

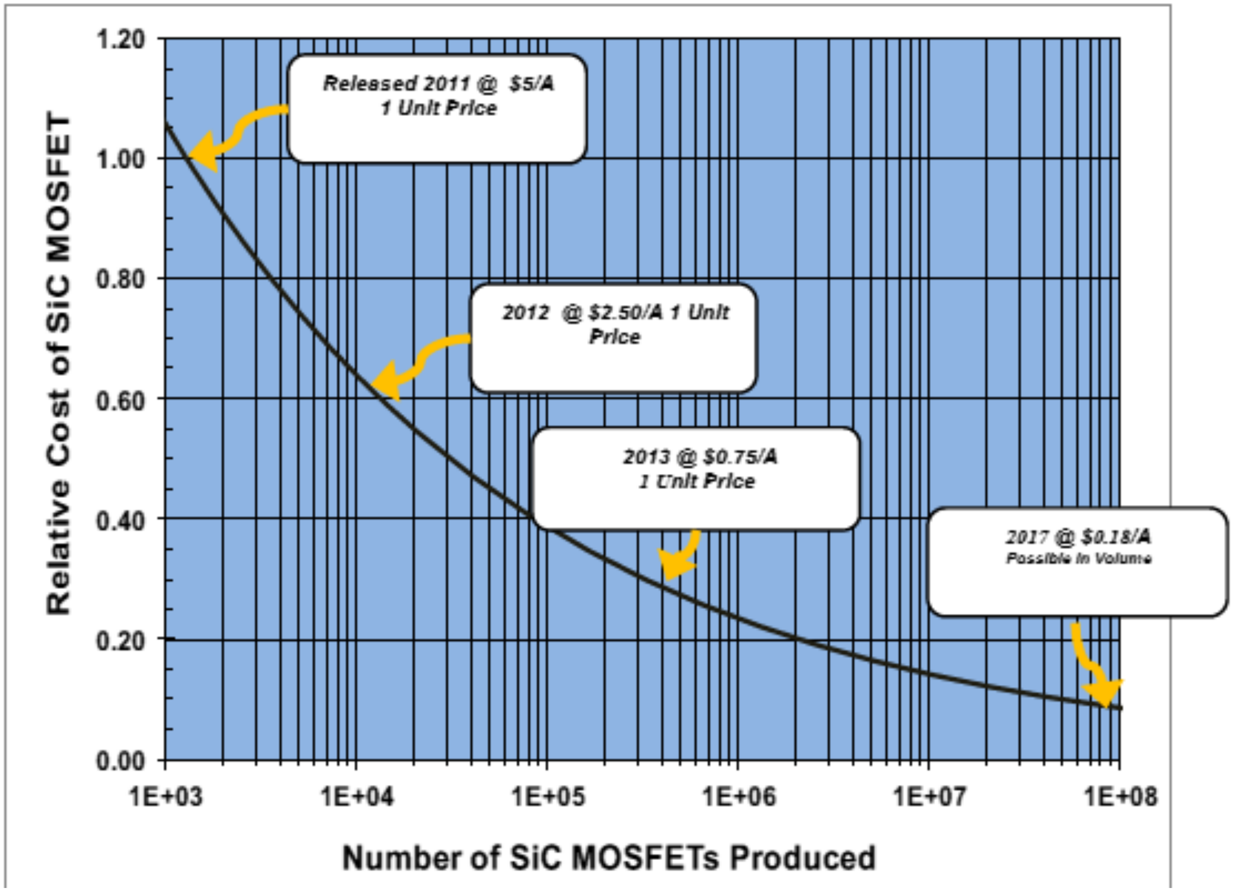
Source: Dr. Muhammad Nawaz, ABB, ESCDERC 2016 but modified

NEREID WORKSHOP BERTINORO OCT 2016

Costs...

Technical Trends in SiC

Fraunhofer IISB



Source: © Cree / nist.gov

Task 4.2: GaN roadblocks

- **Customers want cost parity at the device level**
  – Replace e.g. Si SJ device by a GaN device that yields at par or better system efficiency
- **GaN-on-Si wafer cost is (too) high**
  – Multi-wafer reactors/New concepts
  – Growth on CTE matches substrates (poly-AlN, ...)
  – Others....to reduce growth time and Defect Density
  – 150mm versus 200mm (vs 300 mm ?)
- **GaN Reliability is different from Si (JEDEC) and is not well enough understood—Need standardisation**
  – JEDEC is a minimum requirement, but we need more (GaN specific testing like Dyn Ron, hard switching testing, surge current capability etc)

Task 4.2: status GaN-on-Si

Threats/weaknesses:

- The buffer stack is critical
  - Causes limitations for breakdown, current collapse, RF loss
- High density of threading dislocations & point defects
  - Critical threshold values to achieve reliable devices have not been identified
  - Mechanisms not fully understood
- Drive towards thicker epilayers for power
- Cost roadmap

Strengths/Opportunities:

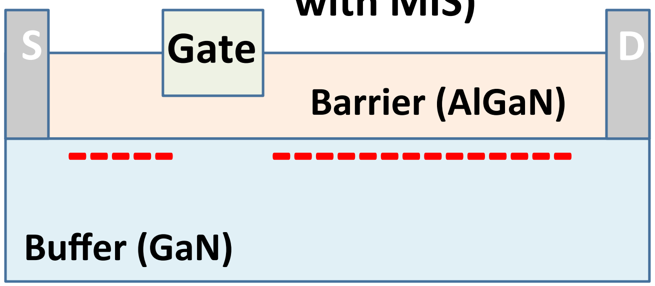
- Main (proven?) choice for power, increasing interest for RF
- Scaling diameter is on-going (now at 200mm)
- Si fab compatibility
  - substrate thickness and contamination
- Easy back-side processing
  - E.g. TSV, local substrate removal, replacing Si by diamond
- Novel integration options, e.g. through SOI, 3D stacking, …
  - Gate drivers, RF digital front end and RF filters, …

Task 4.2: development

- Quality improvement for enhanced reliability
  - Reduction of TD density
    - Nucleation, buffer designs
  - Understanding of fundamental behaviour
    - structural & crystal investigations
    - Modelling
- Higher voltage: thicker / better buffers
  - 600V -> 900V -> 1200V
- Low Rsheet heterostructures
  - E.g. InAlN ~ 220 Ohm/sq
- Selective regrowth
  - n-GaN for ohmic contacts
  - p-GaN for e-mode gates, vertical transistors
  - For combined GaN/CMOS
  - Requires integration in device process flow

Task 4.2: Normally off

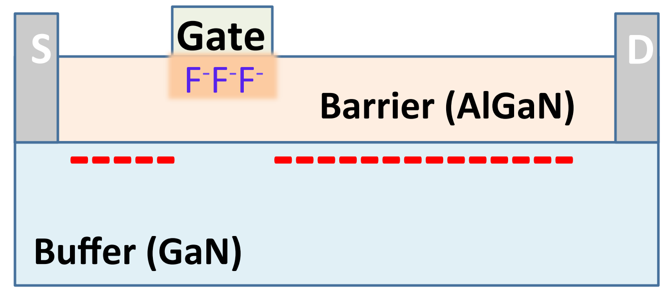
Recess on the Schottky Gate (also with MIS)



- **Leakage, trapping, …**

Oka et al., IEEE EDL 29, 668 (2008)

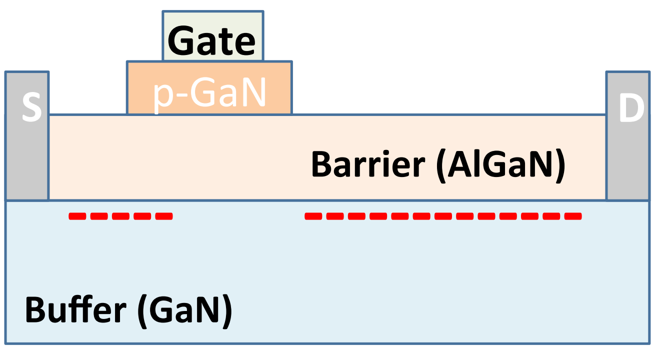
Fluorine implantation



- **Vth instabilities, leakage, …**

Feng et al., IEEE EDL 31, 2386 (2010)

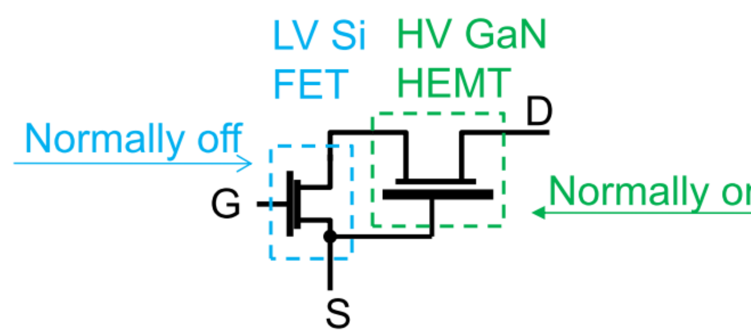
p-type Gate



- **Need for p-type, Vth~1.5 V, …**

Uemoto et al., IEEE TED 54, 3393 (2007)

Cascode configuration



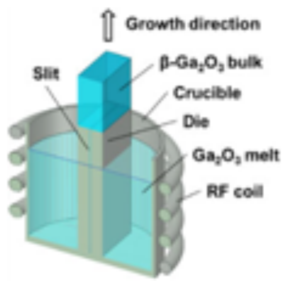
- **Combined Si/GaN, MIS gate, …**

Eg. Transphorm, …

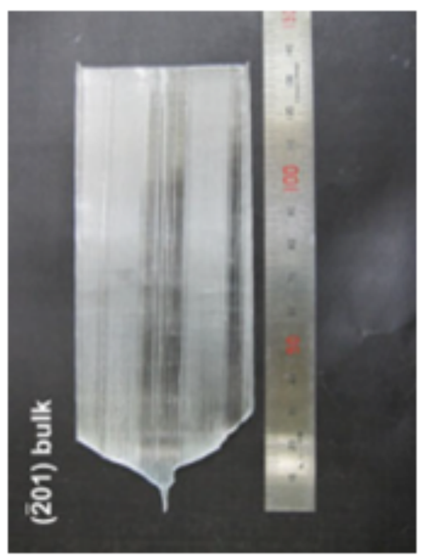
New technologies…

UWBG--Ga_2O_3 : E_c=8MV/cm

- Substrates by Edge Fed Growth idem to Sapphire. The only WBG material that can be grown from the melt (low cost, DD<10^4 cm^{-2}). Low thermal conductivity. No p-type doping.
- Epi by HVPE, MOCVD, MBE (β-Ga2O3) or MIST epitaxy (α-Ga2O3)
- Currently at 2” (cots). Expected 4” in 2018, 6” in 2022.
- Very good n-type doping control with very low resistivity.
- Publications on first 600V Schottky diodes and Transistors



4 in. (2̄01)



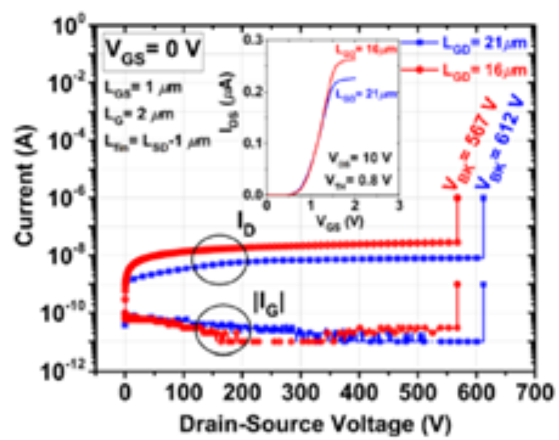
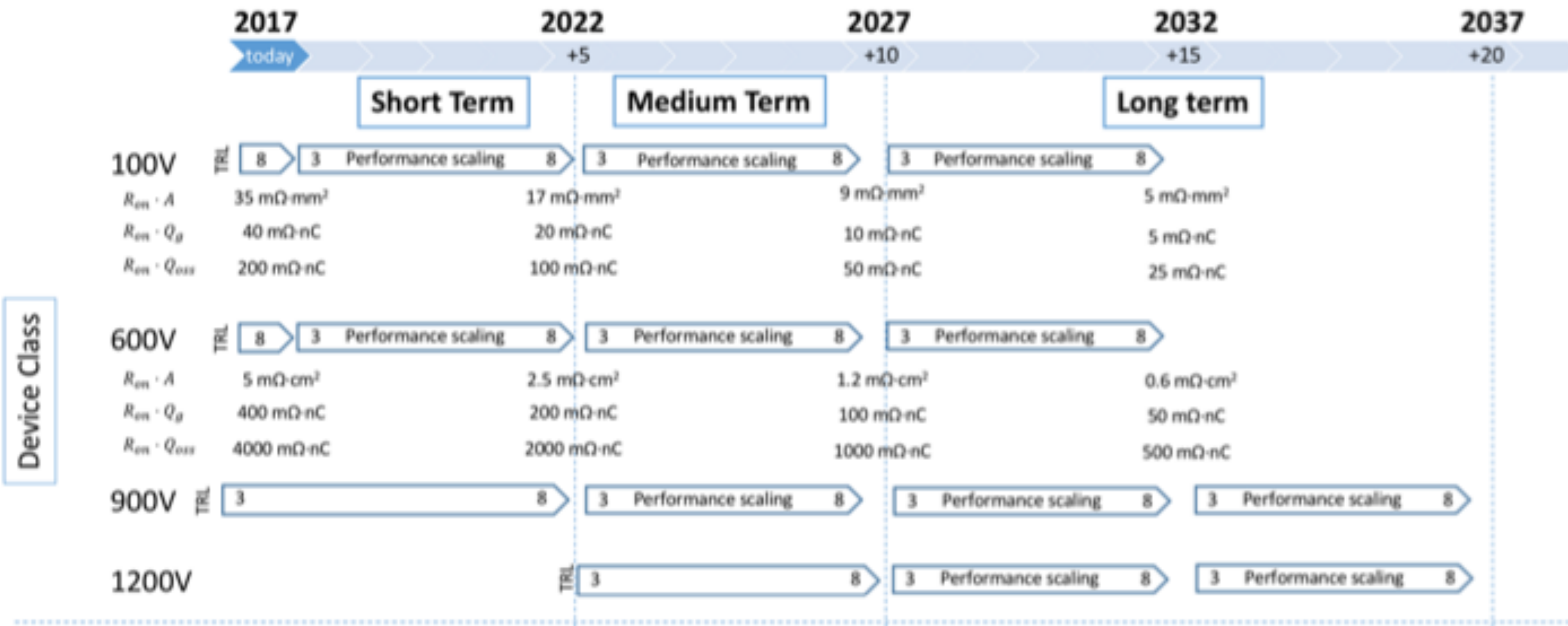


FIG. 5. The breakdown voltages of Ga_2O_3 finFETs with $L_G = 2$ μm and $L_{GD} = 16, 21$ μm while biased in the off-state at $V_{GS} = 0$ V. The inset shows the transfer characteristics of the same device indicating a $V_{TH} = +0.8$ V.

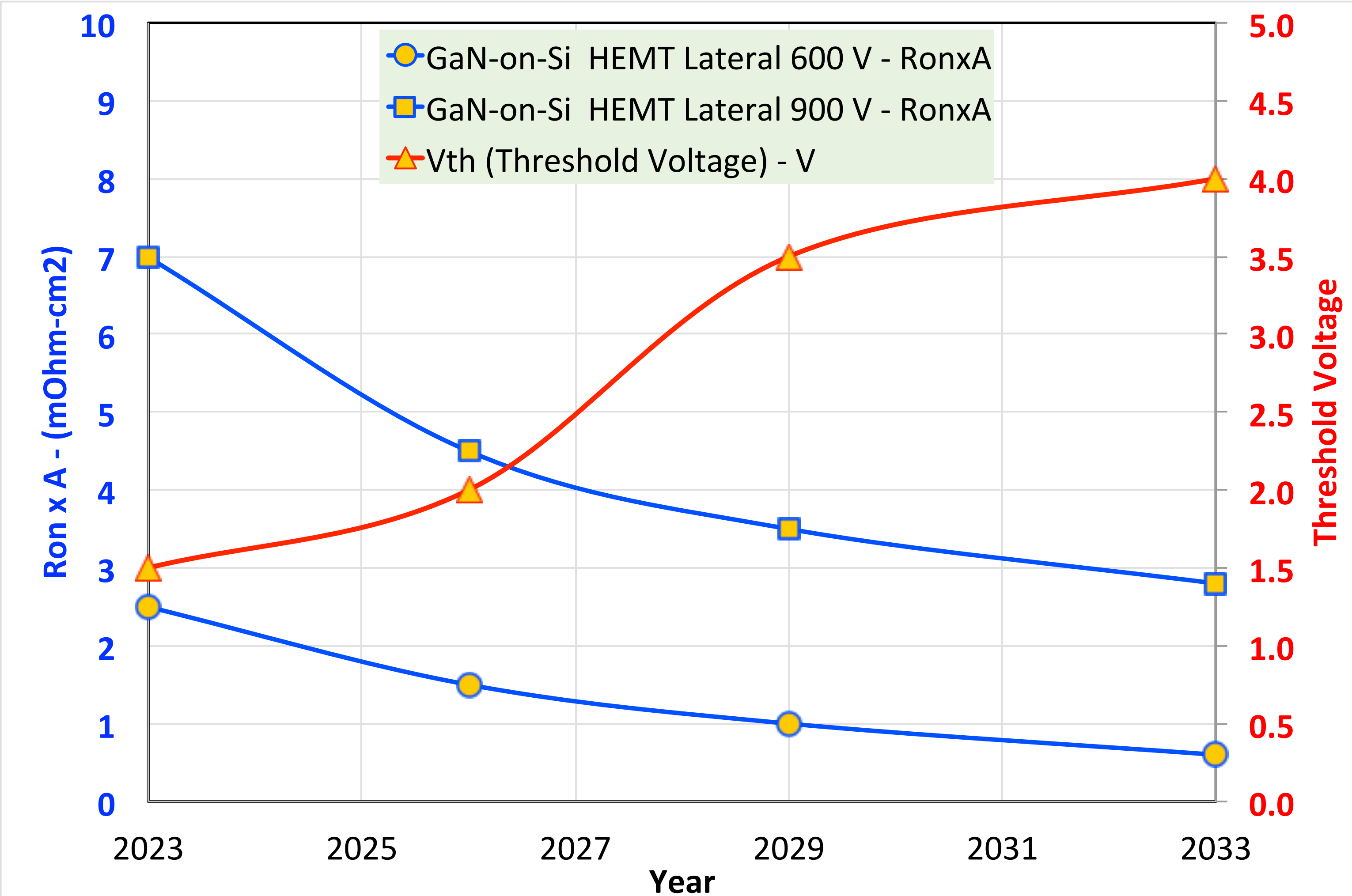
Roadmapping: GaN FoM

c) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	Short/ Medium term: 5+	Medium / long term: 10+	long term: 15+
Ron x A 100V: 35 mΩ.mm² 600V: 5 mΩ.cm² 900V: commercially not existing	100V: 17mΩ·mm² 600V: 2.5mΩ·cm² 900V: 7mΩ·cm²	100V: 9mΩ·mm² 600V: 1.2mΩ·cm² 900V: 4.5mΩ·cm²	100V: 5mΩ·mm² 600V: 0.6mΩ·cm² 900V: 2.8mΩ·cm²
$R_{on} \cdot Q_g$ 100V: 40 mΩ.nC 600V: 400 mΩ.nC	100V: 20 mΩ.nC 600V: 200 mΩ.nC	100V: 10 mΩ.nC 600V: 100 mΩ.nC	100V: 5 mΩ.nC 600V: 50 mΩ.nC
$R_{on} \cdot Q_{oss}$ 100V: 200 mΩ.nC 600V: 4000 mΩ.nC	100V: 100 mΩ.nC 600V: 2000 mΩ.nC	100V: 50 mΩ.nC 600V: 1000 mΩ.nC	100V: 25 mΩ.nC 600V: 500 mΩ.nC
Ig	<1µA/mm	<10nA/mm	<1nA/mm
Vth (at I_{DS} 10µA/mm)	>2.5V	>3.5V (tunable 1V to 5V)	>4V (tunable 1V to 5V)
Lifetime (yrs @ Temp), Today: 15yrs (80% rated voltage), 1FIT	10yrs @ 150°C 20yrs @125°C 1ppm, 20yrs (solar, automotive)	20yrs @ 175°C	20yrs @ 200°C
Short Circuit Robustness	5µs @ 80% of V-rating	10µs @ 80% of V-rating	

Roadmapping: GaN FoM



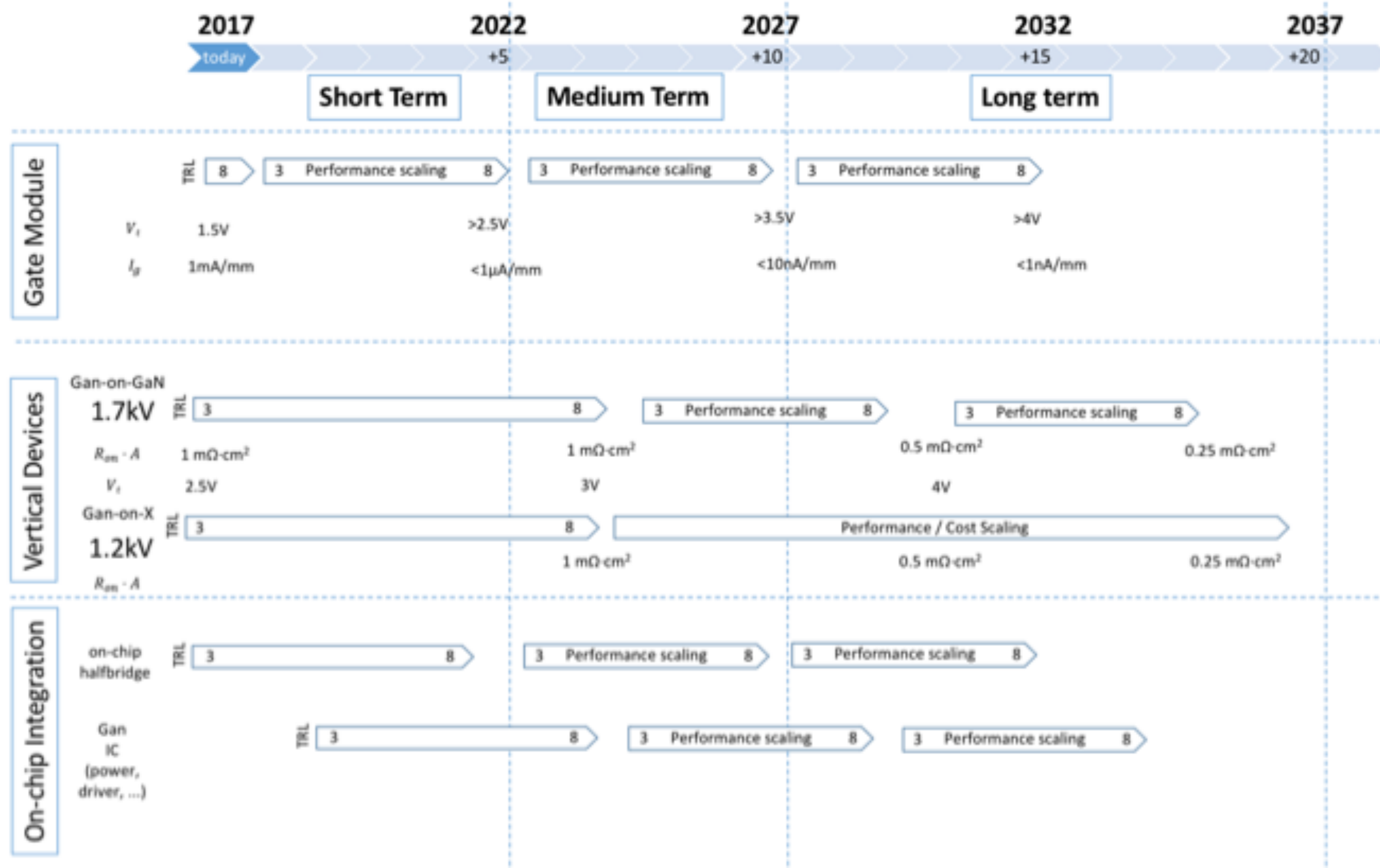
Roadmapping: GaN FoM



GaN Roadmapping Applications & Technologies

b) Potential for application or Application needs and Impact for Europe	Short/ Medium term: 5+	Medium / long term: 10+	long term: 15+
Low power DC/DC converter (POL)	Volume	Predominant	Predominant
Power supplies (PFC, e.g. for data centre)	Volume	Predominant	significant
Automotive EV/HEV (DC-DC converter, charger)	Prototype	Volume	Predominant
PV (roof/home)	Prototype	Volume	Predominant
Motor drives	Prototype	Volume	Predominant
Mobile chargers/adapters	Volume	Predominant	significant
c) Technology and design challenges		...	
GaN-on-Si substrate diameter	Cost Wafer size, 8"	Cost Wafer size, 8"	Cost Wafer size, 12"
GaN-on-Si substrate thickness	Semi std		
p-Gate architecture	p-Gate architecture dominant Blanket growth or blanket regrowth	Selective regrowth Polarization Engineering	Isolated architecture dominant
MIS-Gate structures	Solving basic material science issues	Dit engineering Industrialization	Reliability Yield
Ohmic contacts	<0.5 ohm.mm Alloyed metals	<0.2 ohm.mm Regrown contacts	<0.1 ohm.mm Regrown contacts
On-Chip Integration	Topology Reliability Thermal management Packaging	Cost	Cost System
Thin wafers and interconnects	<100µm	<60µm	Electrically required thickness

Roadmapping: GaN Technology



SiC Roadmapping
Applications & Technologies

b) Potential for application or Application needs and Impact for Europe	Short/ Medium term: 5+	Medium / long term: 10+	long term: 15+
Power supplies (PFC, e.g. for data centre)	Volume	Volume	significant
PV (roof/home)	Volume	Volume	Predominant
PV (MV, central)	Prototype	Volume	Predominant
Automotive EV/HEV (DC-DC converter, charger)	Prototype	Volume	significant
Automotive EV/HEV (traction inverter)		Prototype	Volume
Motor drives (industry)	Prototype	Volume	Predominant
Traction (trains, trams)	Prototype	Volume	Predominant
Wind power	Prototype	Volume	Predominant
Grid: power transmission and distribution (e.g. HVDC)		Prototype	Volume
Airplanes	Prototype	Prototype	Volume
c) Technology and design challenges			
Advanced passivation for high ruggedness (humidity, gases, environmental impacts)	In the substrate	On the chip	
Self-aligned process techniques for high manufacturability (e.g. TrenchMOS)	Prototype	Volume	
Wafer thinning and bonding Thermal, mechanical, electrical (Ron) Today: 100µm	50µm	30µm	Electrically required thickness

main recommendations for Smart Energy Roadmapping

Main recommendations:

- Need to identify the **killer applications** for GaN/SiC devices;
- **Gate architecture** (the long term one) need to be finalized soon (MIS/pGate) to finalize gate leakage and threshold voltage values
- Reliability and Robustness evaluation/**standardization**
- Need to have a completely new approach (full system redesign)
- Costs comparison must be done at system level (not device level)

To exploit the full potential of WBS:

- Packaging and system integration technologies enabling low parasitic inductances to master EMC issues enabling reliability at higher temperatures
- Low inductance packaging and integration technologies: power PCB with chip embedding, system-in-package (SIP), switching cell ..
- Passive components for fast switching: mainly inductors, reduce losses at high switching frequencies, thermal management of (integrated) passives