NEREID

3rd General Workshop, Sardinia, June 2018

« Nanoscale FET » Roadmap

WP3 – Task 3.1

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NanoElectronics Roadmap for Europe: Identification and Dissemination

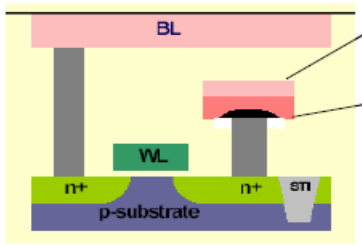
Coordinators of the sub-Tasks

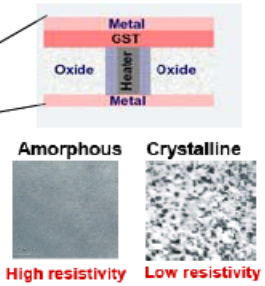
- **FD-SOI:** Stephane Monfray, STMicroelectronics
- **FinFET:** Anda Mocuta, IMEC
- **Nanowires:** Lars-Erik Wernersson, Lund University
- **Negative Capacitance FET:** Marie Garcia-Bardon, IMEC
- **Carbon Nanotubes**: Marie Garcia-Bardon, IMEC
- **Memories:** Carlo Cagli, LETI
- **3D Sequential Integration:** Claire Fenouillet, LETI
- **Modelling/Simulation tools:** Luca Selmi, Udine University
- **Characterization Tools:** Gerard Ghibaudo, Grenoble INP/CNRS
- **Reliability**: Ben Kaczer, IMEC

Nanoscale FET roadmap for low energy, scaling, high perf., new functionalities

… IC evolution …

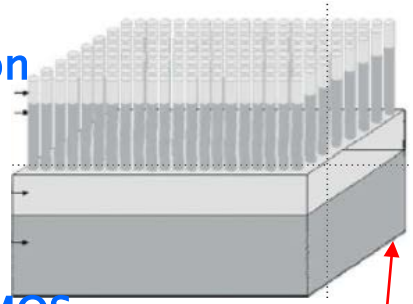
NEMS



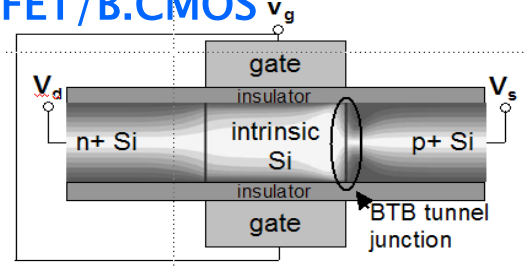


Non-charge/
PCRAM

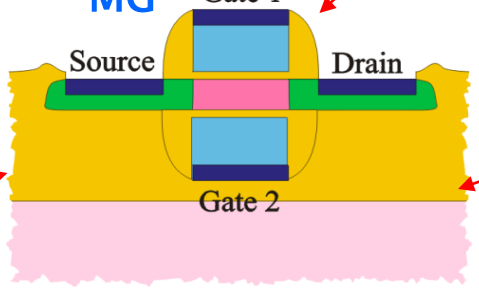
NW/Carbon
-based
MtM



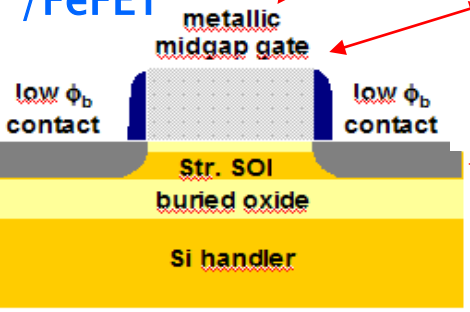
TFET/B.CMOS

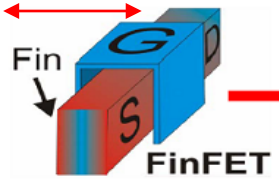


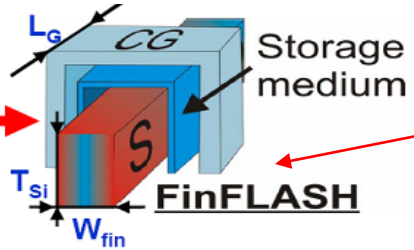
MG



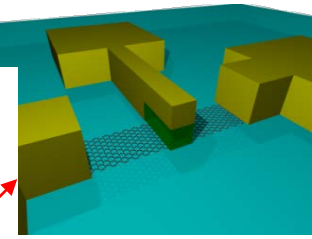
FDSOI/NCFET
/FeFET



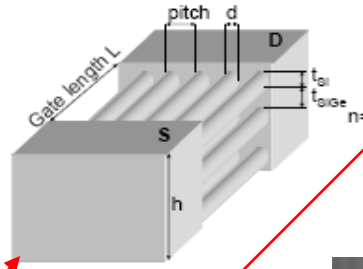




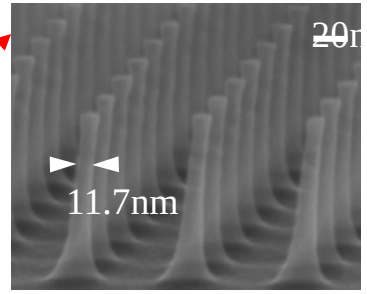
Nanosheet/2D-FET



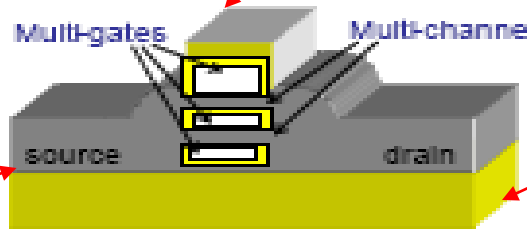
3D-NW



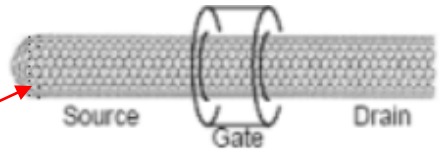
Lateral/Vertical



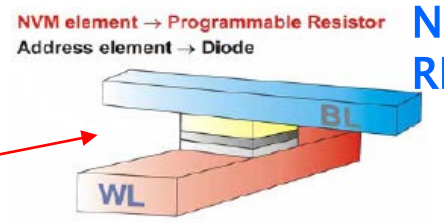
NWFET/NVM



MC



CNTFET



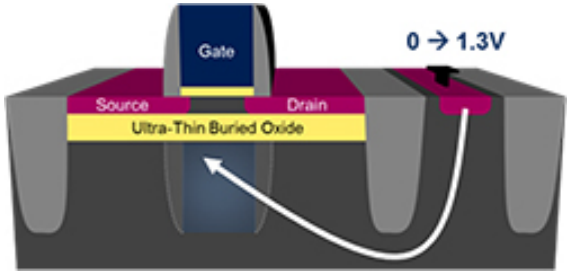
Non-charge/
RRAM/MRAM

… IC evolution …

FD-SOI

Topic « *FDSOI* » (1/2)

- Principle:



- FD-SOI technology enables control of the behavior of transistors not only through the gate, but also by polarizing the substrate underneath the device, similarly to the **body bias** available in Bulk technology
- **more power / lower leakage** /wider range of operation down to lower voltages
- The **manufacturing process for FD-SOI is much simpler** than alternatives

❖ 1. Key research questions or issues

-Improving performances (strain technologies for Higher drive current, Si & BOX thickness reduction, new materials (GeOI, III-V OI) and 3D integration)

-Design evolutions exploiting back biasing techniques

-Differentiation: FDSOI Logic & embedded flash memories for IoT / Automotive applications

- Medium term: 5+: **dual stressors on sSOI wafers, Tsi<6nm, Tbox<15nm, development of planar nanosheet devices** (2 channels), **ULP IoT** dedicated design **Vd<0.5V**, embedded PCM, monolithic 3D
- Long term: 10+ : **Tsi<5nm, Tbox<10nm, 3D multi-layers nanosheet devices with new materials, Vd<0,4V,** monolithic 3D with high-mobility materials, new flash memories

❖ 2. Potential for application or Application needs and Impact for Europe

Low power devices for Automotive, Consumer, IoT, Imaging and future non CMOS computing

- Medium term: 5+ : Automotive, Consumer, **ULP devices (wearable IoT), Spatial, High speed datacom,**
- Long term: 10+ : **Smart sensors (environment), bio and autonomous sensors, ULP for medical IoT, Neuromorphic & Quantum computing**

Topic « *FDSOI*» (2/2)

❖ 3. Technology and design challenges

Develop Integration of Strain SOI substrates (processing of tensile strain for NMOS & compressive strain for PMOS), Compatibility with low power flash memories, FDSOI design with Vdd<0,4V, Integration with new materials (SiGe with high Ge content) and III-V materials in 3D process

- Medium term: 5+ : Local strain N & P, PCM integrated with FDSOI, Subthreshold circuits, High Ge SiGeOI, Thermal management for 3D
- Long term: 10+ : Development of solutions for sub-60mV/dec devices, 3D III-V OI circuit, Co-integration of CMOS with Si- photonic

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

	2023	2026	2029	2033
Ieff/Ioff	Ieff 470/420 µA/µm @10nA/µm Ioff	Ieff 470/420 µA/µm @10nA/µm Ioff	Differentiation through options	Differentiation through options
Variability (Avt)	<1mV.µm	<0.9mV.µm	<0.8mV.µm	<0.8mV.µm
Vdd (logic)	<0,7V	<0,65V	<0,6V	<0,6V
Subthreshold slope	<70mV/dec	<65mV/dec	<65mV/dec Introduction of sub-60mV/dec	<60mV/dec Introduction of sub-60mV/dec

GLOBAL RECOMMENDATIONS

Develop differentiated options (RF, Embedded Memories, Imaging, Sensors) on FDSOI (applications for automotive, IoT)

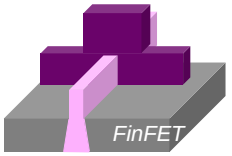
Develop ULP design (Vd<0,4V) for IoT market (wearable, medical…)

From device architecture point of view, FDSOI technology can suit 14nm & 10nm nodes using sSOI and other materials

FDSOI and 3D integration can respond to future neuromorphic and quantum computing approaches

FinFET

Topic: FINFET



❖ 1. Key research questions or issues

- subthreshold slope control **to less than 70mV/dec at very short gate length (<14nm)**
- **improved device performance (Ion/Ieff at given Ioff) while scaling the gate length and pitch**
- **control of parasitic capacitances** at scaled dimensions
- **Variability control** at very scaled dimensions
  - ➢ Medium term: 5+: innovation needs to continue in the following areas: contact resistivity, conformal doping, dopant activation above solid solubility limit, low k or air spacer; HKMG scaling and multi-Vt; high mobility channels; channel strain enhancement; integration of taller fins**; understand under what conditions nanowires will outperform finfets**; **Co-integration with other device architectures or between 2 channel materials**; **3Dsequential integration with other devices**
  - ➢ Long term: 10+ : Co-integration with other device architectures or between 2 channel materials; 3Dsequential integration with other devices

❖ 2.Potential for application or Application needs and Impact for Europe

- current workhorse device for Si CMOS technologies
- **current best option for high performance space**
- currently **can cover part of the low power/low cost space**
- can be **considered for quantum computing as qbits**
- specialty sensors

Topic: FINFET

3. Technology and design challenges

No single device/material able to replace Si CMOS; Co-integration of finfet with other device architectures or between different channel materials will be key; Improve finfet analog performance

- Medium term: 5+ develop **finfets that can be processed at low T**; develop finfets that **can withstand a long thermal cycle for 3D seq integration**;develop integration flows for **multiple channel materials and strain**(e.g. Si, SiGe, Ge, III-V)
- Long term: 10+ : develop **co-integration schemes between finFETs and nanowires/nanosheets**

4. Definition of FoMs (quantitive or qualitative) or planned evolution

	2023	2026	2029	2033
d) Definition of FoMs (quantitative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)				
Ieff at fixed Ioff (normalized): 1	1.2	1.3	1.45	1.55
CV/I (normalized): 1	0.75	0.7	0.55	0.5
S (mV/dec): 65	67	69	71	75
min achievable Ioff	<10pA/um	<10pA/um	<10pA/um	<10pA/um
Avt	<1mV.um	<1mV.um	<0.8mV.um	<0.8mV.um

5. Other issues and challenges, and interaction with other Tasks/WPs:

- **Manufacturing processes and integration will become very complex**; working with increased aspect ratios will be key; system level studies to decide what are the best devices to be co-integrated and in what way, for a given application

GLOBAL RECOMMENDATIONS

Develop co-integration of different channel materials

Develop co-integration with other transistor architectures (nanowires, nanosheets, vertical devices)

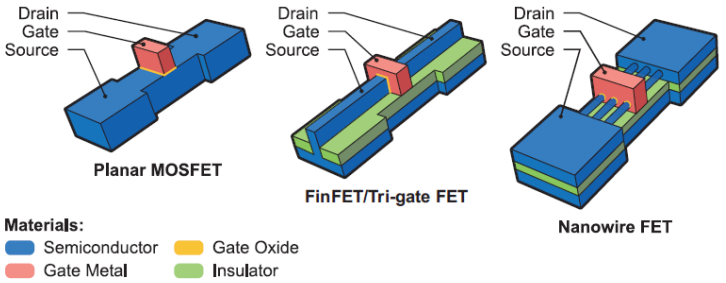
Develop low thermal cycle finFETs for sequential integration

Develop low contact resistivity and high strain solutions, low K spacer materials or airgap spacer, finFET analog performance, finFETs as devices for quantum computing

Nanowires

Topic « *NWs* » (1/2)

- Principle



Key advantages:
Advantageous transport
→ high transconduc. and I_{on}
Wrap-gate geometry
→ low output conduc. and DIBL
Band gap engineering
→ reduced I_{off}

❖ 1. Key research questions or issues

-What performance (Ion, Ioff, gm, ft/fmax, NF) can be achieved in different materials and geometries?

-Circuit/technology co-design in 3D transistor architectures

-Differentiation: Advantageous transport properties (III-Vs and Ge) combined with GAA for electrostatic control

- Medium term: 5+: Available data suggests that the best performance (lowest Ioff, highest Ion, highest gm, etc) is obtained for Si, Ge, and III-V nanowires.
- Long term: 10+ : Co-design transistor/circuit/technology for 3D structures

❖ 2. Potential for application or Application needs and Impact for Europe

Extend the roadmap for CMOS scaling based on improved electrostatic control and increased drive current

Enhance the CMOS RF & millimeter wave-properties by (III-V) materials integration

Medium term: 5+ :Introduction of **hybrid III-V/Si(Ge) and/or all-III-V technology for high-performance applications (both RF/mmWave and mixed-mode)**

Long term: 10+ : **Integration of high-speed logic** and high-performance front-ends **using III-V technology combined with CMOS and possible TFETs**

Topic « *NWs» (2/2)*

- 3. Technology and design challenges

- **Challenges in terms of 3D processing in complex geometries at 10 nm Lg**
- **3D transistors/circuits with nanowires stacked in 3D**
- Medium term: 5+ : Maturing of the process technology for Si, Ge and III-V nanowires to meet the requirements of IoT and high-performance applications
  - Long term: 10+ : Circuit layout in complex 3D architectures with minimized parasitics

- 4. Definition of FoMs (quantitive or qualitative) or planned evolution

	2023	2026	2029	2033
- I_{on}, I_{off}, g_m, f_t/f_{max}, NF	Ion 650 µA/µm (normalized to periphery) > 3mS/µm gm (normalized to periphery) , <1nA/µm Ioff , > 500 GHz fmax	gm > 3.6 mS/µm	gm > 4.3 mW/µm	gm > 5.1 mS/µm

GLOBAL RECOMMENDATIONS

Develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar)

Develop transistor/circuit co-design strategies for mixed and mmW applications

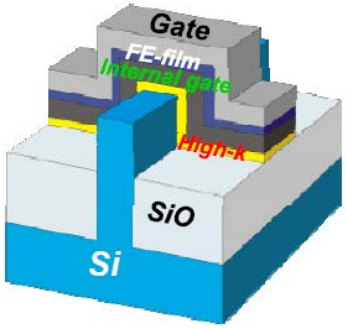
Consider the 3D aspects of processing (stacking, vertical integrations etc)
Identify the best material and geometry options for logics (high-speed as well as low-power)

The electrostatics and heterostructure design options provided are beneficial for TFETs

Negative Capacitance FET

Topic « *NCFET* » (1/2)

Exemple of Trigate NCFET:



- NCFETs have the potential to break the 60 mV/dec subthreshold slope limit but rely on another mechanism than TFETs. NCFETs have the same structure as MOSFETs except that a ferroelectric thin film is inserted between the dielectric and the gate.

❖ 1. Key research topics or issues

- **What is the minimum FE layer polarization switching speed**
- **Expected SS improvement over equivalent MOSFET or FinFET**
- **Proof that hysteresis free and sub-60 mV/dec operation are possible**
- **Limit of drive current due to increased EOT**
- **Variability, Reliability, Trapping in FE layer**

❖ 2. Potential for application or Application needs and Impact for Europe

- **NCFET is a potential candidate to continue the logic scaling roadmap if included in advanced devices gate stacks at aggressive nodes**
- **NCFET could also be a candidate to expand technologies at more relaxed dimensions such as in SOI and bulk planar 28 nm to 65 nm nodes, by improving performance and reducing power without area scaling and at lower cost than aggressive nodes**

Topic « *NCFET» (2/2)*

❖ 3. Technology and design challenges

-Fabrication of thin Hafnium based (in HfxZr1-xO2 and HfAlO) ferroelectric layers. Challenges of ferroelectric phase formation: strain, doping and anneal effect on Orthorhombic fraction, polarization barrier, crystallization

-Identification of the adapted coercive field and remanent polarization for logic application

-Capacitance matching

-Polarization switching dynamics and frequency limit

-Need and feasibility to make FE-layers with uni-domain nucleation

-Impact of depolarization field

-Footprint and scaling challenges

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

Device level metrics: Average SS over 3 to 4 decades (forward and reverse), Ion/Ioff over Vdd and Vt ranges (impact of Vdd and Vt on FE operation), Negative DIBL, negative differential resistance

Circuit metrics: Logic active power consumption due to hysteresis, SRAM stability with hysteresis

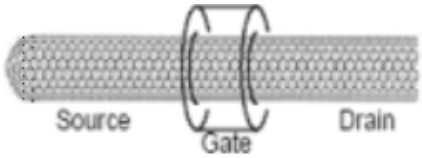
GLOBAL RECOMMENDATIONS:

−Identify the maximum switching speed from dedicated RF measurements
−Identify from TCAD and modelling the optimal dimensions, in particular the coercive field and remanent polarization for ultra scaled FETs
−Develop thin Hafnium based Ferroelectric layers with low coercive field and target polarization
−Develop understanding of the impact of traps and develop design and technology mitigation strategies
−Develop compact models and design tools and evaluate the power-performance on real design contexts
−Investigate the impact of hysteresis at design level
−Investigate the scaling potential of the device

Carbon NanoTube FET

Topic « *CNTFET* » (1/2)

Carbon NanoTube FET:



- Depending on the arrangement of the carbon atoms, the CNTs can be either metallic or semiconducting, and are considered both for interconnect or as field effect transistors (FETs).

❖ 1. Key research topics or issues

- **Percentage of metallic CNTs**
- **Parasitic source/drain series resistance**
- **Impact of Schottky barriers in ON and OFF states**
- **Coupling capacitance between the CNT and the surrounding conductors at scaled dimension**

❖ 2. Potential for application or Application needs and Impact for Europe

- **Nanotubes offer theoretically the potential of very fast (THz) and ultimately scaled transistors for logic applications, with self-assembly based fabrication**
- **CNTs are potential candidates for future via and wire material in nano-scale VLSI circuits, eliminating electromigration reliability concerns**
- **Transistors with properly functionalized CNTs are already being used as sensitive and selective chemical and biosensors**
- **CNT-based nano-light sources and detectors may allow intra-chip optical communications and individual molecule level spectroscopy**

Topic « *CNTFET» (2/2)*

❖ 3. Technology and design challenges

-Technology solutions have to be found to remove metallic CNTs, or logic circuit design solutions to deal with caused variability and failure-Capacitance matching

-Size-independent contact schemes with low Schottky barrier heights have to be developed

-Solutions have to be found to screen the impact of the Schottky barrier on leakage

-Fabrication speed: non metallic catalysts are slow, metallic catalyst lead to possible metallic CNTs hence shorts and device variability

-The growth direction of SWNTs on SiO2-Si substrates is difficult to control since SiO2 is an amorphous material. Misaligned CNTs lead to variability and failure

-CMOS compatible metals for source/drain

-High variability due to doping fluctuation in the ultra-thin body if n/p devices are made by doping

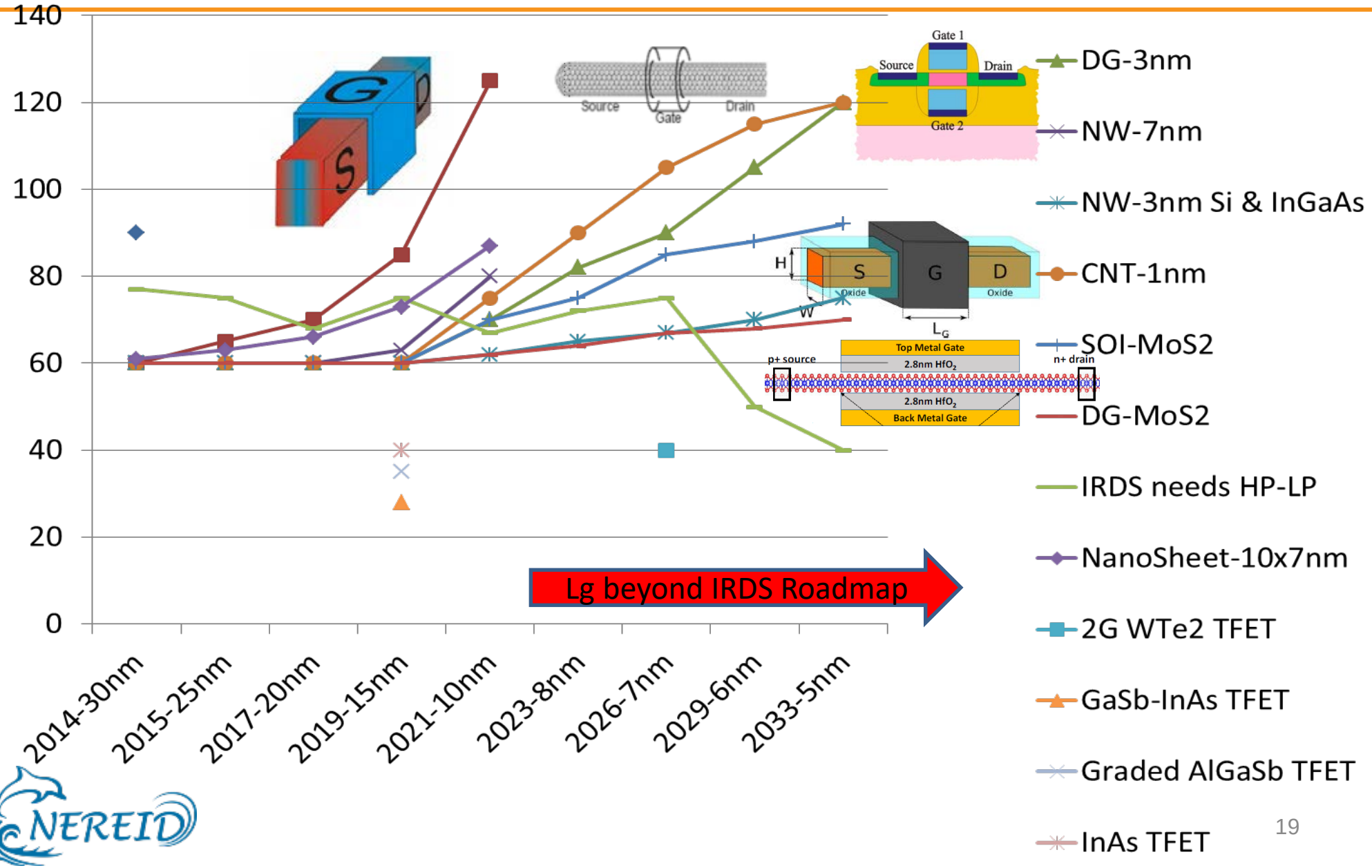
❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

The FoMs of Silicon MOSFETs (Ion, Ioff, gm, SS) apply. Percentage of failure and variability due the metallic CNTs and bad orientation (failed growth)

GLOBAL RECOMMENDATIONS:

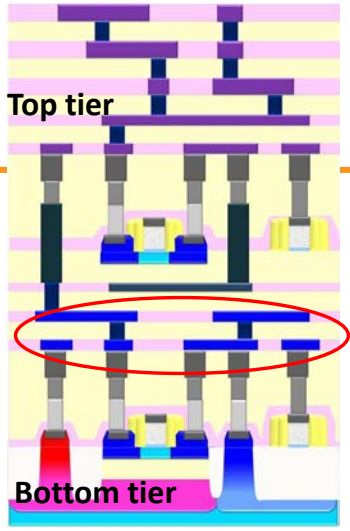
–Develop solutions to lower the Schottky barriers at source/drain
–Develop solutions to remove the metallic CNTs
–Develop faster growing process
–Develop circuit design strategies to deal with variability induced by m-CNTs and doping fluctuation
–Develop compact models and design tools and evaluate the power-performance on real design contexts taking into account the physics of the device (quantum capacitance) and its parasitics

Sub. Swing vs Year / Lg (mV/dec)*(Sim.)*



3D sequential

Topic « *3D Sequential* » (1/2)



- Principle

- 3D sequential is an alternative to conventional device scaling.
- Compared to TSV-based 3D ICs, 3D sequential process flow offers the possibility to stack devices with a lithographic alignment precision (few nm) enabling via density > 100 million/mm^2 between transistors tiers (for 14nm design rules).
- Possibility to merge several technologies, material…

❖ 1. Key research questions or issues

- **Which applications will benefit from very high density interconnections:**
  - ➢ Medium term: **5+: For IoT: intelligent local processing of the data to decrease the bandwith of data transmission. Neuromorphic architectures.**
- **Thermal stable metallization with low resistance** (5+: Cu/ULK or W/ULK) (10+: Co, Silicided intercos)
- **Reliability for low temperature gate stack**
- **Low thermal cycle device temperature**
  - ➢ Medium term: 5+: **Same performance for top and bottom Mosfets**

❖ 2. Potential for application or Application needs and Impact for Europe

CMOS on CMOS for area scaling (5+: **SRAM memory** block to block) (10+: **Enabler for in memory computing architecture and neuromorphic**), **imager co-integrated with logic** (5+: 3D pixels for smart pixels with local memory storing) (10+: Smart pixels with local computing capabilities (each pixel will benefit from its local computing unit)), **Computation immersed in memory, Sensors and CMOS for IOT** (5+: NEMS, bolometers with the local analog parts with better performance than ASIC and better cost than co-integration) (10+: **multisensing platform**), **beyond CMOS devices co-integration with CMOS** (5+: introduction of **TFET, 2D TMD, graphene**) (10+: **Qubit addressing**)

Topic « *3D sequential*» (2/2)

❖ 3. Technology and design challenges

Design tools optimized for sequential 3D not available, reducing parasitics in each implementation (5+: Wire length decrease) (10+: material optimization)**, thermal management/self-heating mitigation** (5+: layout optimization) (10+: layout + heat spreaders + thermoelectric cooling, energy harvester)**, manufacturing challenges** (5+: same performance, same yield as 2D integration) (10+: Yield on multi-Tiers)

- Medium term: 5+ : Use of 2D existing tools to provide non fully optimized (fold or shrunk techniques) 3D place and route tools.
- Long term: 10+ : **Actual 3D place and route tools with 3D optimization at the logic gate scale.**

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

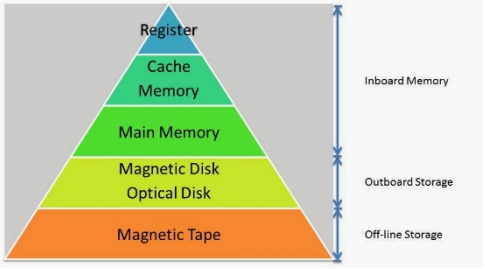
Top level device performance and reliability (5+: similar to 2D), contamination management (5+: In industrial fab with W or Cu intercos), **System level performance versus 2D or 3DTSV** (5+: same as 2D TSV) (**10+: > than 2D or 3DTSV**)**, System level area versus 2D or 3DTSV** (5+: same as 2D TSV) (**10+: < than 2D or 3DTSV**)**, System level cost comparison versus 2D or 3DTSV including yield** (5+: same as 2D TSV) (**10+: < than 2D or 3DTSV**)**, multi-tiers stacking** (5+: 2 tiers), (**10+: more than 2 Tiers**)**.**

❖ 5. Other issues and challenges, and interaction with other Tasks/WPs.

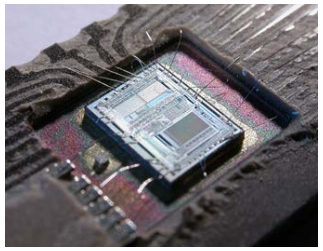
GLOBAL RECOMMENDATIONS
To define which applications will benefit from very high density interconnections (IOT, neuromorphic…)
Development of a 3D place and route tool
3D sequential can combine any CMOS from bulk planar to Finfet or FDSOI…
FDSOI and 3D integration can respond to future neuromorphic and quantum computing approaches

Non-charge based Memories

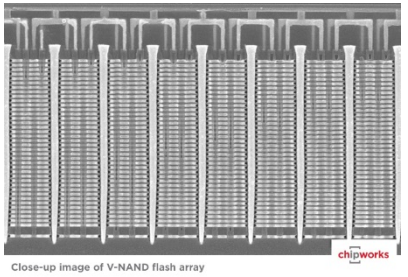
Topic « NVM » (1/2)



- SCM



- Embedded memory (IoT)



- Stand-alone

- **Stand-alone is pure 3D NAND-Flash.**
- **Emerging NVM aims at SCM** (memory btw DRAM and storage) **and embedded for automotive or IoT.**
- **New disruptive app like neuromorphic…**

5 years	OxRAM and CBRAM	PCM	MRAM	FeFET
Main key research issues	**Variability** Work on cell structure Improve materials	**Current consumpt.** Work on thermal confinement, GST etching	**Process complexity** Process improvements and machine improvement	Increase of ΔVth Variability control Physics understanding
Technology and design challenges	**Confinement of CF** and definition of new applications	Thermal improvement: **heater structure and GST etching**	**Scalability** Work on material.	Widen the material screening in addition to the standard Si:HfO2

5 years	Embedded and IoT	SCM
Potential for applications	**integration at scaled node <28nm scaled SoC** **automotive application**	**Applications on PC, tablet, phones, consumer markets, High speed computation, Fast boot** Recovery after power loss

Topic « *NVM*» (2/2)

10 years	OxRAM and CBRAM	PCM	MRAM	FeFET
Main key research issues	**Variability** Encapsulation or new material	**Scaling**	**Scaling under 14nm**	**Increase of ΔVth Variability control Physics understanding**
Technology/design challenges	Confinement of CF and definition of new appli	**Integrability <28nm**	**Magnetic stability**. New interfaces	

10 years	Embedded and IoT	SCM
Potential for applications	**Scaling of cunsumption. Voltage and current**	First demonstrators

	2023	2026	2029	2033
dMain FoMs				
• **BER** • **Endurance** • **Retention** • **Forming voltage (for OxRAM)**	BER<1E-6 (w/0 ECC) >1E5 10Y@85C and soldering reflow compliant <3V			BER<1E-6 (w/0 ECC) >1E6 (for SCM >1E10) 10Y@85C and soldering reflow compliant <2V

Global recommendation:

*OxRAM, HRS broadening is the Challenge. New materials, new programming schemes need to be investigated

*CBRAM, same as OxRAM plus a special focus on data retention, which is probably the most challenging topic for CBRAM

* PCM, needs to progress on integration, necessary for GST patterning. In addition, material research needs to be continued to optimize data retention for scaled nodes

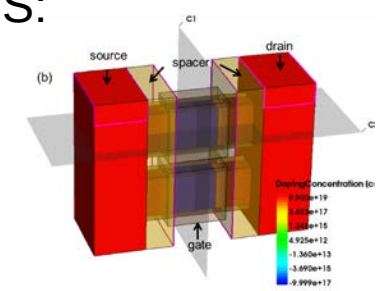
* MRAM, etching, thus integration, problems can be much harder to solve than expected. The high current consumption can be a serious drawback for real applications, in particular for IoT

* FeFET, widen the material screening in addition to the standard Si:HfO2. A lot of work is necessary on the interface between channel and Fe layer.

Modeling/Simulation

Topic « *Modeling and Simulation* » (1/2)

- Scenarios for nanoCMOS:
  - New materials
  - Complex 3D devices
  - Vertical stacking
  - Steep slope



[S.Jin, SISPAD 2016]

Wishlist for M&S (in general):
- **proof of concept of new devices, benchmarking and screening of technology options, assessment up to circuit level (DTCO)**
- **assist interpretation of experimental data and extraction of physically meaningful parameters**
- **it should be predictive of trends and actual absolute average values and variability**

❖ 1. Key research topics or issues

- Enablers : Bias dependent full-bands of confined materials ((s)SiGe, (s)Ge, III-V, CNT, 2D)

- Device architectures (with parasitics) and new channel materials (FDSOI/FinFET → GAA, NW, NSH, stacked...)

- Modeling variability and reliability, process modelling, DTCO (new materials/architectures)

- Modeling novel steep-slope device concepts for ULP electronics (and related materials)

- Medium term: 5+: **multi-valley/subband electrostatics of multilayer structures** including wave-function penetration, transport models comprehensive of tunneling and all relevant scattering (remote-X, SR), degradation mechanisms and models, defects, traps, variability in wire-like devices (selected materials)
- Long term: 10+ **: multi-scale implementations** (transfer to TCAD), **ac/transient regimes** (with q.m. effects)

❖ 2. Potential for application or Application needs and Impact for Europe

Accelerate development of ULP technologies, Reinforce modeling SME ecosystem, transfer of tools to industry

- Medium term: 5+ : **Further growth of M&S including SME ecosystem**
- Long term: 10+ : Consolidation of TCAD SMEs, **maintain high quality education for nanoelectronics**, attract bright minds to Europe

Topic « *Modeling and Simulation» (2/2)*

- 3. Technology and design challenges

Model verification (including, but not limited to, experimental calibration) at different levels of physical detail

- 4. Definition of FoMs (quantitive or qualitative) or planned evolution

Physical device dimensions and computational dimensionality of manageable problems (e.g.: length, cross section, volume, no. of materials, regions, atoms, eigenstates, particles, wall clock time, CPU time)

  - Medium term: 5+ : steadily improving - Long term: 10+ : steadily improving

- 5. Other issues and challenges, and interaction with other Tasks/WPs

Modeling for memory technologies, Modeling for steep slope devices, Modeling for power devices (automotive, energy), Modeling for large scale arrays of sensing elements integrated onto CMOS

  - Medium term: 5+ : «material» properties, new physics (SiC, GaN, Ferro/Piezo-electrics, … Electrolytes, analytes, etc.)
  - Long term: 10+ : Develop predictive and accurate TCAD solutions for industrial use

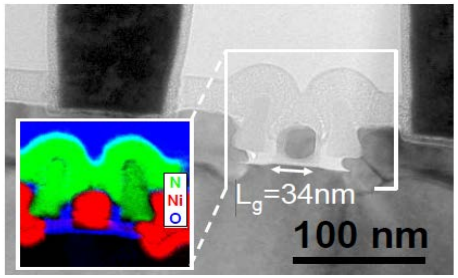
GLOBAL RECOMMENDATIONS:
- Promote dedicated M&S projects in application areas of interest for the European nanoelectronics (ULP electronics, power devices, nano-bio sensing, neuromorphic memory, quantum computing, etc…) **- Identify M&S needs well in advance, systematically devote adequate share of resources, also by embedding modeling in all technology projects**
- Priviledge approaches that account for arbitrary geometry and all relevant physics, e.g. multi-scale, valley, subband, electrostatics of layered structures with wavefunction penetration, transport models comprehensive of tunneling and all relevant scattering mechanisms (remote-X, SR)

Characterization

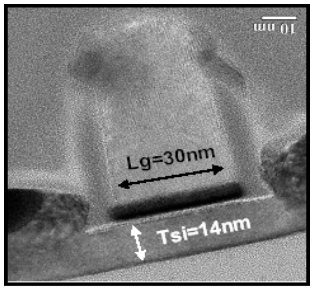
New challenges in electrical characterization

CMOS technologies evolve from bulk to FDSOI/FinFET and NWs:

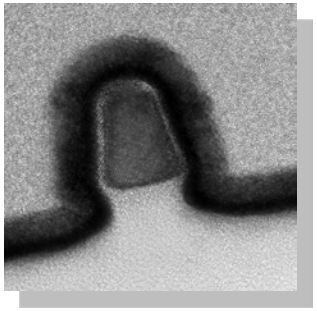
- **Improved electrostatic control,**
- **Better scalability and lower variability ?…**
- **But increasing issues of transport and interfaces in UTB and new materials….**



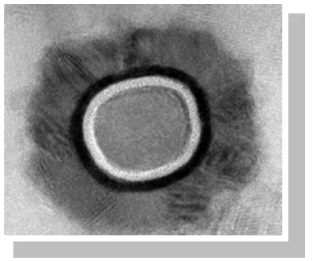
Bulk 28



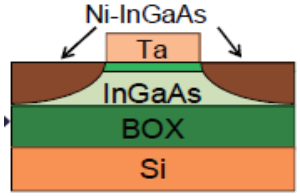
FDSOI



FinFET
Tri-Gate

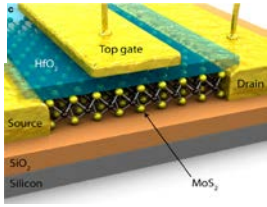


GAA NW



III-V

2D mat



New challenges in electrical characterization

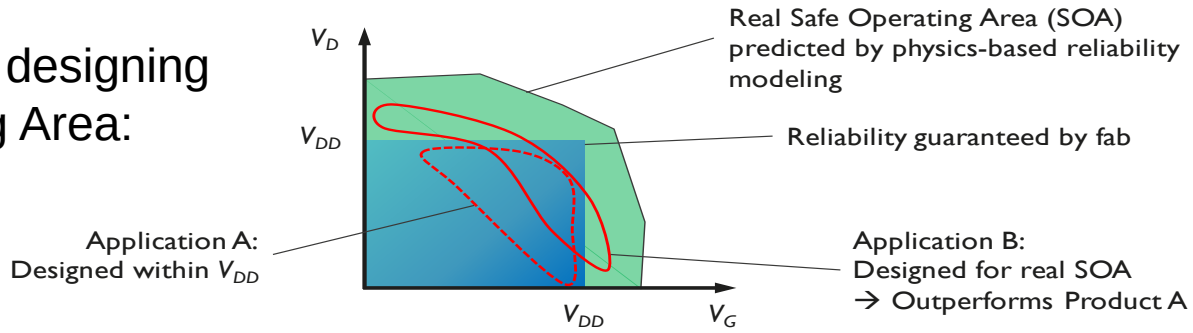
Main issues:

- **CV measurements still feasible using specific test structures (multi fingers or RFCV) on FDSOI, FinFET, NWs…**
- **MOSFET parameter extraction still applicable with new methods and on new 2D materials, III-V, Ge,… Rsd is a key parameter…**
- **Mobility and transport parameters still measurable on standard MOSFETs down to very small Lg but MR very useful tool…**
- **Traps and interface quality can be assessed even on very small area devices using LFN/RTN (C-V, CP area limited unless multi finger use)**
- **Stochastic Variability becomes critical and must be measured in static and in dynamic => problems for non mature technologies but also for TFET, FeFET….**

Reliability

Topic « *reliability* » (1/2)

Illustration of benefit of designing for real Safe Operating Area:



❖ 1. Key research topics or issues

-Physical properties of gate oxide defects responsible for the main degradation mechanisms in existing and novel material systems

-Impact of gate oxide defects on characteristics of existing and novel architecture devices

-Device carrier transport and energy distribution modeling

-Temperature profiles inside devices

-Development of reliability-enabled compact models

❖ 2. Potential for application or Application needs and Impact for Europe

Leveraging the full potential of the devices during application design

- Medium term: 5+ : Development of methodologies to propagate defect properties to lifetime projections and SOA determination
- Long term: 10+ : Acceptance and standardization of methodologies by the semiconductor industry

Topic « *reliability* » (2/2)

❖ 3. Technology and design challenges

-Experimental extraction of statistically significant defect properties

-Computational complexity of reliability enabled TCAD

-Development of reliability-enabled compact models

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

-Full reliability models accurately reproducing mean shifts and distributions in main device parameters, including Vth, SS, gm, Ion, in VG and VD and temperature accelerated testing

-Reliability-enabled compact models

-Computationally manageable reliability-enabled TCAD models

GLOBAL RECOMMENDATIONS:

-Consistently include reliability as a key FoM during novel device design and down-selection
-Dedicate adequate resources to reliability parameter extraction, modeling, and testing in both existing and new material systems
-Promote projects dedicated to reliability enabling collaboration of a broad spectrum of expertise, including physicists, material scientists, technologists, TCAD engineers, and designers
-Develop methodology to propagate reliability to higher application design abstraction layers

Conclusion

Main Recommendations for the most promising technologies for medium and long term Logic and Memory applications presented:

- Nanowire FET
- FD SOI MOSFET
- FinFET
- NCFET
- CNTFET
- Memories: OxRAM, CBRAM, PCM, MRAM, FeFET
- 3D sequential integration
- Modelling/Simulation, Characterization and Reliability