



NanoElectronics Roadmap for Europe: Identification and Dissemination

2nd General Workshop
Athens, April 6-7, 2017

WP5/Task.5.1



Top-Down Approach: first draft



2nd General Workshop– Athens April 6-7, 2017

WP5/Task5.1 – Danilo Demarchi

Aeneas Strategic Agenda



Design Technology is the essential link between the ever-increasing technology push (More Moore (MM) and More-than-Moore (MtM)) and the new products and services required to fulfil societal needs for mobility, security, health, communication, education, digital life style, and safety.

Competitive Value and Grand Challenges

- ❖ To compete with low labour-cost countries, it is of topmost importance for Europe:
 - to develop and offer **sophisticated feature-rich innovative products** with the superior performance and quality needed **to justify a higher price tag**
 - **Time-to-market** is of crucial importance
- ❖ A seamless, open and extendable design ecosystem with
 - **standards which starts at system level**
 - **flexible design flows** for all design domains and heterogeneous subsystems
 - **(co-)design** with and for sophisticated feature-rich innovative products of superior performance and quality
- ❖ Design Technologies apply also to
 - **heterogeneous devices** comprising power
 - **AMS and communication subsystems** (RF or optical)
 - **sensors and actuators** (e.g. MEMS) based on mixed

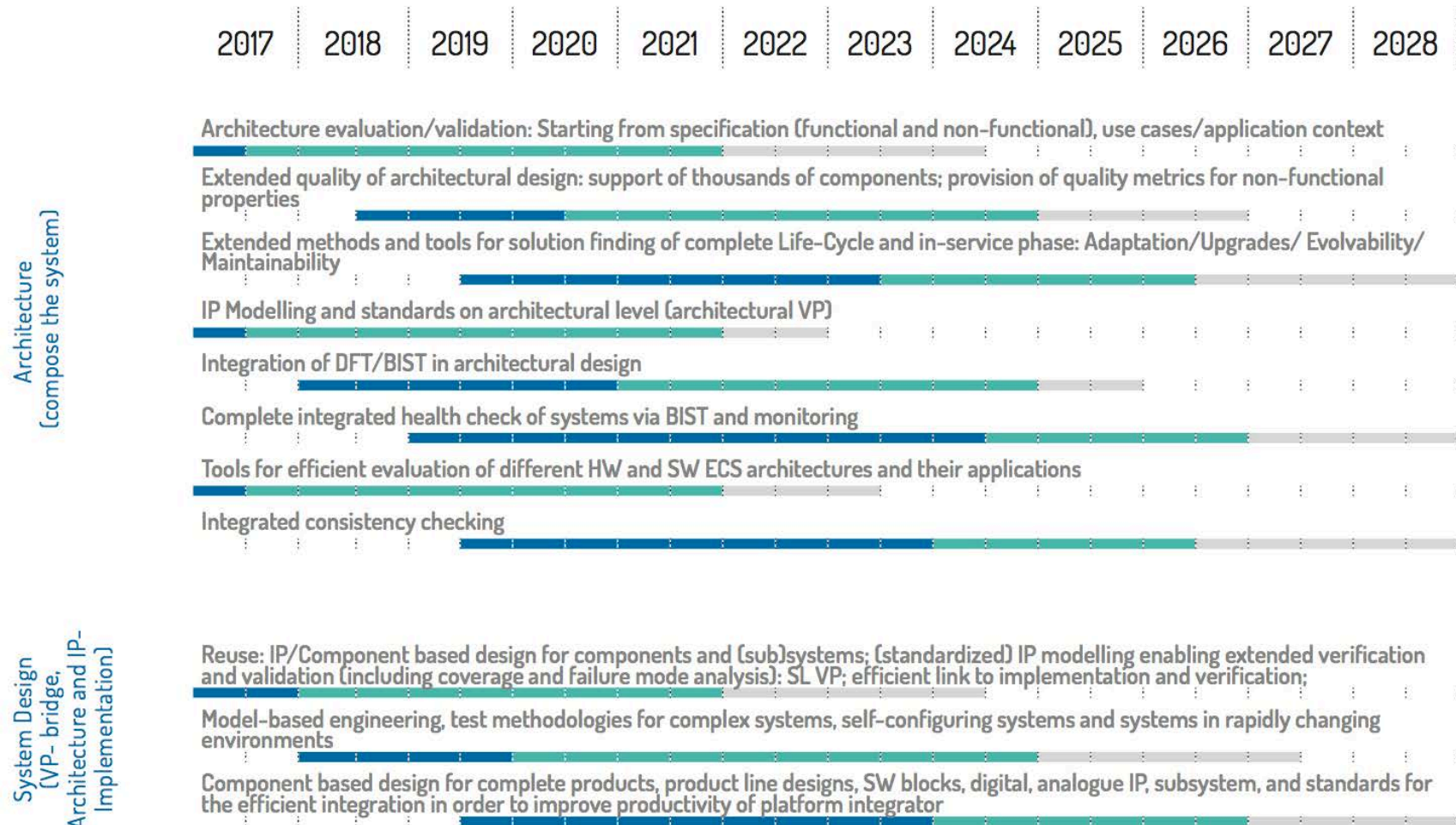
The 3 Grand Challenges

- 1) Managing Complexity
- 2) Managing Diversity
- 3) Managing Multiple Constraints

Designing these highly integrated and complex products requires improved methods for:

- ❖ On-chip integration
- ❖ Verification
- ❖ Embedded Software
- ❖ Technology downscaling

Examples from Aeneas Roadmap





**Outcomes from the Experts
at Domain Workshop in Lausanne
March 31, 2017**



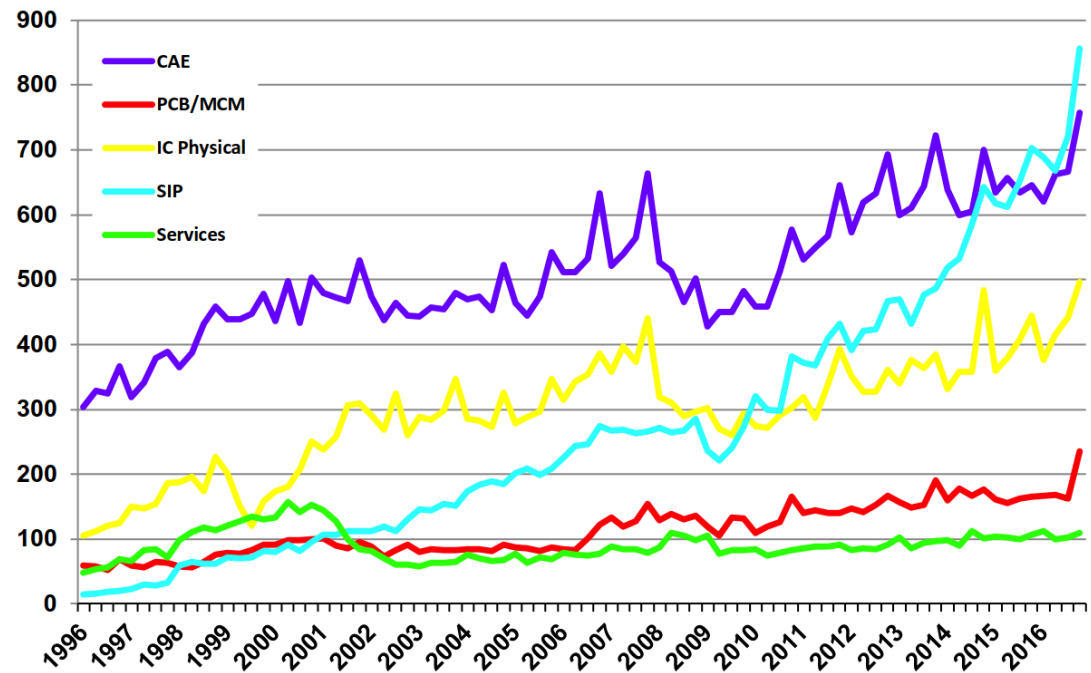
Inputs from Industrial Co-Leader Ralf Pferdmenges, Infineon

❖ New technologies like AI, machine learning, neural networks... will change how we will design in the future

➤ Europe should be one of the early users of these new technologies and their potential

❖ Growing activities and importance of SIP (System IP)

Quarterly EDA, SIP and Services Revenue by Category, Q1 1996 – Q4 2016



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Most Important Outcomes

- ❖ Add **Software** in the middle, starting from the Application
- ❖ **The value is not in the Device but the Data**, the Information at Systemic Level
- ❖ **Validation**: Level of Robustness that is Acceptable, Confidence => **When is it done?**
- ❖ **Balance** of how much happens at each node and the energy for transmission (for reliability/security reasons too)
 - Where to position the intelligence
 - From Embedded Computing to Embedded Intelligence
- ❖ Definition of **Standards** for Interoperability. openness of standard cannot prevent monetisation.

Most Important Outcomes

❖ Re-Usability / Reconfigurability

- Software-like re-programmability with (almost) hardware like efficiency

❖ Energy

- Management
- Consumption when is necessary only
- Importance of categorizing the application in terms of Energy Boundaries

❖ Automated Design Space Exploration and Automated Design Decisions

❖ From Connected Devices to Distributed Embedded Systems (System of Systems) => Network Synthesis, Network is a Design Dimension

❖ Very Good opportunity for Europe to drive the increase in System Knowledge

Most Important Outcomes

❖ Environment is Part of the System

❖ Simplify the list => Reduce the 1st level Concepts/Technologies => Decided to follow the scheme of Alex Yakovlev

- Functionalities:
 - Compute, Sense, Communicate, Store, Learn, AD Convert, DC-DC Regulate ...
- “Physicalities”:
 - Time, Power, Temperature, EM effects, Size, Technology nodes ...
- Criticalities:
 - Reliability, Performance, QoS, Cost, Autonomy, Survivability, Compatibility, Manufacturability, Productivity ...
- Design Paradigms:
 - Codesign(s), Low Power, Real-Time, Real-Power, Model-based, Reconfigurable, Scalable ...
- Design Activities:
 - Specification, Modelling, Analysis, Simulation, Optimization, Testing & Validation, Prototyping, ...



The New Map



Interfaces/Communications
Functional Specs
Computing/Storing Capabilities
Sensing Capabilities
Learning Capabilities
Autonomy

Functionalities

Physicalities

Energy/Power
Response Time
Form Factor
Temperature
EM Effects
Technology Nodes/Impact

Criticalities Opportunities

Manufacturability
Cost
System Level Reliability
Timeline
Lifecycle
QoS
Compatibility/Standardisation
Security (hacking)
Safety
Privacy

Application Aware
HW/SW Co-Design

Design Activities

Testing & Validation
MultiPhysical Modelling/Simulation
MultiParametric Analysis
Optimization
Prototyping

Design Paradigms

Reconfigurability/Flexibility
Artificial Intelligence/Neuromorphic
Energy Aware and Energy Driven Design
Design for IP

Functionalities

i) Functionalities		
a) Key research questions or issues		
<i>Functional Specs</i>		
<i>Interfaces/Communications</i>		
<i>Computing/Storing Capabilities</i>		
<i>Sensing Capabilities</i>		
<i>Learning Capabilities</i>		
<i>Autonomy</i>		
b) Potential for application or Application needs and Impact for Europe		
c) Technology and design challenges		
<i>Functional Specs</i>		
- What to Measure		
- What to Calculate		
- How Well		
<i>Interfaces/Communications</i>		
- Hardware		
- Software		
- External		
- Internal		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Beyond CMOS, WP2		
Advanced Logic and Connectivity, WP 3		
Functional Diversification, WP4		
Heterogeneous Integration, Task 5.2		

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Functionalities

c) Technology and design challenges		
<i>Functional Specs</i>		
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- How Well		
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Physicalities

ii) Physicalities		
a) Key research questions or issues		
<i>Energy/Power</i>		
<i>Response Time</i>		
<i>Form Factor</i>		
<i>Temperature</i>		
<i>EM Effects</i>		
<i>Technology Nodes/Impact</i>		
b) Potential for application or Application needs and Impact for Europe
c) Technology and design challenges
<i>Energy/Power</i>		
- Profile of Energy Sources		
- Energy Transparency (requested energy)		
- Low Consumption		
<i>Form Factor</i>		
- Size		
- Footprint		
- Dimensionality		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
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Heterogeneous Integration, Task 5.2		

Physicalities

c) Technology and design challenges	..
<i>Energy/Power</i>	
- Profile of Energy Sources	
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Heterogeneous Integration, Task 5.2	

Criticalities / Opportunities

iii) Criticalities/Opportunities		
a) Key research questions or issues		
<i>Manufacturability</i>		
<i>Cost</i>		
<i>System Level Reliability</i>		
<i>Timeline</i>		
<i>Lifecycle</i>		
<i>QoS</i>		
<i>Compatibility/Standardisation</i>		
<i>Security (hacking)</i>		
<i>Safety</i>		
b) Potential for application or Application needs and Impact for Europe		
c) Technology and design challenges		
<i>Manufacturability</i>		
- Technical		
- Cost		
- Material Availability		
<i>Lifecycle</i>		
- Duration		
- Recycling		
<i>Security (hacking)</i>		
- Trusted Executing Environment		
- Design for Security		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Advanced Logic and Connectivity, WP 3		
Functional Diversification, WP4		
Heterogeneous Integration, Task 5.2		
Equipment and Manufacturing, WP6		

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Criticalities / Opportunities

c) Technology and design challenges
Manufacturability
- Technical
- Cost
- Material Availability
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Design Paradigms

iv) Design Paradigms		
a) Key research questions or issues		
<i>Reconfigurability/Flexibility</i>		
<i>Artificial Intelligence/Neuromorphic Computing</i>		
<i>Energy Aware and Energy Driven Design</i>		
<i>Design for IP</i>		
b) Potential for application or Application needs and Impact for Europe		
c) Technology and design challenges		
<i>Reconfigurability/Flexibility</i>		
- Hardware		
- On Site Reconfigurability (Critical? Safe?)		
- Closed-loop Adaptation		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
e) Other issues and challenges, and interaction with other Tasks/WPs.		

Design Paradigms

c) Technology and design challenges
<i>Reconfigurability/Flexibility</i>
- Hardware
- On Site Reconfigurability (Critical? Safe?)
- Closed-loop Adaptation
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)
e) Other issues and challenges, and interaction with other Tasks/WPs.

Design Activities

v) Design Activities		
a) Key research questions or issues		
<i>Testing & Validation</i>		
<i>MultiPhysical Domain Modelling and Simulation</i>		
<i>MultiParametric Analysis</i>		
<i>Optimization</i>		
<i>Prototyping</i>		
b) Potential for application or Application needs and Impact for Europe		
c) Technology and design challenges		
<i>Testing & Validation</i>		
- For Manufacturing		
Device Level		
Process Level		
- For Functionality		
Reliability		
Safety		
Security		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Functional Diversification, WP4		
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Design Activities

c) Technology and design challenges		
Testing & Validation		
- For Manufacturing		
Device Level		
Process Level		
- For Functionality		
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d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
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Functional Diversification, WP4		
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Thank you!

