

# NanoElectronics Roadmap for Europe: Identification and Dissemination

2<sup>nd</sup> General Workshop Athens, April 6-7, 2017

WP5/Task.5.1



# **Top-Down Approach: first draft**





#### **Aeneas Strategic Agenda**



Design Technology is the essential link between the ever-increasing technology push (More Moore (MM) and More-than-Moore (MtM)) and the new products and services required to fulfil societal needs for mobility, security, health, communication, education, digital life style, and safety.



#### **Competitive Value and Grand Challenges**

- To compete with low labour-cost countries, it is of topmost importance for Europe:
  - > to develop and offer **sophisticated feature-rich innovative products** with the superior performance and quality needed **to justify a higher price tag**
  - > Time-to-market is of crucial importance
- A seamless, open and extendable design ecosystem with
  - > standards which starts at system level
  - > flexible design flows for all design domains and heterogeneous subsystems
  - (co-)design with and for sophisticated feature-rich innovative products of superior performance and quality
- Design Technologies apply also to
  - ➤ heterogeneous devices comprising power
  - > AMS and communication subsystems (RF or optical)
  - > sensors and actuators (e.g. MEMS) based on mixed



#### The 3 Grand Challenges

- 1) Managing Complexity
- 2) Managing Diversity
- 3) Managing Multiple Constraints

Designing these highly integrated and complex products requires improved methods for:

- On-chip integration
- Verification
- Embedded Software
- Technology downscaling



#### **Examples from Aeneas Roadmap**

Architecture (compose the system) 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028

Architecture evaluation/validation: Starting from specification (functional and non-functional), use cases/application context

Extended quality of architectural design: support of thousands of components; provision of quality metrics for non-functional properties

Extended methods and tools for solution finding of complete Life-Cycle and in-service phase: Adaptation/Upgrades/ Evolvability/ Maintainability

IP Modelling and standards on architectural level (architectural VP)

Integration of DFT/BIST in architectural design

Complete integrated health check of systems via BIST and monitoring

Tools for efficient evaluation of different HW and SW ECS architectures and their applications

Integrated consistency checking

System Design (VP- bridge, Architecture and IP-Implementation)

Reuse: IP/Component based design for components and (sub)systems; (standardized) IP modelling enabling extended verification and validation (including coverage and failure mode analysis): SL VP; efficient link to implementation and verification;

Model-based engineering, test methodologies for complex systems, self-configuring systems and systems in rapidly changing environments

Component based design for complete products, product line designs, SW blocks, digital, analogue IP, subsystem, and standards for the efficient integration in order to improve productivity of platform integrator





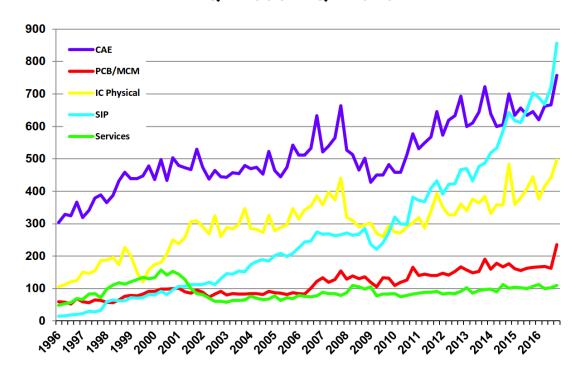
# Outcomes from the Experts at Domain Workshop in Lausanne March 31, 2017



#### Inputs from Industrial Co-Leader Ralf Pferdmenges, Infineon

- New technologies like AI, machine learning, neural networks... will change how we will design in the future
  - Europe should be one of the early users of these new technologies and their potential
- Growing activities and importance of SIP (System IP)

Quarterly EDA, SIP and Services Revenue by Category, Q1 1996 – Q4 2016





#### **Most Important Outcomes**

- Add **Software** in the middle, starting from the Application
- The value is not in the Device but the Data, the Information at Systemic Level
- Validation: Level of Robustness that is Acceptable, Confidence => When is it done?
- ❖ Balance of how much happens at each node and the energy for transmission (for reliability/security reasons too)
  - ➤ Where to position the intelligence
  - > From Embedded Computing to Embedded Intelligence
- Definition of Standards for Interoperabilty. openess of standard cannot prevent monetisation.



#### **Most Important Outcomes**

- Re-Usability / Reconfigurability
  - > Software-like re-programmability with (almost) hardware like efficiency
- Energy
  - Management
  - Consumption when is necessary only
  - > Importance of categorizing the application in terms of Energy Boundaries
- Automated Design Space Exploration and Automated Design Decisions
- From Connected Devices to Distributed Embedded Systems (System of Systems) => Network Synthesis, Network is a Design Dimension
- Very Good opportunity for Europe to drive the increase in System Knowledge



#### **Most Important Outcomes**

- Environment is Part of the System
- ❖ Simplify the list => Reduce the 1<sup>st</sup> level Concepts/Technologies => Decided to follow the scheme of Alex Yakovlev
  - Functionalities:
    - Compute, Sense, Communicate, Store, Learn, AD Convert, DC-DC Regulate ...
  - "Physicalities":
    - Time, Power, Temperature, EM effects, Size, Technology nodes ...
  - Criticalities:
    - Reliability, Performance, QoS, Cost, Autonomy, Survivability, Compatibility, Manufacturability, Productivity ...
  - Design Paradigms:
    - Codesign(s), Low Power, Real-Time, Real-Power, Model-based, Reconfigurable, Scalable ...
  - Design Activities:
    - Specification, Modelling, Analysis, Simulation, Optimization, Testing & Validation, Prototyping, ...





# The New Map



Interfaces/Communications
Functional Specs
Computing/Storing Capabilitie
Sensing Capabilities
Learning Capabilities
Autonomy

Criticalities
Opportunities

Manufacturability

Cost

System Level Reliability

Timeline

Lifecyle

QoS

Compatibility/Stansardisation

Security (hacking)

Safety

Privacy

Functionalities

Physicalities

Energy/Power
Response Time
Form Factor
Temperature
EM Effects
Technology Nodes/Impact

Application Aware HW/SW Co-Design

Design Paradigms

Reconfigurability/Flexibility
Artificial Intelligence/Neuromorphic
Energy Aware and Energy Driven Design
Design for IP

Design Activities

Testing & Validation
MultiPhysical Modelling/Simulation
MultiParametric Analysis
Optimization
Prototyping

#### **Functionalities**

i) Functionalities	_	
a) Key research questions or issues		
Functional Specs		
Interfaces/Communications		
Computing/Storing Capabilities		
Sensing Capabilities		
Learning Capabilities		
Autonomy		
b) Potential for application or Application needs and Impact for Europe		
c) Technology and design challenges		
Functional Specs		
- What to Measure		
- What to Calculate		
- How Well		
Interfaces/Communications		
- Hardware		
- Software		
- External		
- Internal		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
e) Other issues and challenges, and interaction with other Tasks/WPs.		
Beyond CMOS, WP2		
Advanced Logic and Connectivity, WP 3		
Functional Diversification, WP4		
Heterogeneous Integration, Task 5.2		



#### **Functionalities**

c) Technology and design challenges		
Functional Specs		
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Energy/Power		
Response Time		
Form Factor		
Temperature		
EM Effects		
Technology Nodes/Impact		
b) Potential for application or Application needs and Impact for Europe		
c) Technology and design challenges	Ī	Ī
Energy/Power		
- Profile of Energy Sources		
- Energy Transparency (requested energy)		
- Low Consumption		
Form Factor		
- Size		
- Footprint		
- Dimensionality		
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)		
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Heterogeneous Integration, Task 5.2		



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# **Criticalities / Opportunities**

iii) Criticalities/Opportunities	
a) Key research questions or issues	
Manufacturability	
Cost	
System Level Reliability	
Timeline	
Lifecyle	
QoS	
Compatibility/Stansardisation	
Security (hacking)	
Safety	
b) Potential for application or Application needs and Impact for Europe	
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c) Technology and design challenges  Manufacturability	
- Technical	
- Cost	
- Material Availability	
Lifecyle	
- Duration	
- Recycling	
Security (hacking)	
- Trusted Executing Environment	
- Design for Security	
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Equipment and Manufacturing, WP6	
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# **Design Paradigms**

iv) Design Paradigms	
a) Key research questions or issues	
Reconfugurability/Flexibility	
Artificial Intelligence/Neuromorphic Computing	
Energy Aware and Energy Driven Design	
Design for IP	
b) Potential for application or Application needs and Impact for Europe	
c) Technology and design challenges	
Reconfugurability/Flexibility	
- Hardware	
- On Site Reconfigurability (Critical? Safe?)	
- Closed-loop Adaptation	
d) Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)	
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### **Design Paradigms**

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On Site Reconfigurability (Critical? Safe?)	
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# **Design Activities**

New research questions or issues		
Testing & Validation  AutiPhysical Domain Modelling and Simulation  AutiPhysical Domain Modelling and Simulation  Diptimization  Diptimization  Diptimization or Application needs and Impact for Europe  District of application or Application needs and Impact for Europe  Device Level Process Level For Functionality Reliability Safety Security  Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  Dother issues and challenges, and interaction with other Tasks/WPs.  Functional Diversification, WP4  Leterogeneous Integration, Task 5.2	v) Design Activities	_
MultiPhysical Domain Modelling and Simulation MultiParametric Analysis  Iptimization Pototyping  In Petential for application or Application needs and Impact for Europe  In Technology and design challenges In Security  Device Level Process Level Process Level Process Level Profunctionality Reliability Security  In Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  In Other issues and challenges, and interaction with other Tasks/WPs.  Junctional Diversification, WP4 Interogeneous Integration, Task 5.2	a) Key research questions or issues	
AultiParametric Analysis  Definization  Trototyping  Definization or Application needs and Impact for Europe  Technology and design challenges  Testing & Validation  For Manufacturing  Device Level  Process Level  For Functionality  Reliability  Safety  Security  Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  Other issues and challenges, and interaction with other Tasks/WPs.  Functional Diversification, WP4  Reterogeneous Integration, Task 5.2	Testing & Validation	
Prototyping  Description  Prototyping  Description  Technology and design challenges  Pesting & Validation  For Manufacturing  Device Level  Process Level  For Functionality  Reliability  Safety  Security  Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  Of Other issues and challenges, and interaction with other Tasks/WPs.  Functional Diversification, WP4  Reterogeneous Integration, Task 5.2	MultiPhysical Domain Modelling and Simulation	
Potential for application or Application needs and Impact for Europe    Technology and design challenges	MultiParametric Analysis	
Deposition of Potential for application of Application needs and Impact for Europe  Technology and design challenges  Testing & Validation  For Manufacturing  Device Level  Process Level  For Functionality  Reliability  Safety  Security  Definition of FoMs (quantative or qualitative) or planned evolution (based on SoA @ 2017 and evolution vs time)  Other issues and challenges, and interaction with other Tasks/WPs.  Functional Diversification, WP4  Reterogeneous Integration, Task 5.2	Optimization	
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# **Design Activities**

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# Thank you!



