WP4 Functional diversification
Task 4.2 Smart Energy

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2nd General Workshop Session 2

Athens April 6-7, 2017

Task 4.2 Smart Energy

Industrial Co-Leader			
WP4	4.2 Smart Energy	W. Dettmann	Infineon
General and Domain Workshops			
WP4	4.2 Smart Energy	Mikael Östling	KTH
WP4	4.2 Smart Energy	Steve Stoffels	IMEC
Domain Workshops			
WP4	4.2 Smart Energy	Gaudenzio Meneghesso	UniPD
WP4	4.2 Smart Energy	Peter Moens	On Semi
WP4	4.2 Smart Energy	Joff Derluyn	EpiGaN
WP4	4.2 Smart Energy	Anton Bauer	Fraunhofer IISB
WP4	4.2 Smart Energy	Thomas Harder	ECPE Directoe
WP4	4.2 Smart Energy	Thomas Detzel	Infineon Villach
WP4	4.2 Smart Energy	Peter Steeneken	NXP
WP4	4.2 Smart Energy	Giuseppe Croce	STMicroel
WP4	4.2 Smart Energy	Braham Ferreira	TU DELFT

WORKSHOP Bertinoro

	NEREID Workshop 4 – Task 4.2 “Smart Energy” Chairman: Gaudenzio Meneghesso – IUNET Italy
09:00 – 09:10	Gaudenzio Meneghesso, University of Padova “Opening of the Workshop”
09:10 – 09:30 09:30 – 09:50 09:50 – 10:10 10:10 - 10:30	Mikael Östling, KTH, “SiC power switch device status and predictions”. Peter Moens, ON Semi “Status and oulook of GaN power devices from an industry perspective” Giuseppe Croce, STMicroelectronics “Smart Power Technology Roadmap and Trends” Thomas Detzel, Infineon "GaN in a Silicon world: Competition or Coexistence?"
10:30 – 11:00	Break
11:00 – 11:20 11:20 – 11:40 11:40 – 12:00 12:00 – 12:20 12:20 – 12:40	Joff Derluyn, EPIGAN, “GaN from the epitaxy perspective” Steve Stoffels, IMEC “Outlook for 200mm E-mode device technology” Anton Bauer, Fraunhofer IISB “Potential of SiC for Automotive Power Electronics” Thomas Harder, ECPE, "WBG System Integration" Braham Ferreira, TU Delft “International Technology Roadmap for Wide Band-gap Power Semiconductor ITRW”
12:40 – 14:00	Lunch
14:00 – 17:30	Discussion for road-mapping ONLY for NEREID experts and members Coffee break during the discussion

The story…

Global Warming

Energy Conservation

Renewable Energy

Improving the Efficiency

Electrical Conversion

Power Devices

At least 50 % of the electricity used in the world is controlled by Power Devices.

B.J. Baliga, Advanced High Voltage Power Device Concepts, Springer

Lead Applications for SiC & GaN (CLINT/ECPE Roadmap Workshop, 4/10/16)

World-wide Market for Medium-Voltage Power Electronics due to the Energy Transition

Source	Cumulated installed power until 2050	Annual replacement in 2050
Solar (50% MV)	2.500 GW	250 GW
Wind on-shore (50%)	2.500 GW	250 GW
Wind off-shore (100%)	500 GW	50 GW
Battery power (50%)	1.000 GW	125 GW
Elektrolysers (100%)	500 GW	75 GW
HVDC (100%)	250 GW	30 GW
Over all	7.250 GW	780 GW

- Figures based on internal studies

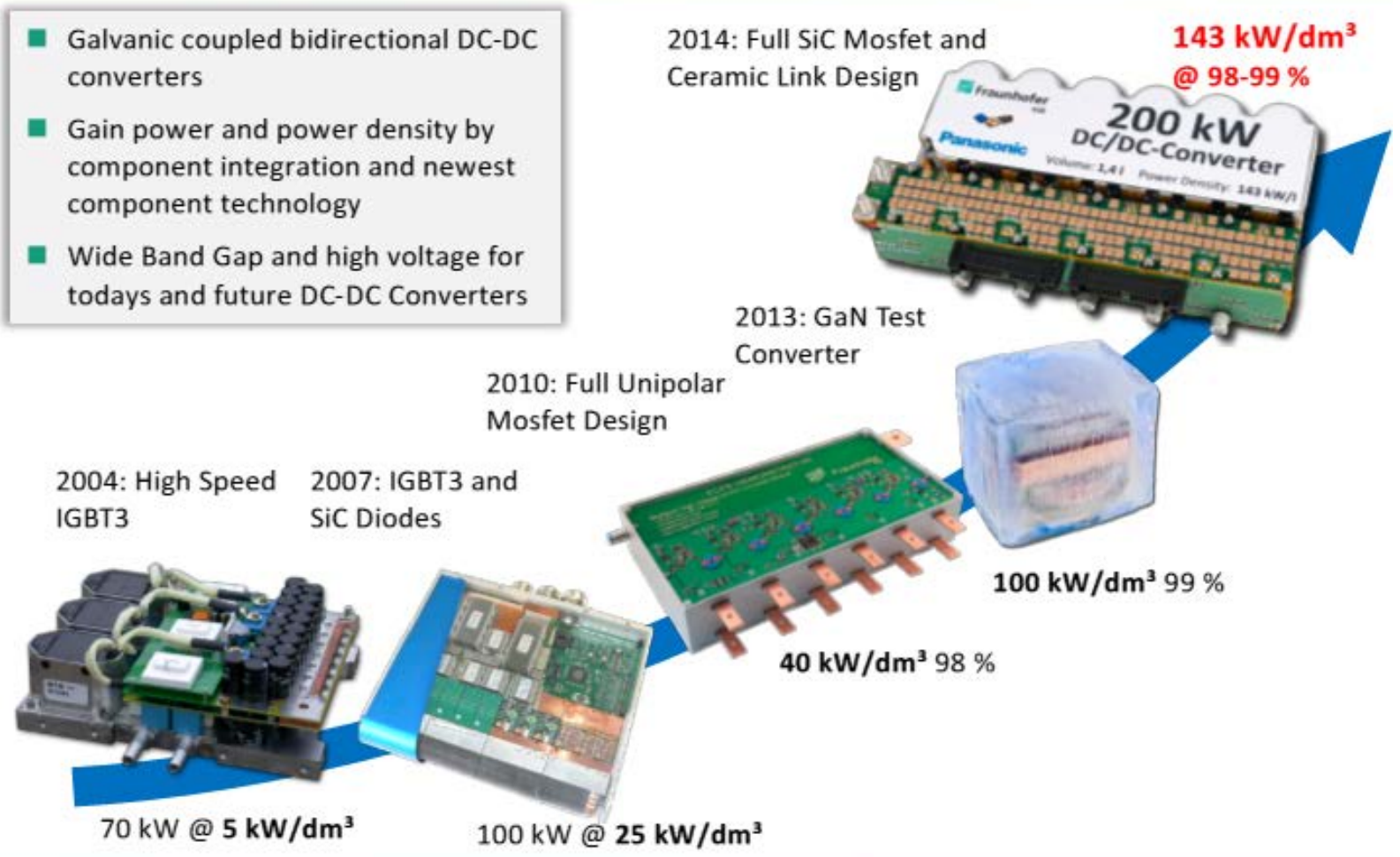
Source: B. Burger, Fraunhofer ISE, Industriearbeitskreis Mittelspannungs-Leistungselektronik, 19.09.2016 in Berlin

The potential …

Gain Power Density by WBG

Fraunhofer IISB

- Galvanic coupled bidirectional DC-DC converters
- Gain power and power density by component integration and newest component technology
- Wide Band Gap and high voltage for todays and future DC-DC Converters



System benefit …

Mobile Systems: Automotive

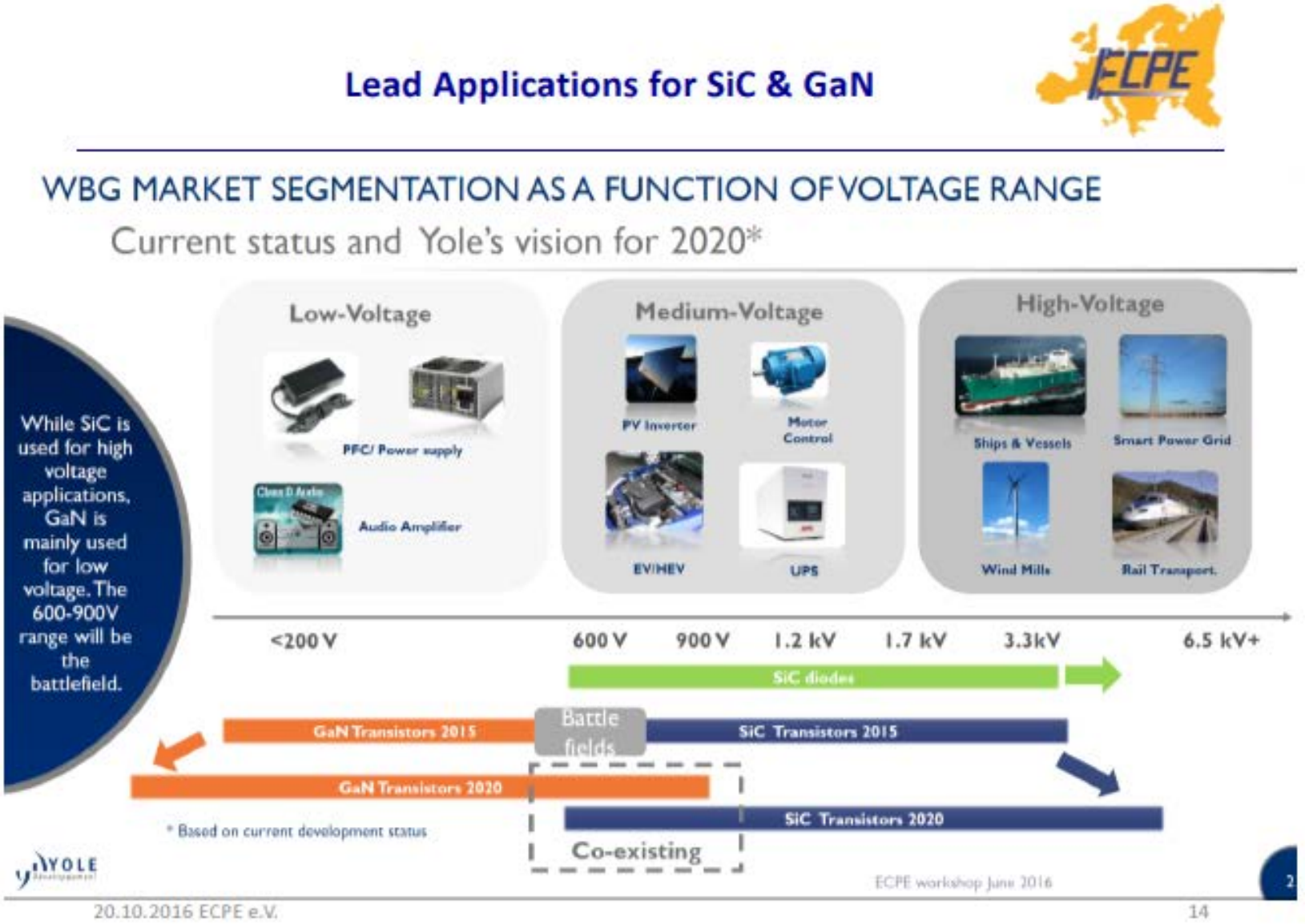
- Any mobile system should benefit
  - Higher efficiency is higher range or smaller storage
  - Smaller volume and lower weight of the converter and cooler
  - By leverage effect even smaller volume and lower weight of the storage
- Good example is Toyota
  - 10% fuel savings targeted, 5% achieved on prototypes already
  - Power control unit down to 20% of volume, weight from 18kg down to 4kg
  - On the market in 2020

Source: Toyota

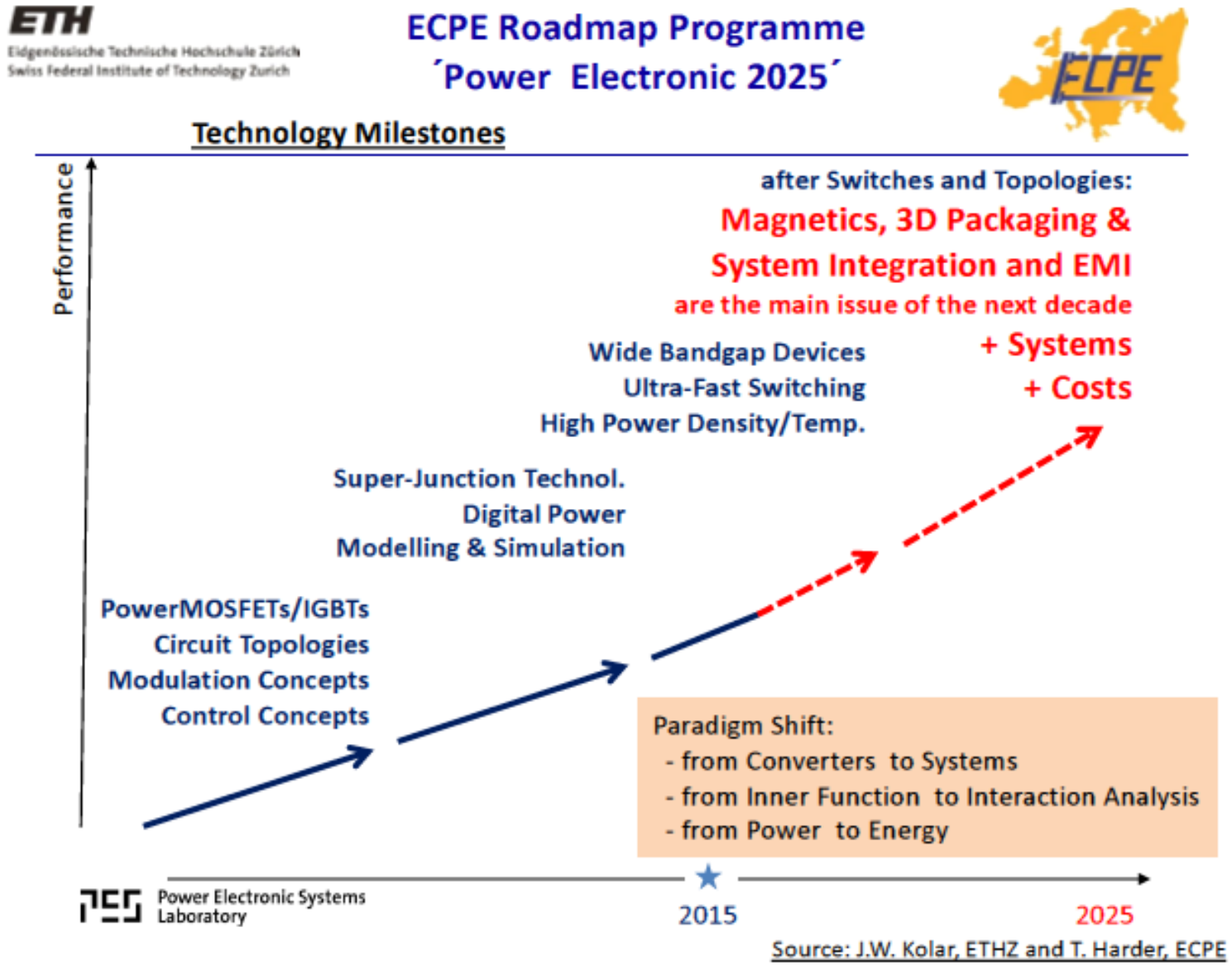
Universität Bremen

Source: ECPE Roadmap Workshop ´Power Electr. 2025´, Munich, 26.03.2015

Co-existing & dedication…



Roadmaps…


ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
ECPE Roadmap Programme
´Power Electronic 2025´
ECPE
Technology Milestones
Performance
after Switches and Topologies:
Magnetics, 3D Packaging &
System Integration and EMI
are the main issue of the next decade
+ Systems
+ Costs
Wide Bandgap Devices
Ultra-Fast Switching
High Power Density/Temp.
Super-Junction Technol.
Digital Power
Modelling & Simulation
PowerMOSFETs/IGBTs
Circuit Topologies
Modulation Concepts
Control Concepts
Paradigm Shift:
- from Converters to Systems
- from Inner Function to Interaction Analysis
- from Power to Energy
Power Electronic Systems Laboratory
2015
2025
Source: J.W. Kolar, ETHZ and T. Harder, ECPE

WP4 Energy diversification

- WP4 will define the **strategy** for a roadmap for those **technologies** that **extend the field of application** of semiconductor technologies by **adding new functionalities or extend application range**.
- These technologies, falling under the denomination of “More than Moore”, do not scale simply with geometrical size, and are widely diversified; **therefore new metrics will have to be identified for the roadmap**. It includes two main Tasks:
- T4.1 Smart Sensors
- **T4.2 Smart Energy**

Task 4.2 Smart Energy : WBS

wide band-gap semiconductors:

Fast switching is the key for **size and weight reduction** with WBG power semiconductors **leading to several issues**: **EMC, low parasitic inductances of the packaging and interconnection technologies, power losses related to passive components, need for system integration solutions, optimised switching cell, integrated drivers**, ...

As a consequence, the extreme miniaturization of power electronic systems leads to **higher power density** which requires **new improved cooling techniques**, but also leads to higher operation (and junction) temperature.

Issues related to high temperature power electronics: advanced materials and processes for **packaging** and **interconnection** (chip level and system level), **polymer moulding & encapsulation**, substrates, **temperature range for passive components**, **robustness and reliability**, ...

Task 4.2 Smart Energy: Objectives

- To identify the **best application of Power Si and wide band-gap semiconductors** devices (WBS) and provide a clear indication on **where these devices will be disruptive** in their applications;
- Highlight all the **technological** and **material** issues that need to be solved in order to guarantee a large market penetration of these devices;
- To provide a roadmap for the “standard” Si-based technology and the market penetration of WBS devices taking into account **cost/benefit analysis**, the degree if maturity and its expected evolution.

Task 4.2 : Issues

Highlight all the **technological** and **material** issues that need to be solved in order to guarantee a large market penetration of these devices;

Technological and material issues

- Material (substrates, quality, reproducibility, supply chain, wafer size, maximum thickness for heteroepitaxial growth)
- Processing issues (contacts, gate, isolation)
- Normally off operation (hybrid or intrinsic)
- Isolated gate (MIS) devices
- Sustainable breakdown, Operational (rated) voltage
- Robustness (UIS, short circuit) & Reliability
- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)ù
- Gate drivers
- …….

Task 4.2 : Roadmap

- To provide a roadmap for the standard Si-based technology and the market penetration of WBS devices taking into account **cost/benefit analysis**, the degree of maturity and its expected evolution.

Roadmap and cost/benefit for WBS

- Large wafer sizes, multi-wafer reactors
- New circuit topologies
- Novel device topologies (lateral vs vertical)
- Novel substrates (bulk GaN/alternative carriers)
- Reliability and stability of WBS
- New technologies at the interfaces for lower costs and higher reliability

Key figures of merit devices :

Device level

- Normally off – Vth > 2V
- Low gate leakage at maximum gate voltage
- Breakdown Voltage 650 V, 1200 V devices
- Ron vs Qg (efficiency vs speed)
- Dyn $R_{DS,ON}$ < 20% at maximum voltage
- Reliability/robustness > 20year
- Maximum operating channel temperature

System level point of view:

- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)
- Gate drivers

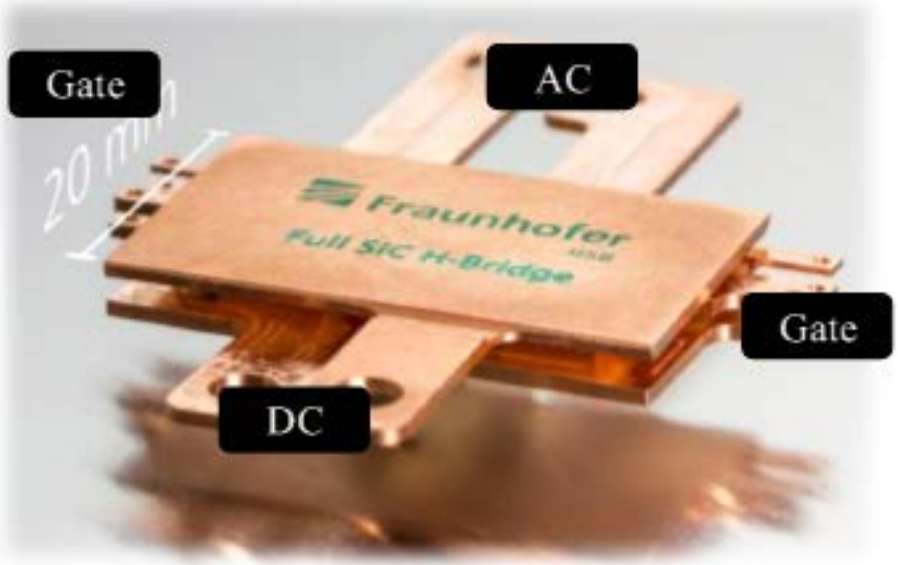
SiC

Technical Trends in SiC

Fraunhofer IISB

Innovative Modul Design

- Full Bridge - Busbar SiC-Modul
- Technologies
  - Chip on Busbar
  - Double Side Silver Sintering
- Module Data
  - max. 80A / 600V (1200V)
  - SiC-FETs
  - Silicium Puls Capacitors
  - Ultra Low Inductance
- Concept
  - Modular: H-/Half Bridge
  - Double Side Cooling
  - Small Dimensions



Roadmap

SiC Device Roadmap

Going for more technological maturity

Going for more compactness for power converters

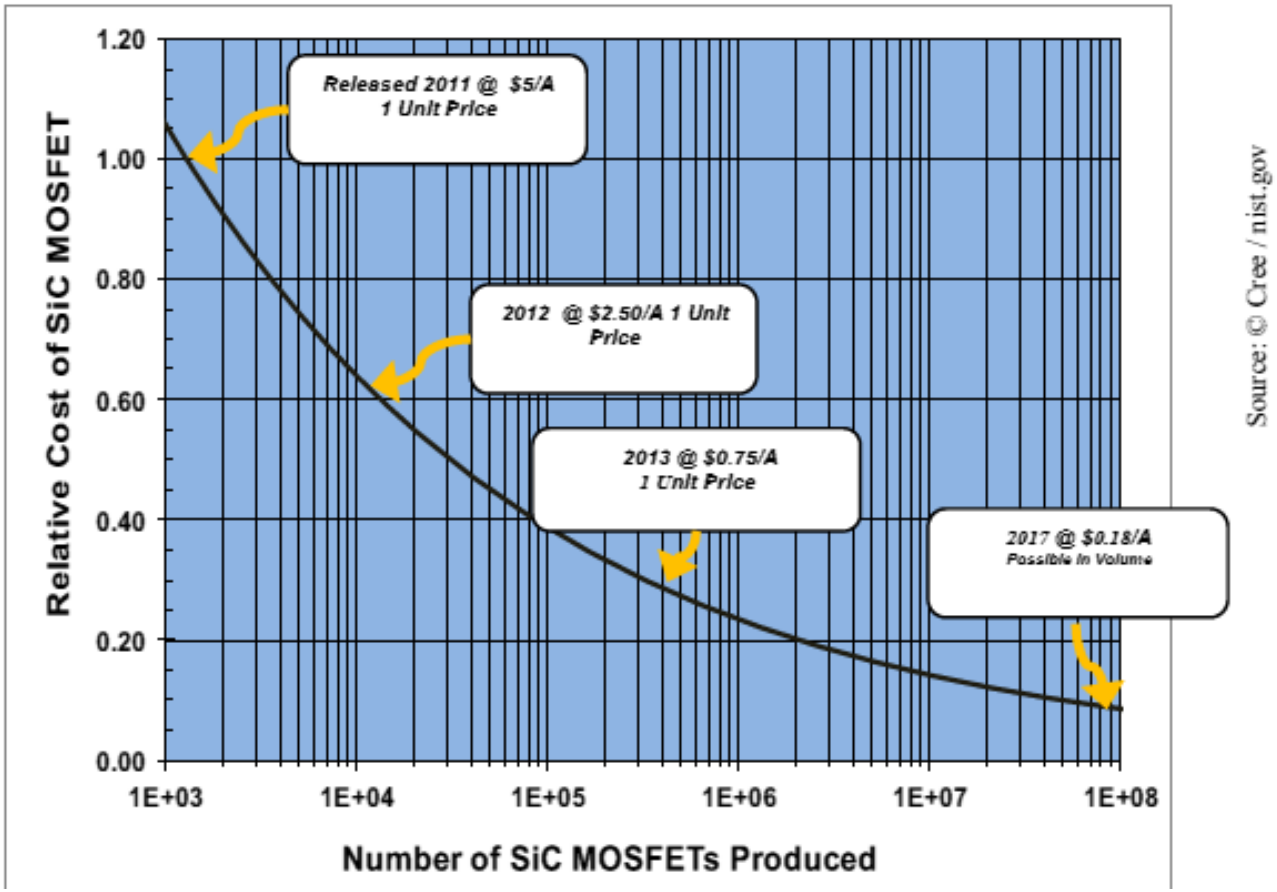
Years	Si 4.5 kV IGBT or BIGT	4H-SiC 1.2 - 1.7 kV MOSFET JFET/BJT	4H-SiC 3.3 kV MOSFET	4H-SiC 6.5 kV MOSFET IGBT	4H-SiC 10.0 kV MOSFET IGBT	4H-SiC 15.0 kV IGBT	4H-SiC 20 – 30 kV IGBT GTO	AlN/ Diamond 30 – 50 kV IGBT/GTO
2016	√√√	√√	√	x	x	x	x	x
2018	√√√	√√√	√√	√	x	x	x	x
2020	√√√	√√√	√√	√	√	x	x	x
2022	√√√	√√√	√√√	√√	√√	√	√	x
2024	√√√	√√√	√√√	√√√	√√√	√√√	√√	√

x Fundamental potential exist but technological solution is not ready yet
√ Engineering die samples available. Probably not qualified chip. Complete package solution may not be ready yet.
√√ Qualified chip ready. Complete package solution probably ready to be tested in the field.
√√√ Fully mature and qualified chip is available along with qualified packaged power module to be tested in the field.

Source: Dr. Muhammad Nawaz, ABB, ESCDERC 2016 but modified

Costs…

Technical Trends in SiC



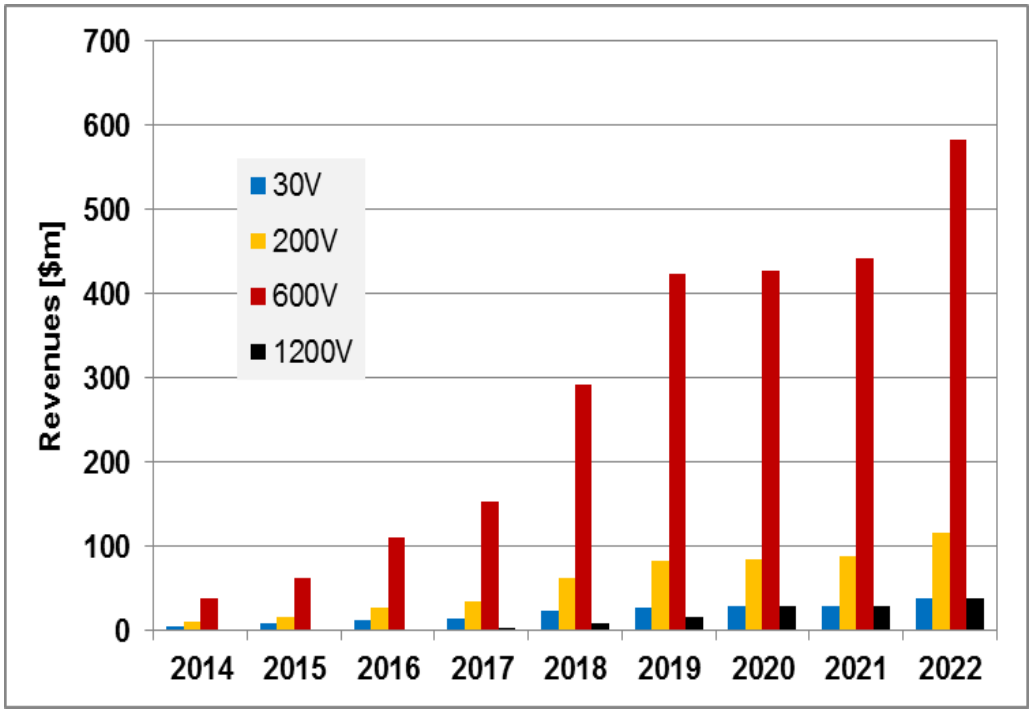
SiC summary…

Summary

- Replacing Si with SiC switch devices gives great savings with respect to energy density, efficiency, and physical systems volume
- At 1200-1700V SiC MOSFETs, JFETs and BJT performs about equally good
- In a few years the cost issues with SiC looks very competitive < 5 cents/Amp
- Above 15 kV, BJTs/IGBTs are likely to be the first choice
- For high temperature and radhard environments BJTs have a clear advantage

Task 4.2: GaN outlook

- Total Power Semiconductor market ~25B$
  - Si SuperJunction market ~2.2B$ in 2020
  - IGBT market ~1B$ in 2020
- By 2020, GaN is expected (hoped) to take 25% of Si SJ market **[but depends on when cost parity with Si is achieved]**



Task 4.2: GaN roadblocks

- Customers want cost parity at the device level
  - Replace e.g. Si SJ device by a GaN device that yields at par or better system efficiency
- GaN-on-Si wafer cost is (too) high
  - Multi-wafer reactors/New concepts
  - Growth on CTE matches substrates (poly-AlN, …)
  - Others….to reduce growth time and Defect Density
  - 150mm versus 200mm (vs 300 mm ?)
- GaN Reliability is different from Si (JEDEC) and is not well enough understood—Need standardisation
  - JEDEC is a minimum requirement, but we need more (GaN specific testing like Dyn Ron, hard switching testing, surge current capability etc)

Task 4.2: status GaN-on-Si

Threats/weaknesses:

- The buffer stack is critical
  - Causes limitations for breakdown, current collapse, RF loss
- High density of threading dislocations & point defects
  - Critical threshold values to achieve reliable devices have not been identified
  - Mechanisms not fully understood
- Drive towards thicker epilayers for power
- Cost roadmap

Strengths/Opportunities:

- Main (proven?) choice for power, increasing interest for RF
- Scaling diameter is on-going (now at 200mm)
- Si fab compatibility
  - substrate thickness and contamination
- Easy back-side processing
  - E.g. TSV, local substrate removal, replacing Si by diamond
- Novel integration options, e.g. through SOI, 3D stacking, …
  - Gate drivers, RF digital front end and RF filters, …

Task 4.2: development

- Quality improvement for enhanced reliability
  - Reduction of TD density
    - Nucleation, buffer designs
  - Understanding of fundamental behaviour
    - structural & crystal investigations
    - Modelling
- Higher voltage: thicker / better buffers
  - 600V -> 900V -> 1200V
- Low Rsheet heterostructures
  - E.g. InAlN ~ 220 Ohm/sq
- Selective regrowth
  - n-GaN for ohmic contacts
  - p-GaN for e-mode gates, vertical transistors
  - For combined GaN/CMOS
  - Requires integration in device process flow

Task 4.2: imec GaN Program

HIGH LEVEL PLAN OF GAN TECHNOLOGY AT IMEC

TARGETING SHORT AND LONG TERMS NEEDS OF GAN