NEREID

2° General Workshop, Athens, April 2017

« Nanoscale FET » Roadmap

WP3 – Task 3.1

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NanoElectronics Roadmap for Europe: Identification and Dissemination

HORIZON 2020

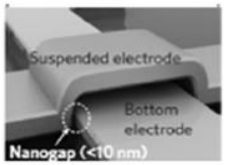
Coordinators of the sub-Tasks

- **FD-SOI:** Stephane Monfray, STMicroelectronics
- **FinFET:** Anda Mocuta, IMEC
- **Nanowires:** Lars-Erik Wernersson, Lund University
- **Memories,** Carlo Cagli, LETI
- **Tunnel FET:** Kirsten Moselund, IBM Zurich
- **3D Sequential Integration:** Claire Fenouillet, LETI
- **Modelling/Simulation tools:** Luca Selmi, Udine University
- **Characterization Tools:** Gerard Ghibaudo, Grenoble INP/CNRS

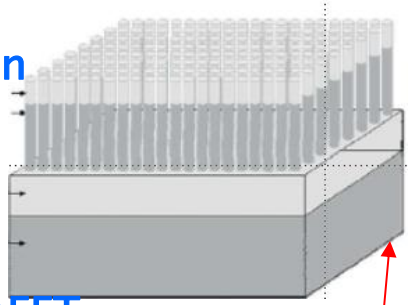
Nanoscale FET roadmap for low energy, scaling, high perf., new functionalities

… IC evolution …

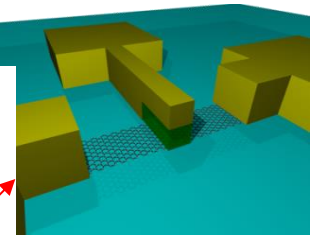
NEMS



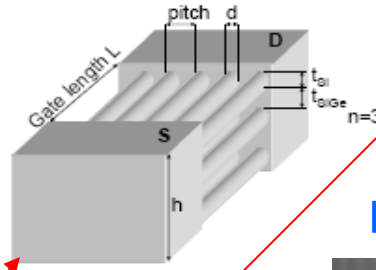
NW/Carbon-based MtM



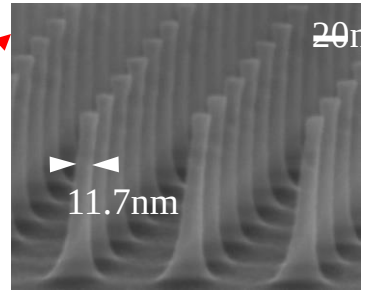
Nanosheet/2D-FET

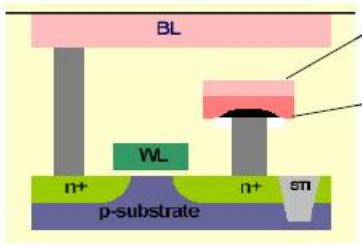


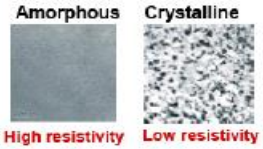
3D-NW



Lateral/Vertical

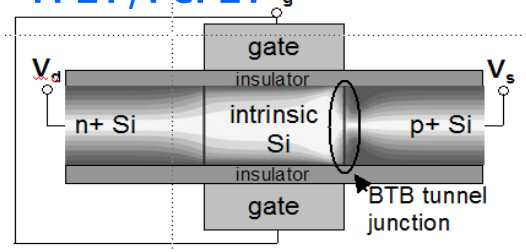






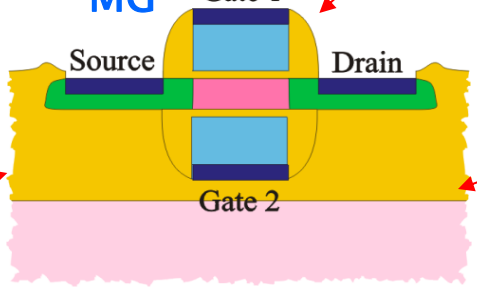
Non-charge/ PCRAM

TFET/FeFET

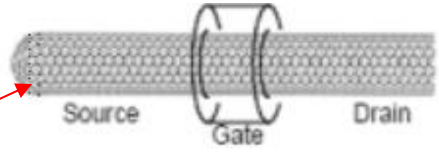


NW/NVM

MG

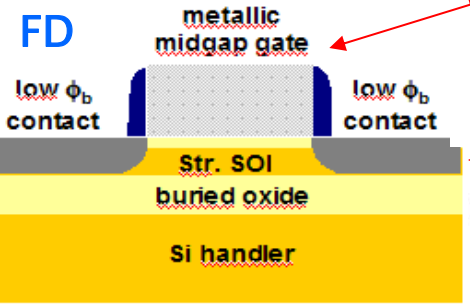


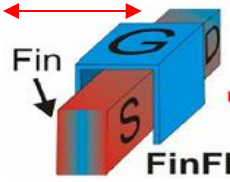
MC

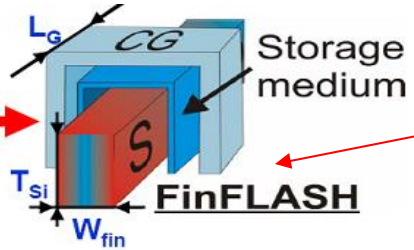


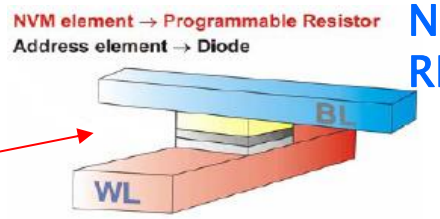
CNT

FD









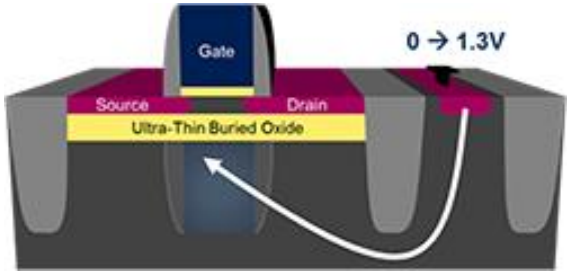
Non-charge/ RRAM

… IC evolution …

FD-SOI

Topic « *FDSOI* » (1/2)

- Principle



- FD-SOI technology enables control of the behavior of transistors not only through the gate, but also by polarizing the substrate underneath the device, similarly to the **body bias** available in Bulk technology
- **more power / lower leakage** /wider range of operation down to lower voltages
- The **manufacturing process for FD-SOI is much simpler** than alternatives

❖ 1. Key research questions or issues

-Improving performances (strain technologies for Higher drive current, Si & BOX thickness reduction, new materials (GeOI, III-V OI) and 3D integration)

-Design evolutions exploiting back biasing techniques

-Differentiation: FDSOI Logic & embedded flash memories for IoT / Automotive applications

- Medium term: 5+: **dual stressors on sSOI wafers, Tsi<6nm, Tbox<15nm, development of planar nanosheet devices** (2 channels), **ULP IoT** dedicated design **Vd=0,4V**, PCM, monolithic 3D
- Long term: 10+ : **Tsi<5nm, Tbox<10nm, 3D multi-layers nanosheet devices with new materials, Vd<0,4V,** monolithic 3D with high-mobility materials, new flash memories

❖ 2. Potential for application or Application needs and Impact for Europe

Low power devices for automotive, IoT and future non CMOS computing

- Medium term: 5+ :Embedded flash for Automotive, **ULP devices (wearable IoT, GPS, connected watches)**
- Long term: 10+ : **New sensors (environment), ULP for medical IoT, neuromorphic & Quantum computing**

Topic « *FDSOI*» (2/2)

❖ 3. Technology and design challenges

Develop Integration of Strain SOI substrates (processing of tensile strain for NMOS & compressive strain for PMOS), Compatibility with low power flash memories, FDSOI design with Vdd<0,4V, Integration with new materials (SiGe with high Ge content) and III-V materials in 3D process

- Medium term: 5+ : Local strain N & P, PCM integrated with FDSOI, Subthreshold circuits, High Ge SiGeOI
- Long term: 10+ : Development of solutions for sub-60mV/dec devices, 3D III-V OI circuits at prod level

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

Ieff/Ioff,, Variability (Avt), Vdd, Subthreshold slope

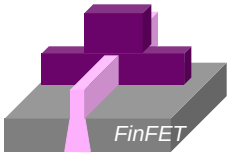
- Medium term: 5+ : Ieff 470/ 420 µA/µm , 10nA/µm Ioff , <1mV.µm, **<0,75V, <70mV/dec**
- Long term: 10+ : Differentiation through options, <0.8mV.µm, **<0,5V, <65mV/dec**, Introduction of sub-60mV/dec technologies

❖ 5. Other issues and challenges, and interaction with other Tasks/WPs.

FIRST GLOBAL RECOMMENDATIONS
Develop differentiated options (RF, Embedded Memories) on FDSOI (applications for automotive, IoT)
Develop ULP design (Vd<0,4V) for IoT market (wearable, medical…)
From device architecture point of view, FDSOI technology can suit 14nm & 10nm nodes
FDSOI and 3D integration can respond to future neuromorphic and quantum computing approaches

FinFET

Topic: FINFET



❖ 1. Key research questions or issues

- subthreshold slope control **to less than 70mV/dec at very short gate length (<14nm)**
- **improved device performance (Ion/Ieff at given Ioff) while scaling the gate length and pitch**
- **control of parasitic capacitances** at scaled dimensions
- **Variability control** at very scaled dimensions
  - Medium term: 5+: innovation needs to continue in the following areas: contact resistivity, conformal doping, dopant activation above solid solubility limit, low k or air spacer; HKMG scaling and multi-Vt; high mobility channels; channel strain enhancement; integration of taller fins**; understand under what conditions nanowires will outperform finfets**; **Co-integration with other device architectures or between 2 channel materials**; **3Dsequential integration with other devices**
  - Long term: 10+ : Co-integration with other device architectures or between 2 channel materials; 3Dsequential integration with other devices

❖ 2.Potential for application or Application needs and Impact for Europe

- current workhorse device for Si CMOS technologies
- **current best option for high performance space**
- currently **can cover part of the low power/low cost space**
- can be **considered for quantum computing as qbits**
- specialty sensors

Topic: FINFET

3. Technology and design challenges

No single device/material able to replace Si CMOS; Co-integration of finfet with other device architectures or between different channel materials will be key; Improve finfet analog performance

- Medium term: 5+ develop **finfets that can be processed at low T**; develop finfets that **can withstand a long thermal cycle for 3D seq integration**;develop integration flows for **multiple channel materials and strain**(e.g. Si, SiGe, Ge, III-V)
- Long term: 10+ : develop **co-integration schemes between finFETs and nanowires/nanosheets**

4. Definition of FoMs (quantitive or qualitative) or planned evolution

Ion, Ieff, CV/I @ fixed Ioff; Ioff/GIDL, Subthreshold slope, Variability (Avt), Vdd,

- Medium term: 5+ : **Ion/Ieff/ CV/I improve 20%/2-3yrs**; Ioff/GIDL<10pA/um; **SS <70mV/dec**; Avt<1mV um; **Vdd<0.7V**
- Long term: 10+ : Ion/Ieff/ CV/I improve 20%/2-3yrs; Ioff/GIDL<10pA/um; SS <70mV/dec; Avt<0.8mV um; **Vdd<0.6V**

5. Other issues and challenges, and interaction with other Tasks/WPs

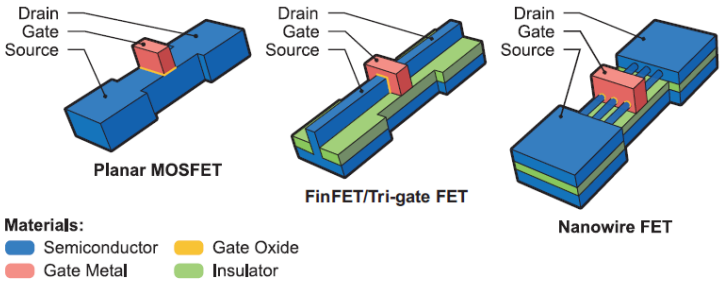
Manufacturing processes and integration will become very complex; working with increased aspect ratios will be key; system level studies to decide what are the best devices to be co-integrated and in what way, for a given application

FIRST GLOBAL RECOMMENDATIONS
Develop co-integration of different channel materials
Develop co-integration with other transistor architectures (nanowires, nanosheets, vertical devices)
Develop low thermal cycle finFETs for sequential integration
Develop low contact resistivity and high strain solutions
Develop low K spacer materials or airgap spacer
Improve finFET analog performance
Develop finFETs as devices for quantum computing

Nanowires

Topic « *NWs* » (1/2)

- Principle



Key advantages:
Advantageous transport
→ high transconduc. and I_{on}
Wrap-gate geometry
→ low output conduc. and DIBL
Band gap engineering
→ reduced I_{off}

❖ 1. Key research questions or issues

-What performance (Ion, Ioff, gm, ft/fmax, NF) can be achieved in different materials and geometries?

-Circuit/technology co-design in 3D transistor architectures

-Differentiation: Advantageous transport properties (III-Vs and Ge) combined with GAA for electrostatic control

- Medium term: 5+: Available data suggests that the best performance (lowest Ioff, highest Ion, highest gm, etc) is obtained for Si, Ge, and III-V nanowires.
- Long term: 10+ : Co-design transistor/circuit/technology for 3D structures

❖ 2. Potential for application or Application needs and Impact for Europe

Extend the roadmap for CMOS scaling based on improved electrostatic control and increased drive current

Enhance the CMOS RF & millimeter wave-properties by (III-V) materials integration

Medium term: 5+ :Introduction of **hybrid III-V/Si(Ge) and/or all-III-V technology for high-performance applications (both RF/mmWave and mixed-mode)**

Long term: 10+ : **Integration of high-speed logic** and high-performance front-ends **using III-V technology combined with CMOS and possible TFETs**

Topic « *NWs» (2/2)*

❖ 3. Technology and design challenges

- **Challenges in terms of 3D processing in complex geometries at 10 nm Lg**
- **3D transistors/circuits with nanowires stacked in 3D**
- Medium term: 5+ : Maturing of the process technology for Si, Ge and III-V nanowires to meet the requirements of IoT and high-performance applications
  - ➢ Long term: 10+ : Circuit layout in complex 3D architectures with minimized parasitics

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

- Ion, Ioff, gm, ft/fmax, NF
- Medium term: 5+ : Rapid development with current status: **Ion 650 µA/µm , 1nA/µm Ioff , > 500 GHz fmax**
  - ➢ Long term: 10+ : Further improvement in fmax and processing stability

❖ 5. Other issues and challenges, and interaction with other Tasks/WPs.

Strong interaction with TFETs and Connectivity

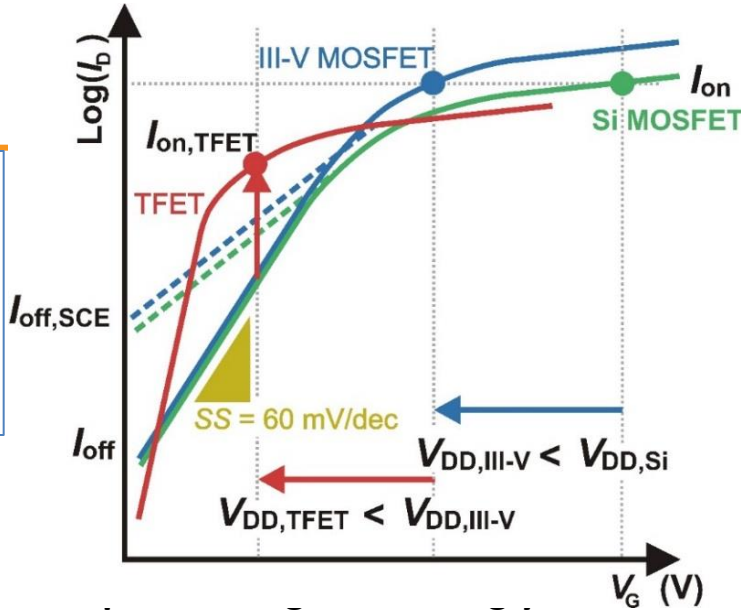
FIRST GLOBAL RECOMMENDATIONS
Develop millimeter wave front-ends with III-V MOSFETs (applications for communication, radar)
Develop transistor/circuit co-design strategies for mixed and mmW applications
Consider the 3D aspects of processing (stacking, vertical integrations etc) **Identify the best material and geometry options for logics (high-speed as well as low-power)**
The electrostatics and heterostructure design options provided are beneficial for TFETs

Tunnel FET

Topic « *Tunnel FET* » (1/2)

- Principle

  - Tunnel FETs (TFETs) are based on the quantum-mechanical phenomenon of tunneling through a barrier.
  - In theory **can achieve sub-thermionic sub-threshold swings, as they are not limited by diffusive transport.**
  - **Difficult to achieve simultaneously high I_{on} and steep subthreshold swing, SS.**



❖ 1. Key research questions or issues

- **Explore device architectures (NW, Airbridge, nanosheet, EHBTFET…)**
- **Understanding the role of traps in limiting TFET performance and how**
- **Demonstrating dense, scalable complementary TFET logic**
- **Explore scalability and limitations in terms of size, speed performance, noise, reliability**

  - Medium term: 5+: Demonstrate performance superior to MOSFET at low voltages, reduction of traps $D_{it}<5x10^{12}$ cm^{-2}, for all contributions (oxide, heterojunction etc. - challenging in III-Vs)
  - Long term: 10+ : Gate length scalability (limited by S to D tunneling), complementary and hybrid platforms.

❖ 2. Potential for application or Application needs and Impact for Europe

Low power devices for low- to mid-range frequency energy constrained IoT and computing. Strong European presence in TFET domain from simulation to device technology.

  - Medium term: 5+ : Exploit low leakage potential of TFETs, exploit T-independence of BTBT mechanism
  - Long term: 10+ : **Hybrid & heterogeneous systems, TFETs need III-Vs** → depend on III-V CMOS.

Topic « *Tunnel FET» (2/2)*

❖ 3. Technology and design challenges

- Non-standard CMOS → requires an ecosystem for III-V capability and integration opportunities.

- Complementary tunnel FET in other than Si technologies are technologically very challenging.

- Reliable TCAD, compact models and design tools which accurately capture behavior and does not require extensive tuning are needed to enable VLSI TFET designs. No design infrastructure for TFETs.

- Medium term: 5+ : Reliable compact models including heterojunctions, TFET design infrastructure.
- Long term: 10+ : III-V/Si(Ge) technology platforms enabled for III-V TFETs

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

I_{60}, Subthreshold swing, dynamic behavior, variability, noise

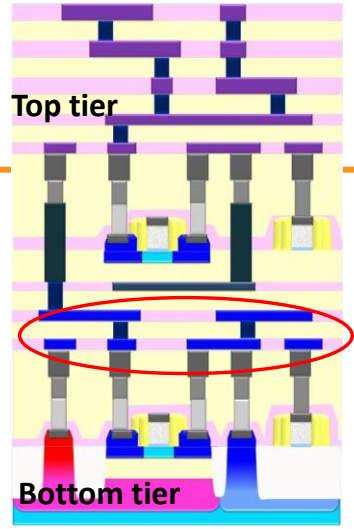
- Medium term: 5+ : **I_{60} =100 µA/µm @ SS<60mV/dec, V_{dd}<0.5V**, explore: dynamics, variability, noise
- Long term: 10+ : application specific, **I_{60} =500 µA/µm or SS<50mV/dec, ultra low power or mid-range applications.** Reliability

❖ 5. Other issues and challenges, and interaction with other Tasks/WPs.

FIRST GLOBAL RECOMMENDATIONS
Demonstrate TFETs with combined performance superior to MOSFETs at <0.5V
Develop understanding of the impact of traps and develop design and technology mitigation strategies.
Develop compact models and design tools including hetero-junctions and III-Vs
Evaluate performance beyond DC-IV: L_G scalability, speed, noise, variability, reliability…..
Establish foundry-level scalable complementary TFET platforms, preferably hybrid CMOS

3D sequential

Topic « 3D Sequential » (1/2)



- Principle
  - 3D sequential is an alternative to conventional device scaling.
  - Compared to TSV-based 3D ICs, 3D sequential process flow offers the possibility to stack devices with a lithographic alignment precision (few nm) enabling via density > 100 million/mm^2 between transistors tiers (for 14nm design rules).
  - Possibility to merge several technologies, material…

❖ 1. Key research questions or issues

- **Which applications will benefit from very high density interconnections:**
  - ➢ Medium term: **5+: For IoT: intelligent local processing of the data to decrease the bandwith of data transmission. Neuromorphic architectures.**
- **Thermal stable metallization with low resistance** (5+: Cu/ULK or W/ULK) (10+: Co, Silicided intercos)
- **Reliability for low temperature gate stack**
- **Low thermal cycle device temperature**
  - ➢ Medium term: 5+: **Same performance for top and bottom Mosfets**

❖ 2. Potential for application or Application needs and Impact for Europe

CMOS on CMOS for area scaling (5+: **SRAM memory** block to block) (10+: **Enabler for in memory computing architecture and neuromorphic**), **imager co-integrated with logic** (5+: 3D pixels for smart pixels with local memory storing) (10+: Smart pixels with local computing capabilities (each pixel will benefit from its local computing unit)), **Computation immersed in memory, Sensors and CMOS for IOT** (5+: NEMS, bolometers with the local analog parts with better performance than ASIC and better cost than co-integration) (10+: **multisensing platform**), **beyond CMOS devices co-integration with CMOS** (5+: introduction of **TFET, 2D TMD, graphene**) (10+: **Qubit addressing**)

Topic « *3D sequential*» (2/2)

❖ 3. Technology and design challenges

Design tools optimized for sequential 3D not available, reducing parasitics in each implementation (5+: Wire length decrease) (10+: material optimization)**, thermal management/self-heating mitigation** (5+: layout optimization) (10+: layout + heat spreaders + thermoelectric cooling, energy harvester)**, manufacturing challenges** (5+: same performance, same yield as 2D integration) (10+: Yield on multi-Tiers)

- Medium term: 5+ : Use of 2D existing tools to provide non fully optimized (fold or shrunk techniques) 3D place and route tools.
- Long term: 10+ : **Actual 3D place and route tools with 3D optimization at the logic gate scale.**

❖ 4. Definition of FoMs (quantitive or qualitative) or planned evolution

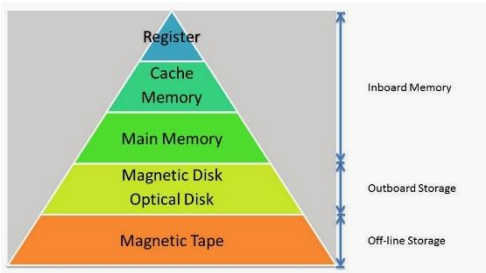
Top level device performance and reliability (5+: similar to 2D), contamination management (5+: In industrial fab with W or Cu intercos), **System level performance versus 2D or 3DTSV** (5+: same as 2D TSV) (**10+: > than 2D or 3DTSV**)**, System level area versus 2D or 3DTSV** (5+: same as 2D TSV) (**10+: < than 2D or 3DTSV**)**, System level cost comparison versus 2D or 3DTSV including yield** (5+: same as 2D TSV) (**10+: < than 2D or 3DTSV**)**, multi-tiers stacking** (5+: 2 tiers), (**10+: more than 2 Tiers**)**.**

❖ 5. Other issues and challenges, and interaction with other Tasks/WPs.

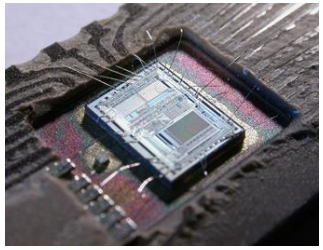
FIRST GLOBAL RECOMMENDATIONS
To define which applications will benefit from very high density interconnections (IOT, neuromorphic…)
Development of a 3D place and route tool
3D sequential can combine any CMOS from bulk planar to Finfet or FDSOI…
FDSOI and 3D integration can respond to future neuromorphic and quantum computing approaches

Non-charge based Memories

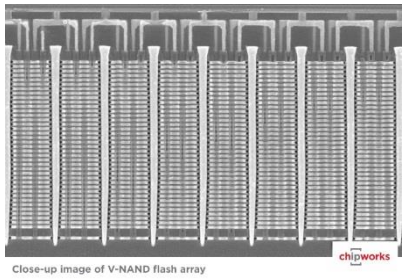
Topic « *NVM* » (1/2)



- SCM



- Embedded memory (IoT)



- Stand-alone

- **Stand-alone is pure 3D NAND-Flash.**
- **Emerging NVM aims at SCM** (memory btw DRAM and storage) **and embedded for automotive or IoT.**
- **New disruptive app like neuromorphic…**

5 years	OxRAM and CBRAM	PCM	MRAM
Main key research issues	**Variability** Work on cell structure Improve materials	**Current consumption** Work on thermal confinement, GST etching	**Process complexity** Process improvements and machine improvement
Technology and design challenges	**Confinement of CF** and definition of new applications	Thermal improvement: **heater structure and GST etching**	**Scalability** Work on material.

5 years	Embedded and IoT	SCM
Potential for applications	**integration at scaled node <28nm scaled SoC** **automotive application**(but spec need to be demonstrated)	**Applications on PC, tablet, phones, consumer markets** **High speed computation** **Fast boot** Recovery after power loss

Topic « *NVM*» (2/2)

10 years	OxRAM and CBRAM	PCM	MRAM
Main key research issues	**Variability** Encapsulation or new material	**scaling**	**Scaling under 14nm**
Technology and design challenges	Confinement of CF and definition of new applications	**Integrability <28nm**	**Magnetic stability**. New interfaces

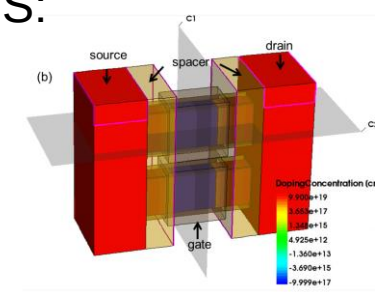
10 years	Embedded and IoT	SCM
Potential for applications	**Scaling of cunsumption. Voltage and current**	First demonstrators

Global recommendation:
OxRAM: HRS broadening is the Challenge. New materials, new programming challenges are required
PCM: process improvements necessary for GST patterning
MRAM: scalability is the issue. This requires new material enabling horizontal scaling

Modeling/Simulation

Topic « *Modeling and Simulation* » (1/2)

- Scenarios for nanoCMOS:
  - New materials
  - Complex 3D devices
  - Vertical stacking
  - Steep slope



[S.Jin, SISPAD 2016]

Wishlist for M&S (in general):
- **proof of concept of new devices, benchmarking and screening of technology options, assessment up to circuit level (DTCO)**
- **assist interpretation of experimental data and extraction of physically meaningful parameters**
- **it should be predictive of trends and actual absolute average values and variability**

❖ 1. Key research topics or issues

- Enablers : Bias dependent full-bands of confined materials ((s)SiGe, (s)Ge, III-V, CNT, 2D)

- Device architectures (with parasitics) and new channel materials (FDSOI/FinFET → GAA, NW, NSH, stacked...)

- Modeling variability and reliability, process modelling, DTCO (new materials/architectures)

- Modeling novel steep-slope device concepts for ULP electronics (and related materials)

- Medium term: 5+: **multi-valley/subband electrostatics of multilayer structures** including wave-function penetration, transport models comprehensive of tunneling and all relevant scattering (remote-X, SR), degradation mechanisms and models, defects, traps, variability in wire-like devices (selected materials)
- Long term: 10+ **: multi-scale implementations** (transfer to TCAD), **ac/transient regimes** (with q.m. effects)

❖ 2. Potential for application or Application needs and Impact for Europe

Accelerate development of ULP technologies, Reinforce modeling SME ecosystem, transfer of tools to industry

- Medium term: 5+ : **Further growth of M&S including SME ecosystem**
- Long term: 10+ : Consolidation of TCAD SMEs, **maintain high quality education for nanoelectronics**, attract bright minds to Europe

Topic « *Modeling and Simulation» (2/2)*

- 3. Technology and design challenges

Model verification (including, but not limited to, experimental calibration) at different levels of physical detail

- 4. Definition of FoMs (quantitive or qualitative) or planned evolution

Physical device dimensions and computational dimensionality of manageable problems (e.g.: length, cross section, volume, no. of materials, regions, atoms, eigenstates, particles, wall clock time, CPU time)

  - Medium term: 5+ : steadily improving - Long term: 10+ : steadily improving

- 5. Other issues and challenges, and interaction with other Tasks/WPs

Modeling for memory technologies, Modeling for steep slope devices, Modeling for power devices (automotive, energy), Modeling for large scale arrays of sensing elements integrated onto CMOS

  - Medium term: 5+ : «material» properties, new physics (SiC, GaN, Ferro/Piezo-electrics, … Electrolytes, analytes, etc.)
  - Long term: 10+ : Develop predictive and accurate TCAD solutions for industrial use

FIRST GLOBAL RECOMMENDATIONS:

- Promote dedicated M&S projects in application areas of interest for the European nanoelectronics (ULP electronics, power devices, nano-bio sensing, neuromorphic memory, quantum computing, etc…)
- Identify M&S needs well in advance, systematically devote adequate share of resources, also by embedding modeling in all technology projects

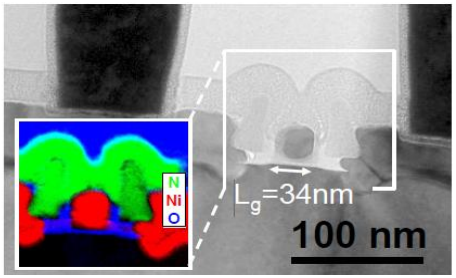
- Priviledge approaches that account for arbitrary geometry and all relevant physics, e.g. multi-scale, valley, subband, electrostatics of layered structures with wavefunction penetration, transport models comprehensive of tunneling and all relevant scattering mechanisms (remote-X, SR)

Characterization

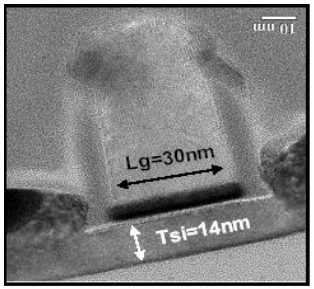
New challenges in electrical characterization

CMOS technologies evolve from bulk to FDSOI/FinFET and NWs:

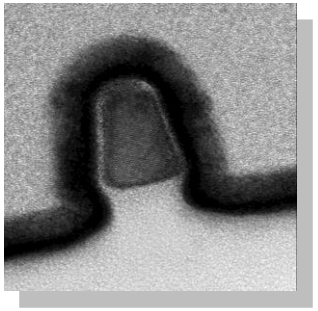
- **Improved electrostatic control,**
- **Better scalability and lower variability ?…**
- **But increasing issues of transport and interfaces in UTB and new materials….**



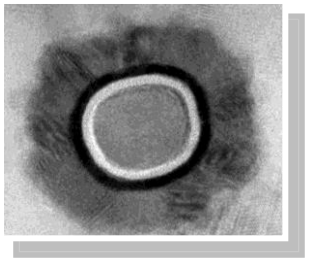
Bulk 28



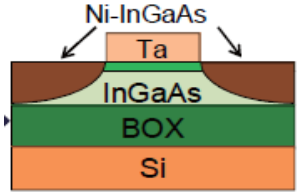
FDSOI



FinFET
Tri-Gate

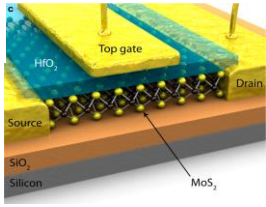


GAA NW



III-V

2D mat



New challenges in electrical characterization

Main issues:

- **CV measurements still feasible using specific test structures (multi fingers or RFCV) on FDSOI, FinFET, NWs…**
- **MOSFET parameter extraction still applicable with new methods and on new 2D materials, III-V, Ge,… Rsd is a key parameter…**
- **Mobility and transport parameters still measurable on standard MOSFETs down to very small Lg but MR very useful tool…**
- **Traps and interface quality can be assessed even on very small area devices using LFN/RTN (C-V, CP area limited unless multi finger use)**
- **Stochastic Variability becomes critical and must be measured in static and in dynamic => problems for non mature technologies but also for TFET, FeFET….**