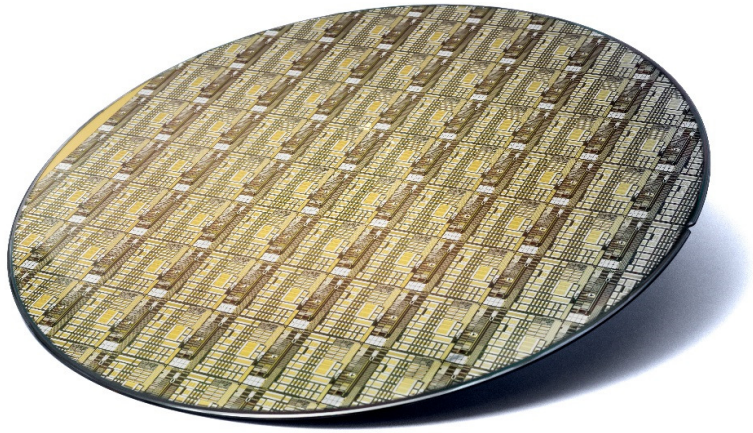
# OUTLOOK FOR 200mm E-MODE DEVICE TECHNOLOGY

S. STOFFELS

# OUTLINE

- High level roadmap for 200mm GaN POWER platform
- 200mm GaN-on-Si: Performance & Reliability Optimization
  - Schottky Diodes
  - p-GaN HEMTS
- Exploration of Novel Concepts
  - Substrates
  - Co-Integration
  - Next generation devices



imec

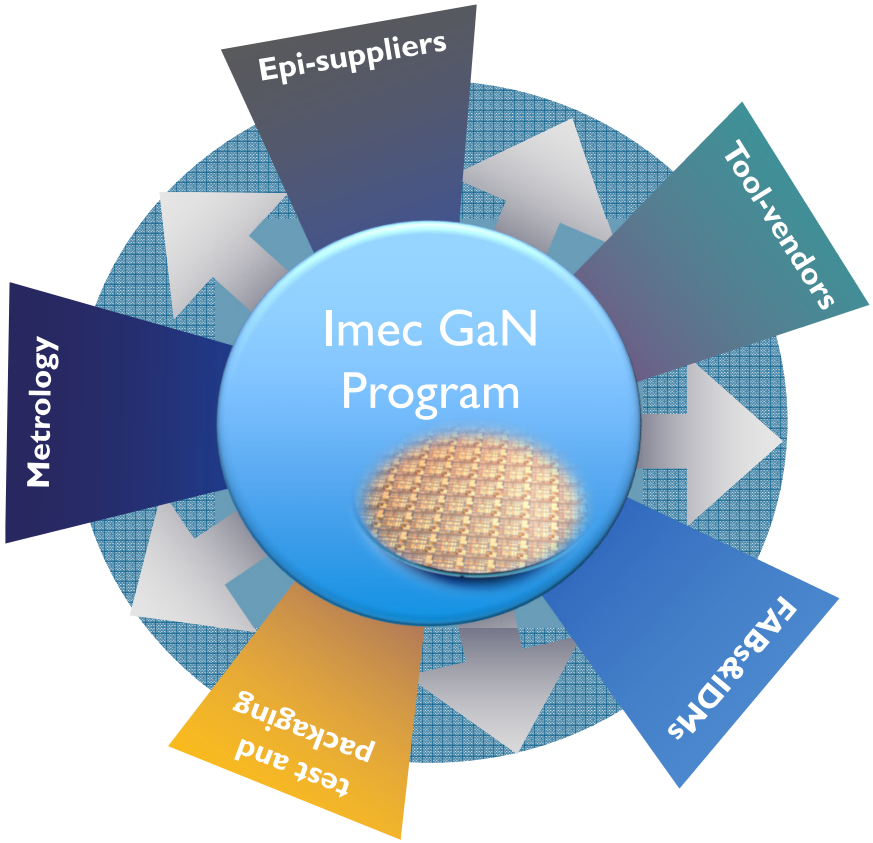
# GaN AT IMEC

## 10+ YEAR OF GAN EXPERIENCE

- **Two dedicated teams:**
  - GaN epi engineering
  - GaN device engineers
- **Proven state of the art epi- capabilities** up to 8-inch GaN-on-Si
  - Imec has access to 3 different reactors from 2 vendors:
    - Veeco K465i
    - Veeco Propel
    - Aixtron G5+ C

  *Imec proprietary recipes have been successfully installed in all these reactors*.
- **8-inch CMOS compatible GaN power device platform**:
  - State of the art of GaN-on-Si epitaxy, e-mode ($V_{TH}$>2V) and diode technology
  - Exploring and de-risking new technologies
  - Tech transfer and/or tailored e-mode transistor (or Schottky diodes) development
- **Fully equipped** for:
  - 100, 150 and 200mm GaN epitaxy and 200mm pilot line processing
  - Metrology systems
  - High-Voltage-Current characterization
  - Reliability setups

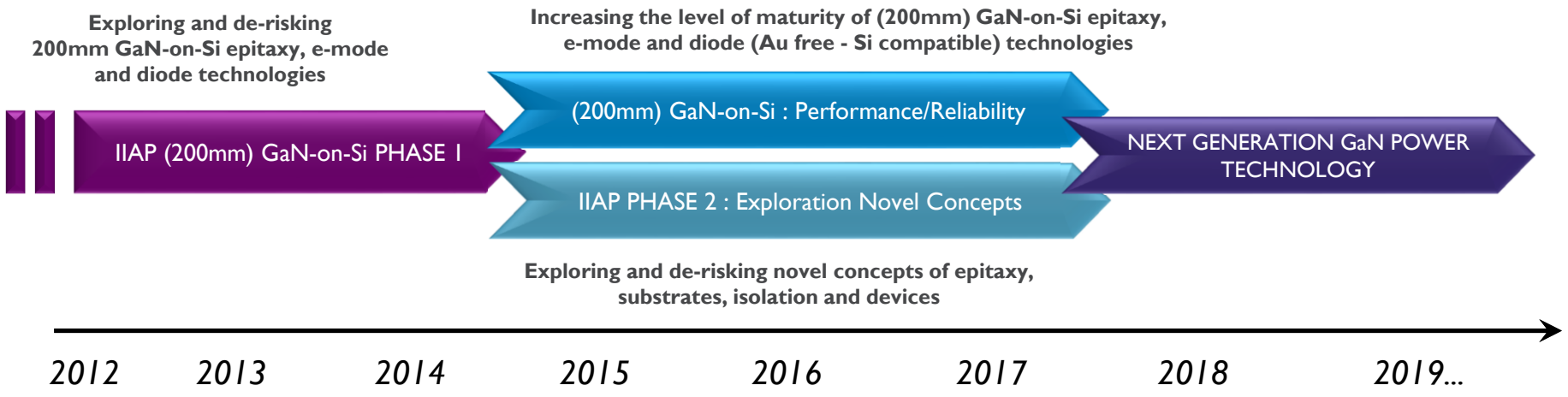
# ECOSYSTEM IN THE GAN PROGRAM




imec

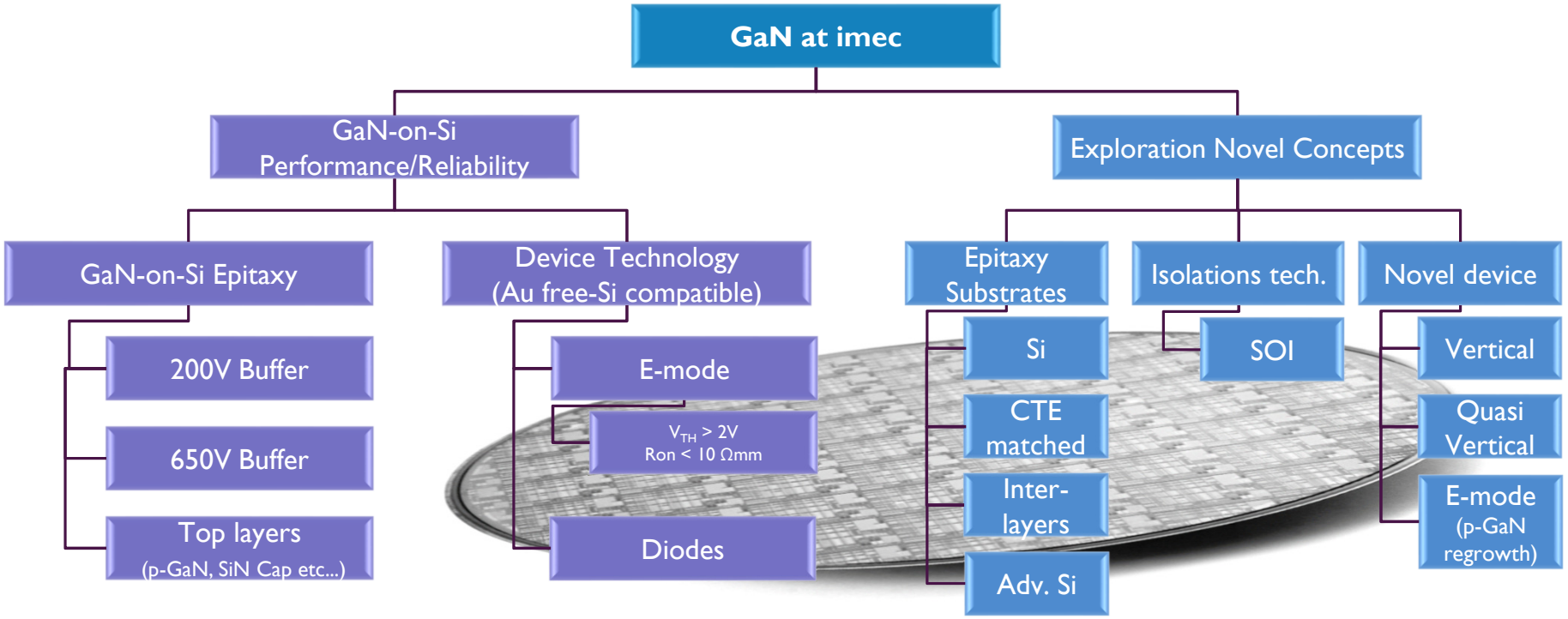
# HIGH LEVEL PLAN OF GAN TECHNOLOGY AT IMEC

## TARGETING SHORT AND LONG TERMS NEEDS OF GAN

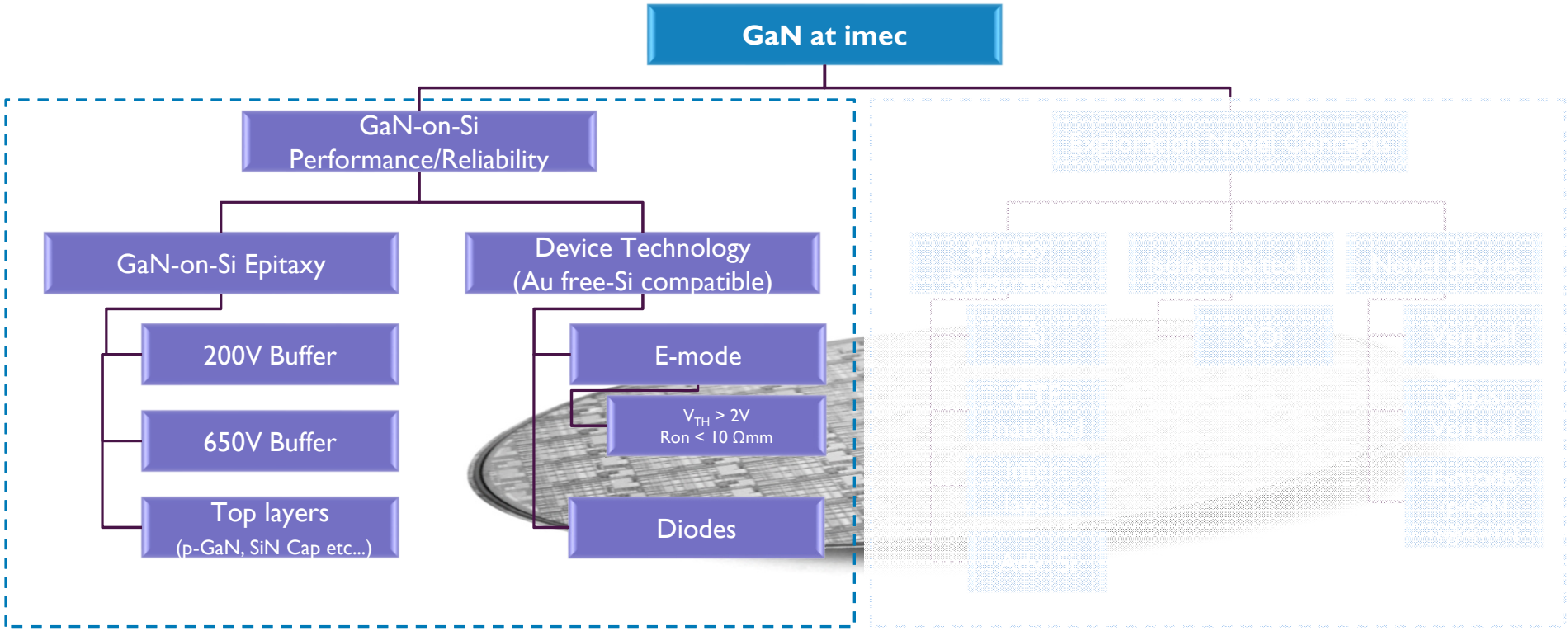



imec

# ADDRESSING SHORT TERMS AND LONG TERMS TOPICS



# ADDRESSING SHORT TERMS AND LONG TERMS TOPICS

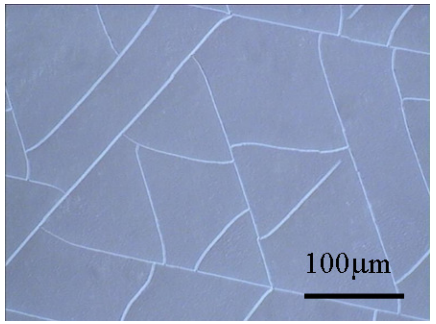


# EPITAXY

# WHY IS GROWING GaN ON Si SUBSTRATE SO DIFFICULT?

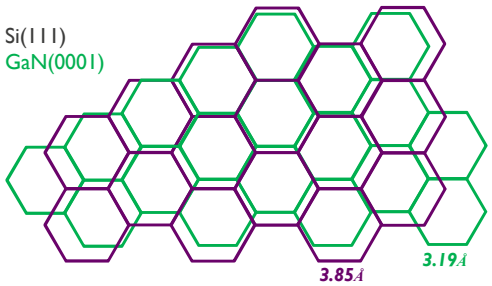
## BECAUSE OF THE **LARGE LATTICE AND THERMAL MISMATCH**

- The Si lattice is 17% larger than the GaN lattice
- CTE mismatch between GaN and Si is 116%

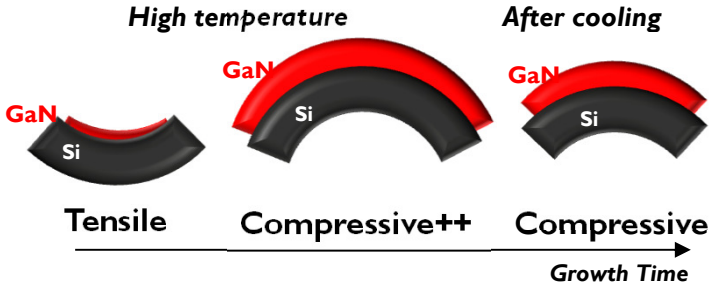



*Large thermal mismatch can result in GaN layer cracking*

***Lattice mismatch***




***Effect of Thermal mismatch***

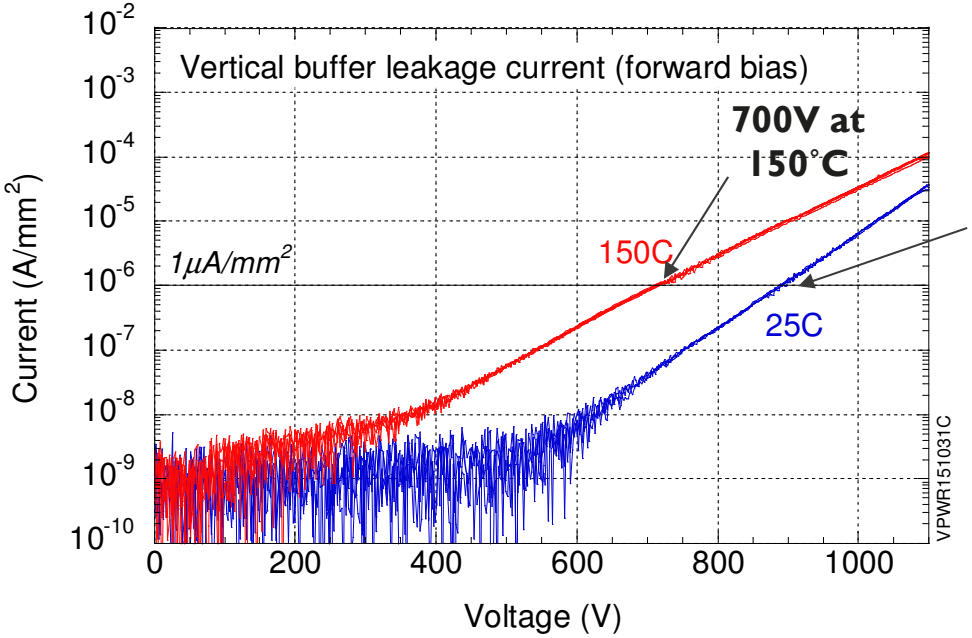



*Y. Saripalli, IEEE-ICEE 2014*

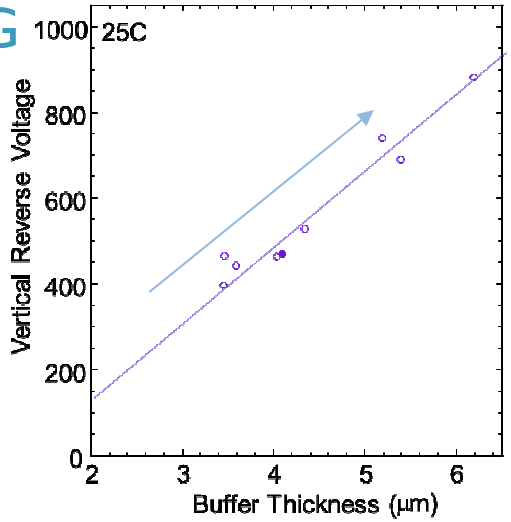
imec

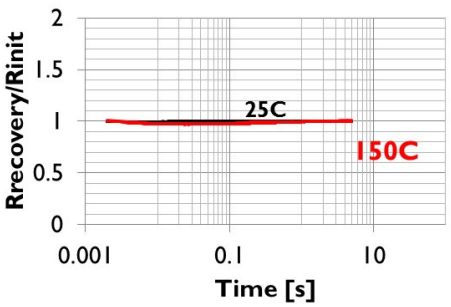
# 200mm GAN-ON-SI EPITAXY AND BENCHMARKING

## 200mm GAN-ON-SI EPITAXY FOR **600V** APPLICATIONS

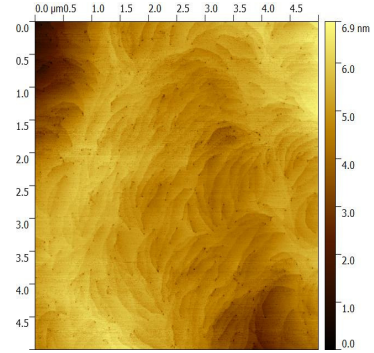



***Breakdown is combined with pit free surface, bow below 50μm and low dispersion/trapping effects at 150°C***




***Low dispersion***

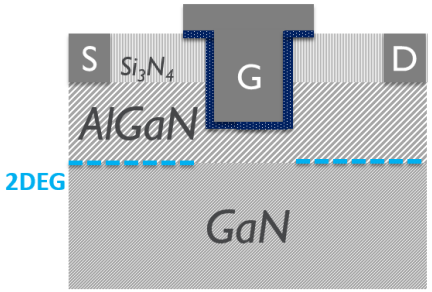


***Good surface quality***

# DEVICE TECHNOLOGY

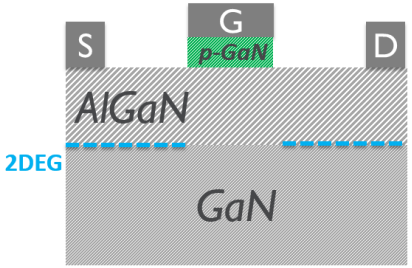
# GaN DEVICE TECHNOLOGY

**MISHEMT**




*The AlGaN layer is recessed below the gate, to locally interrupt the 2DEG to realize e-mode operation.*

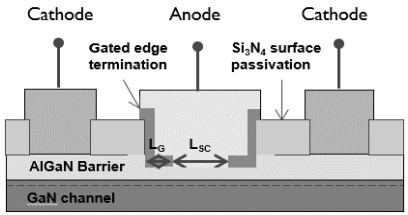
**p-GaN**




*A p-GaN layer below the gate lift-up the band diagram below the gate to realize e-mode operation.*

**Schottky Diode**

**GET-SBD**




*Schottky Diode with edge termination to achieve low leakage under reverse*

**imec has a 200mm platform for processing various GaN power technologies**

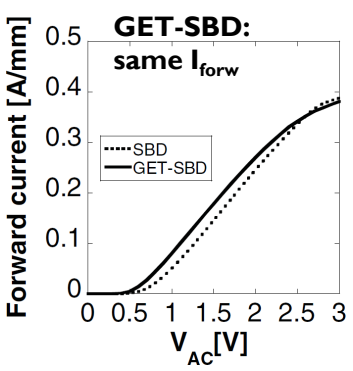
imec

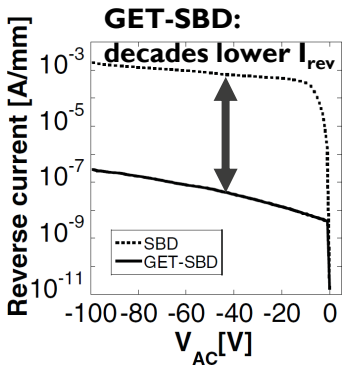
# SCHOTTKY DIODES

# DIODE ARCHITECTURE

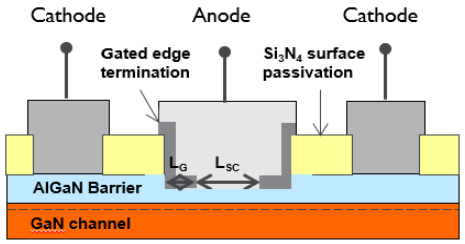
## GATED EDGE TERMINATION (GET) SCHOTTKY BARRIER DIODE (SBD)

- GET-SBD is the architecture of choice *
  - Recessed Schottky Contact in center (with length $L_{SC}$) allows forward current flow
  - Recessed Gated areas at the side (with length $L_G$) block reverse leakage current

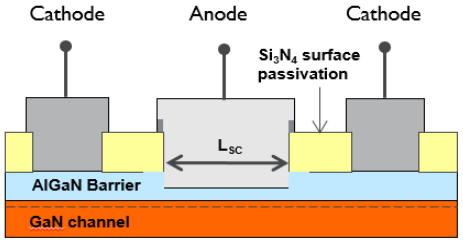



**GET-SBD**




**Conventional SBD**

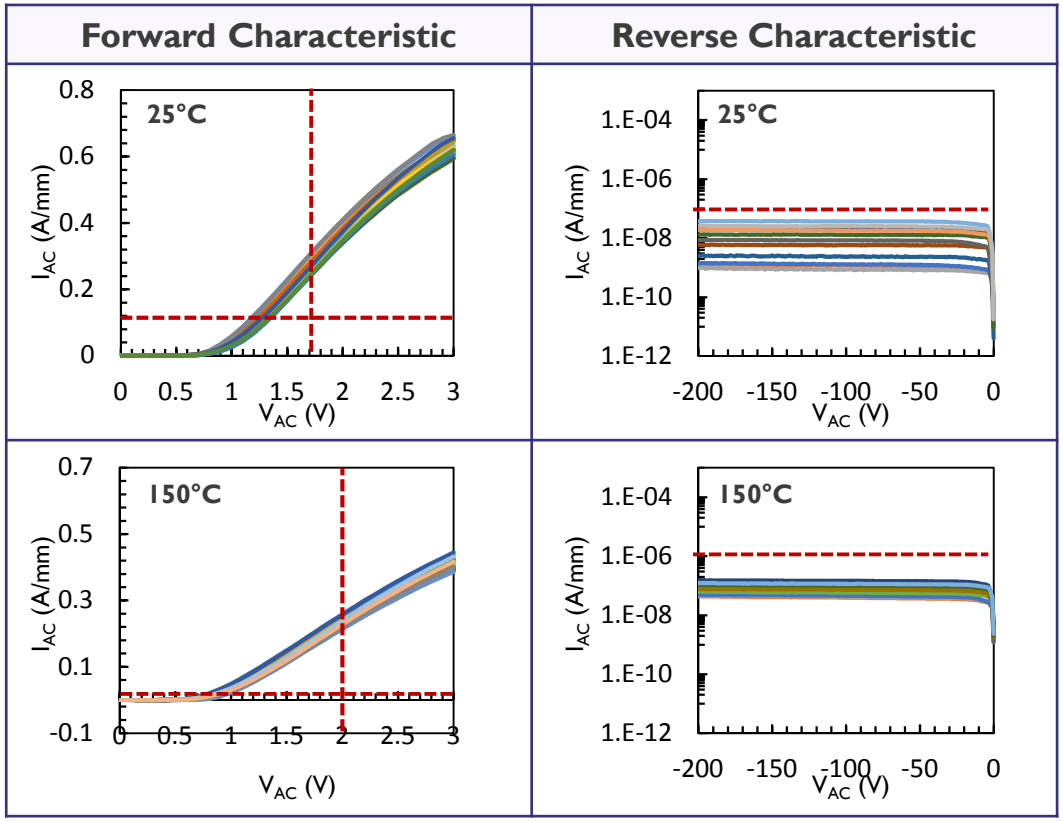



* US 2014/0103357 A1, EP 2722890 A1 and JP 2014 090 059 (published)

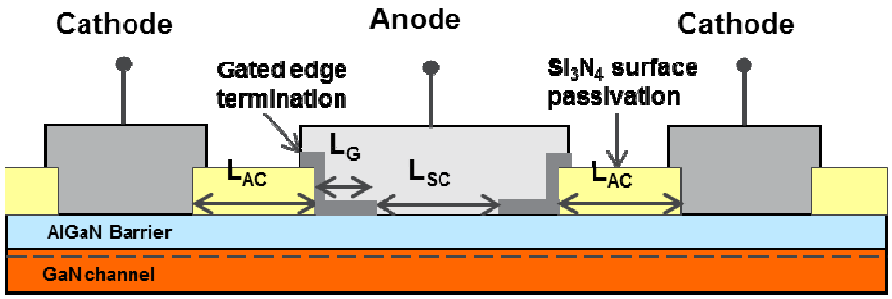
# DIODE PERFORMANCE CRITERIA: DC OPERATION

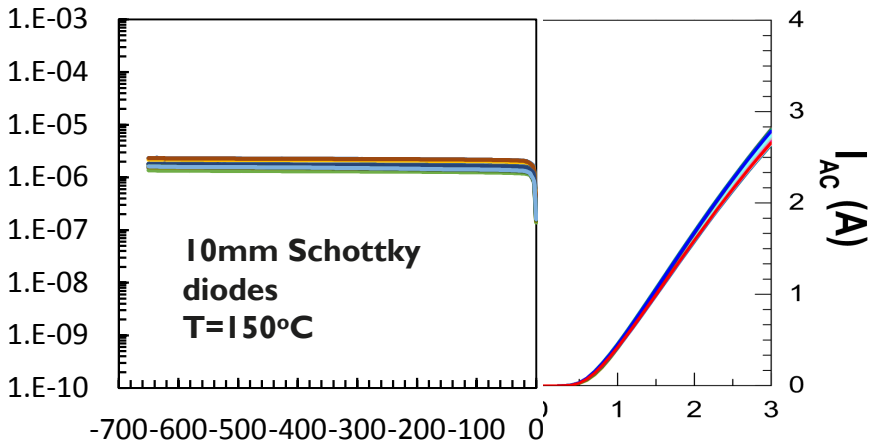
## TARGET VALUES ARE SET ON $I_{FORW}$ AND $I_{REV}$ OF 30 mm POWER DIODES

- Forward Voltage $V_F$
  - $V_F = V_{AC}$ at $I_{AC}$ = 0.1 A/mm
  - Characterizes forward current capability
  - 200V target at 25°C: 1.7 V
  - 200V target at 150°C: 2.0 V
- Reverse Current $I_{rev}$
  - $I_{rev} = I_{AC}$ at $V_{AC}$ = - 200 V
  - Characterizes current blocking capability
  - 200V target at 25°C: 1e-7 A/mm
  - 200V target at 150°C: 1e-6 A/mm



# DIODE PERFORMANCE:
## 650V LARGE AREA POWER DIODES

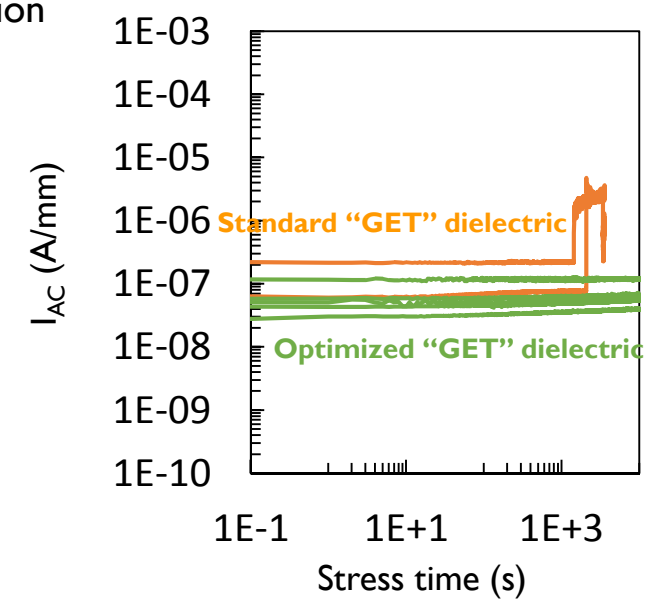



- High breakdown achieved for large Area Schottky Diodes
  - >650V
- Tight distribution on both forward and reverse Characteristics.

# DIODE PERFORMANCE
## RELIABILITY

- Result standardized HTRB test (at 150°C and $V_{AC}$ = - 160 V)
  - Target $t_{BD}$ ≥ 10 ks can be achieved by optimizing the gate dielectric in the gate edge termination region

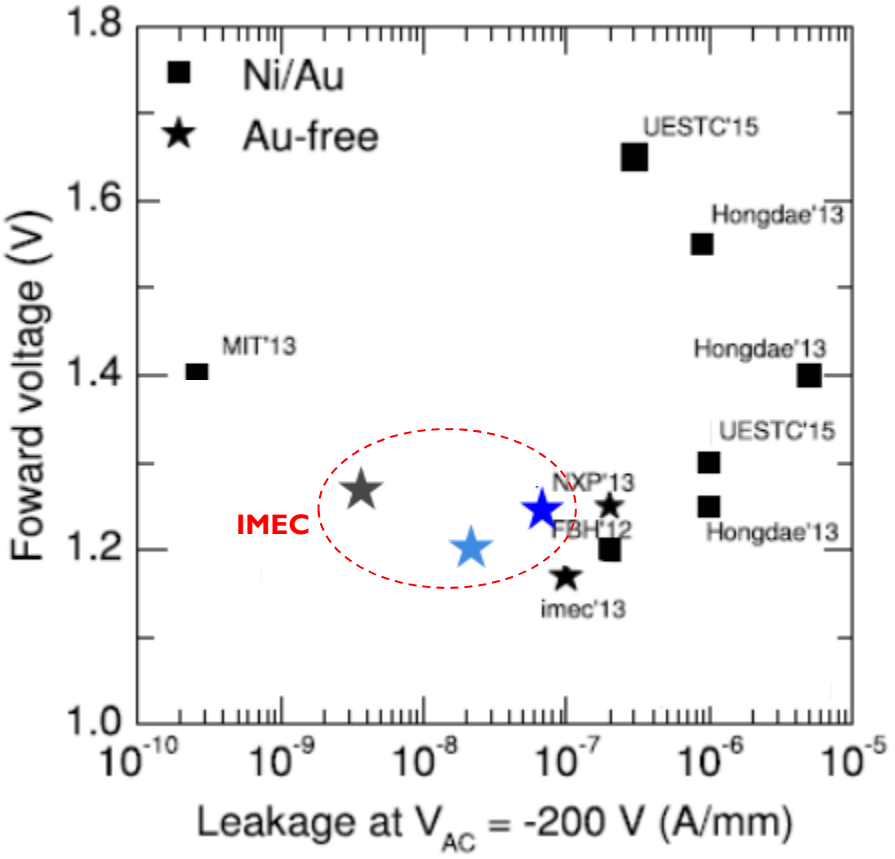



- High temperature reverse bias stress showed improvement of the device stability for optimized GET dielectric.
  - 10mm devices
  - LAC = 5µm
  - VAC = -160V
  - 150°C

# Benchmarking Schottky Diodes

- Benchmarking done at 25°C
  - Many reports only mention 25°C
  - imec devices: median values on 30 mm power diodes

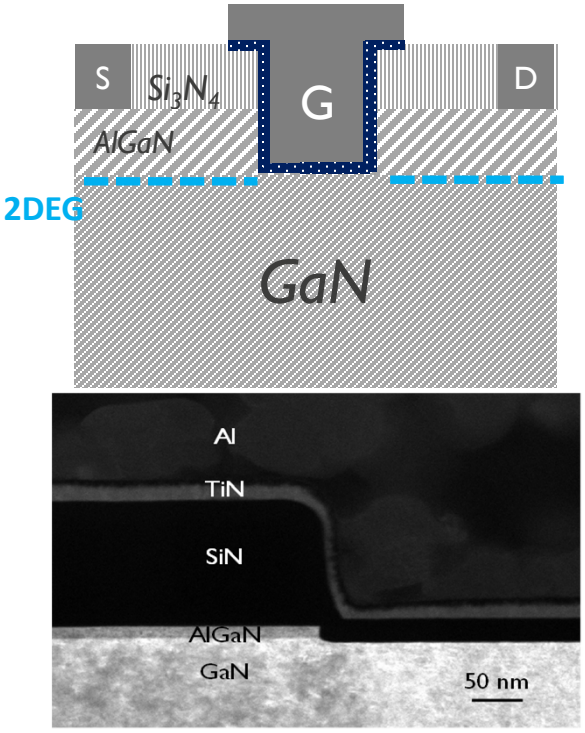
**RT data, anode connection imec (2016)**



# E-MODE DEVICE TECHNOLOGY

# RECESSED MIS-HEMT

## EXCELLENT SURFACE, ROBUST TDDB AND CHALLENGING GATE TECHNOLOGY




**Advantages:**

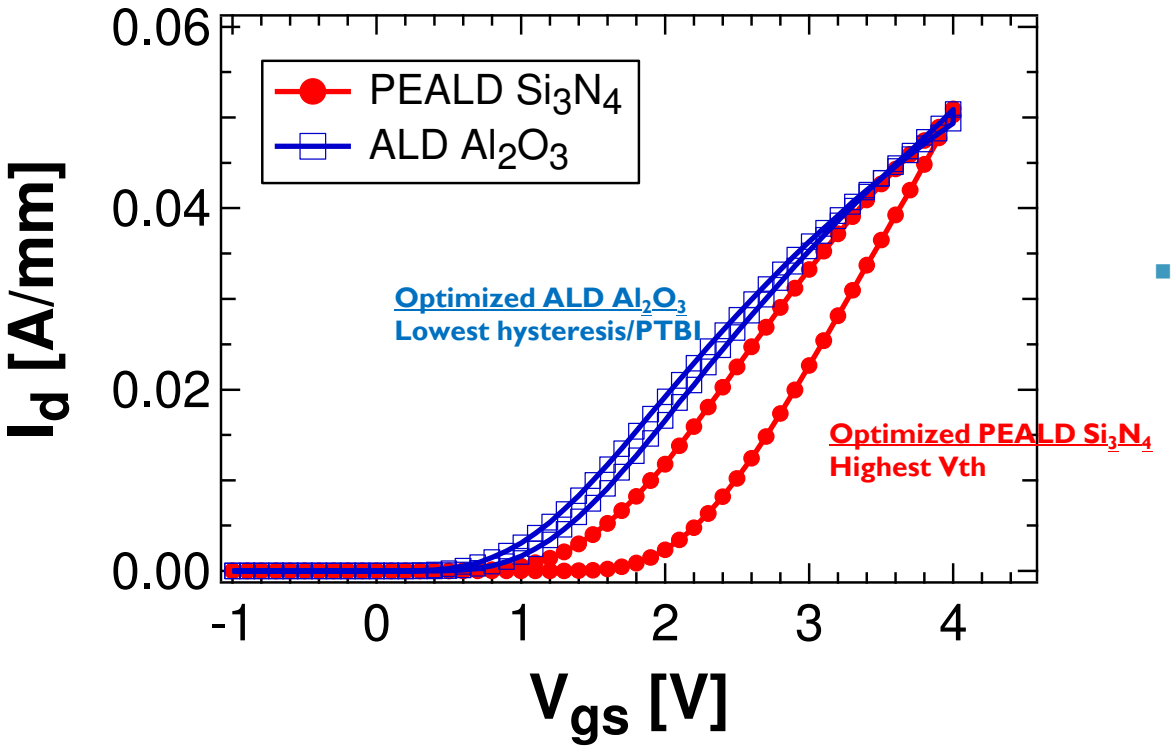
1. AlGaN surface untouched → low surface trapping
2. Robust gate dielectric for TDDB

**Challenges:**

1. Gate dielectric for low hysteresis /PBTI
2. Limited knobs to turn $V_{TH}$:
   - ✓ Recess technology
   - ✓ Dielectric charges and cleaning
   - × Ni/Au metal stack is not allowed in CMOS
   - × Fluorine implantation: unstable

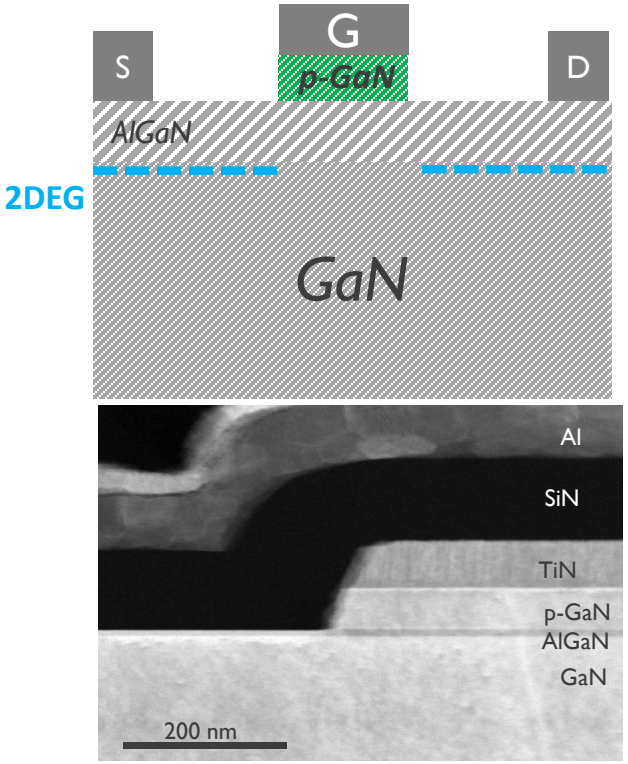

imec

# E-MODE OPERATION OBTAINED WITH RECESSED MISHEMT




- Obtaining simultaneously high $V_t$ and low dispersion/PBTI is challenging

# P-GaN HEMT

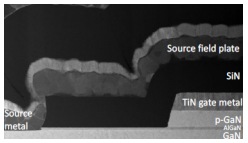


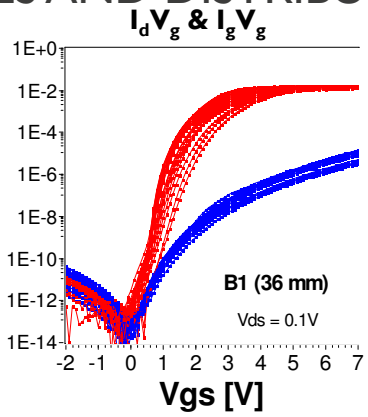

- Many knobs to turn, excellent $V_{th}$, important to control the surface
- **Advantages:**
  - 1. Threshold voltage can be tuned by:
    - p-GaN layer (Mg profile, epi-deposition, etc…)
    - AlGaN barrier design
  - 2. Absence of hysteresis (PBTI)
  - 3. Low dispersion if properly designed
- Disadvantages
  - Larger forward current

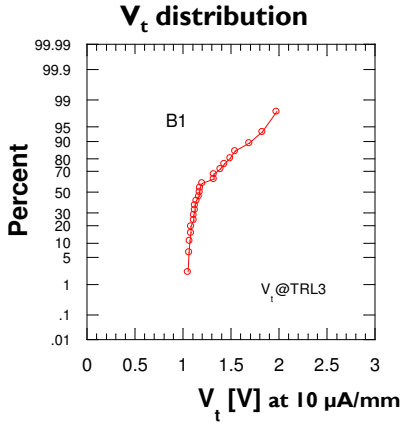

imec

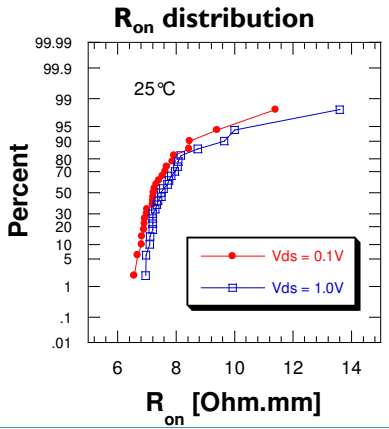
# 36 mm POWER TRANSISTOR DATA SHEET

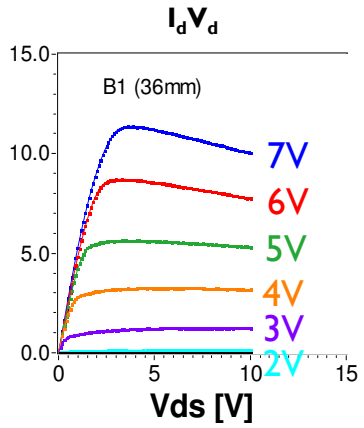
## CURVES AND DISTRIBUTION

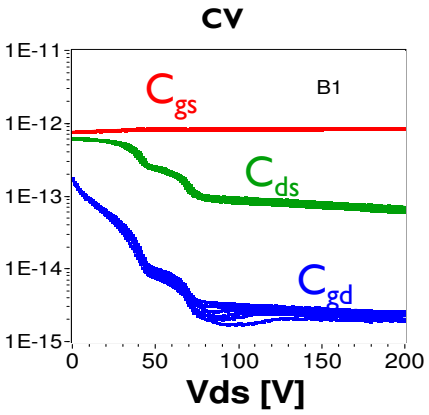


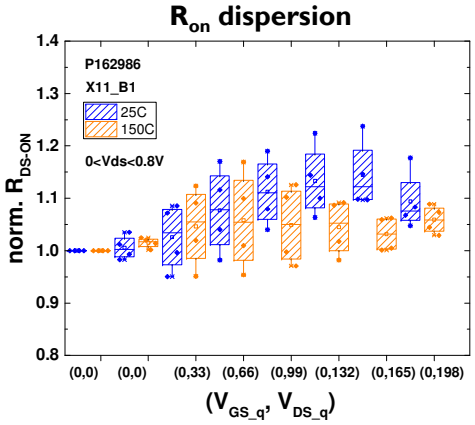



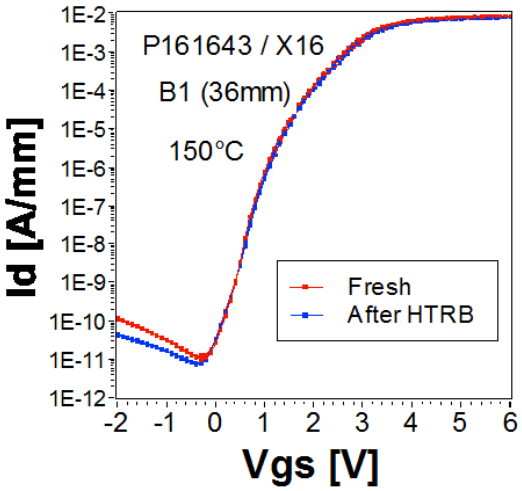




imec

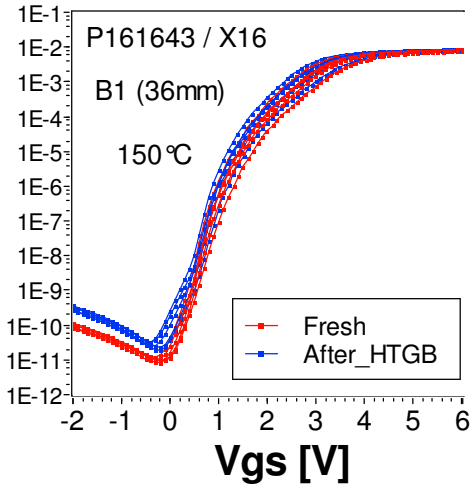
# P-GAN DEVICE RELIABILITY

## HTRB




- High temperature reverse bias ($V_{gs}$= 0V, $V_{ds}$=160V, 10 ksec at 150 °C)
  - 3 wafers from 3 different device lots

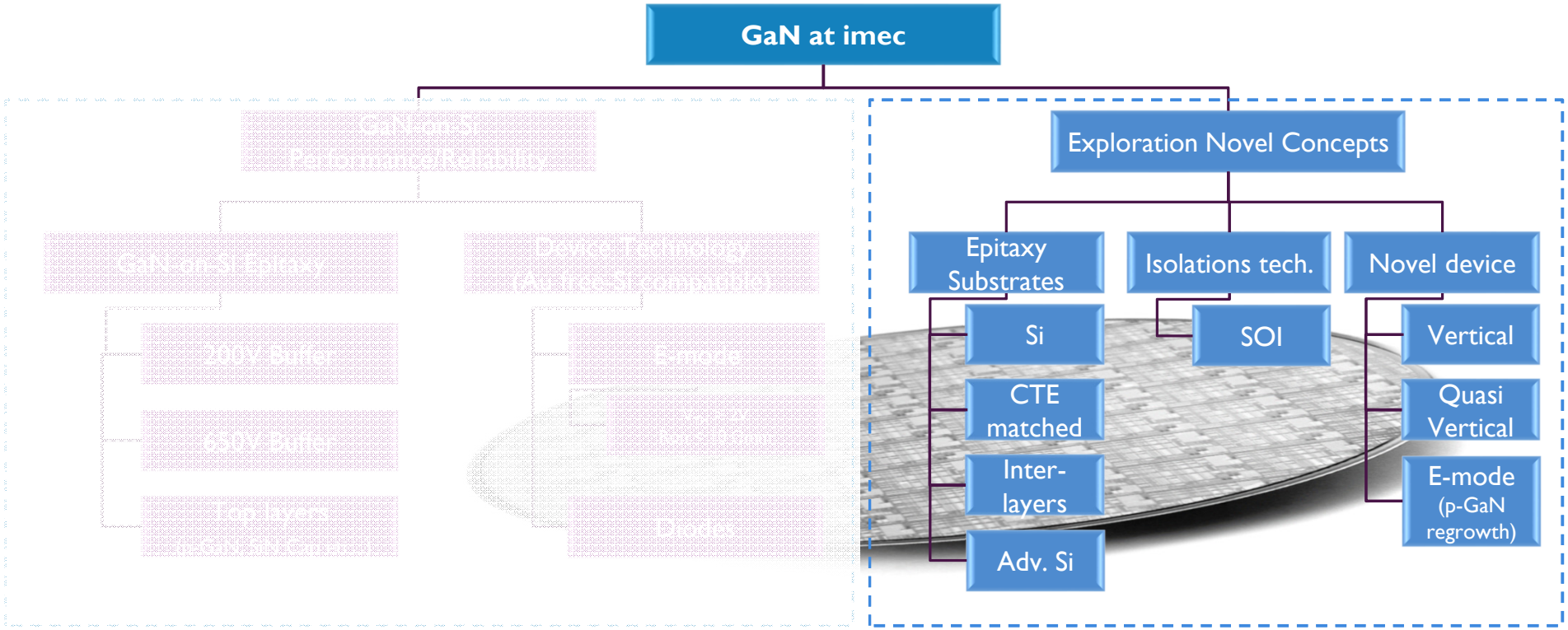
## HTGB




- High temperature gate bias ($V_{GS}$=7V, $V_d$=0V, 10 ksec at 150 °C)
  - Slight shift in $V_t$

imec

# ADDRESSING SHORT TERMS AND LONG TERMS TOPICS



# NEXT GENERATION SUBSTRATES

## 200mm GaN-on-Si is great!

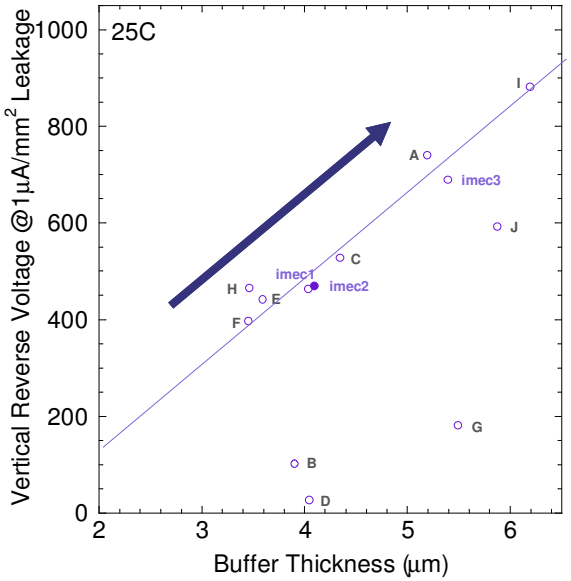
**200mm Si(111) substrates are:**

√ Commercially available

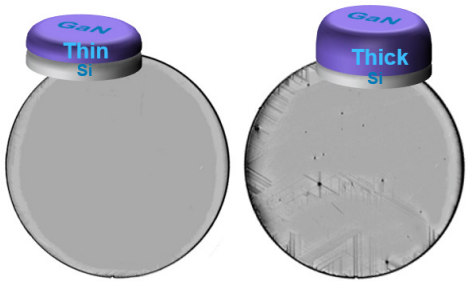
√ Not expensive

√ Can be processed in a Au-free Si CMOS fab

√ Buffer breakdown voltage scales linear with GaN buffer thickness




- ....**<u>but can we do better</u>**?

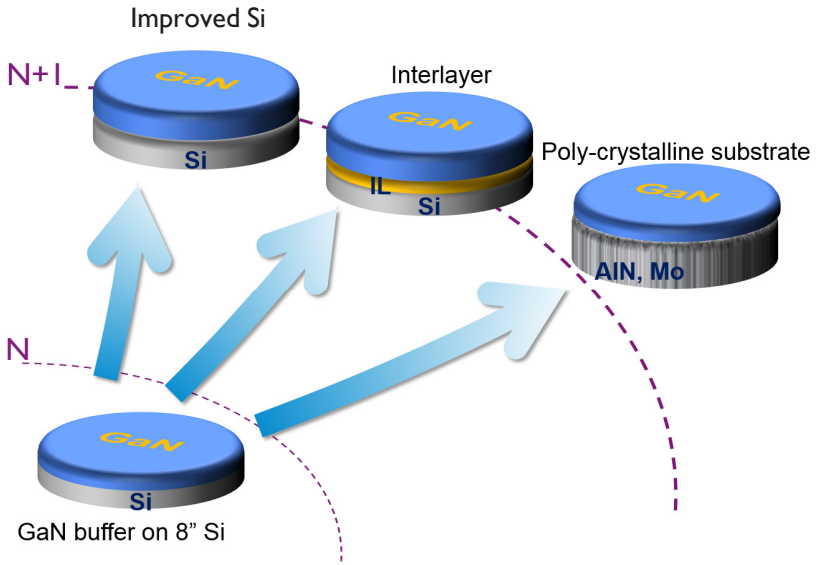



***Large thermal mismatch can result in damage to Si substrate as measured by X-Ray Topography***

imec

# NEXT GENERATION SUBSTRATES

- Are **alternatives possible**?
- Exploration and development of **<u>Novel Concepts for Substrates</u>** for 200mm GaN power Devices that provide better (Al)GaN crystal quality, lower wafer bow, or reduced buffer leakage at high voltage and methods for co-integration of power devices.
  - Improved Si substrates
  - Si with interlayers
  - CTE matched substrates

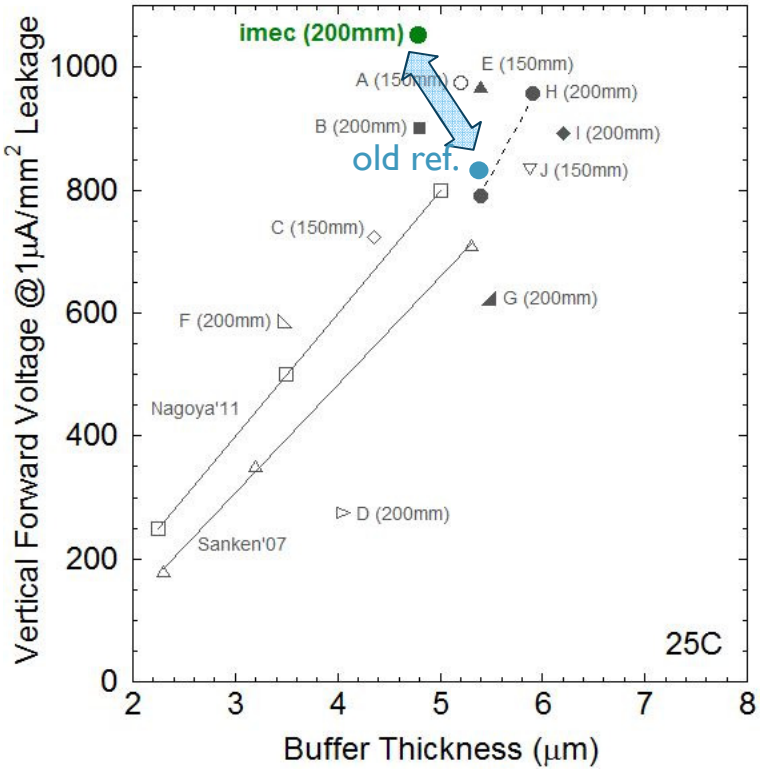


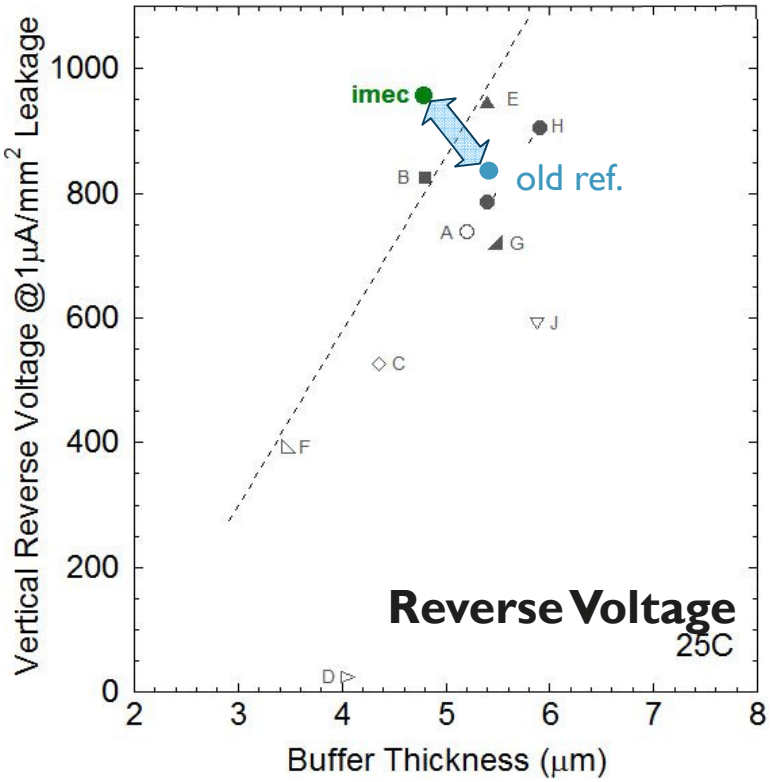

PowerBase

# IMPROVED GaN-on-Si

## Vbd BENCHMARKING AT 25˚C





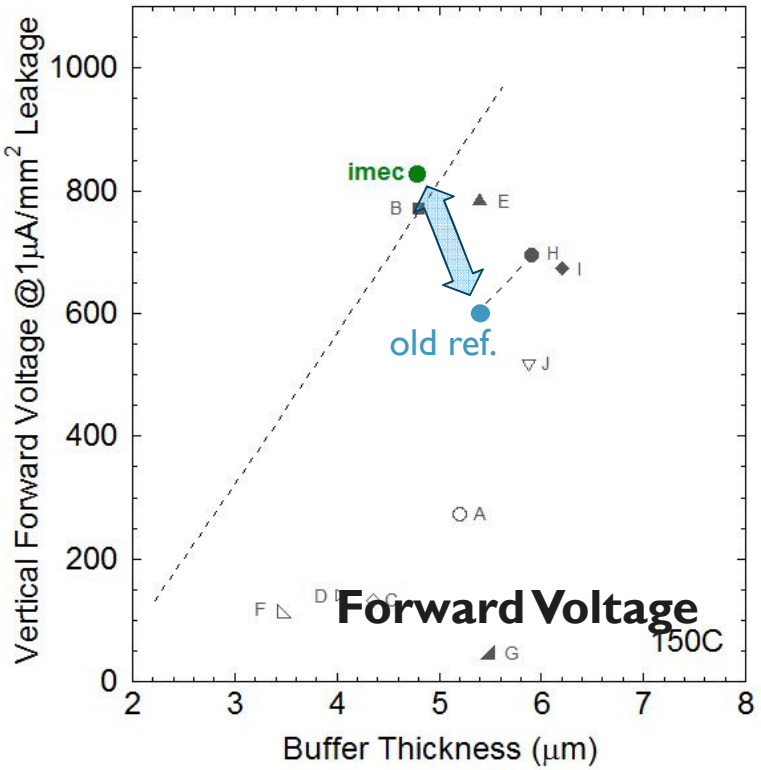



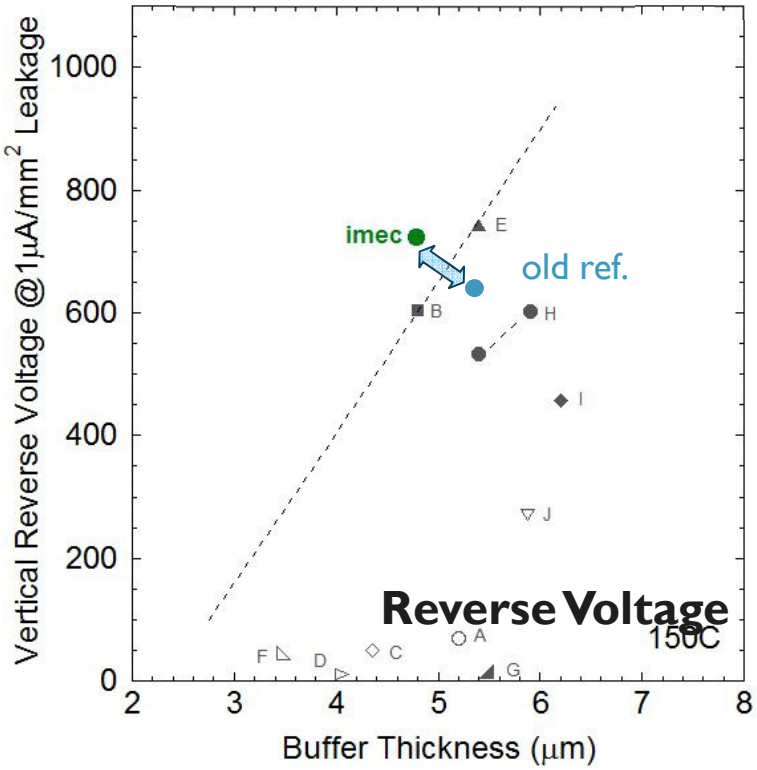

- Similar $V_{bd}$ performance with ~1.3um thickness reduction
- A clear indication of a higher breakdown field strength

# IMPROVED GaN-on-Si

## Vbd BENCHMARKING AT 150°C





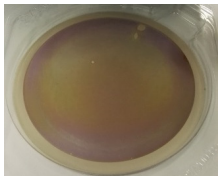

- Similar $V_{bd}$ performance with ~1.3um thickness reduction
- A clear indication of a higher breakdown field strength

imec

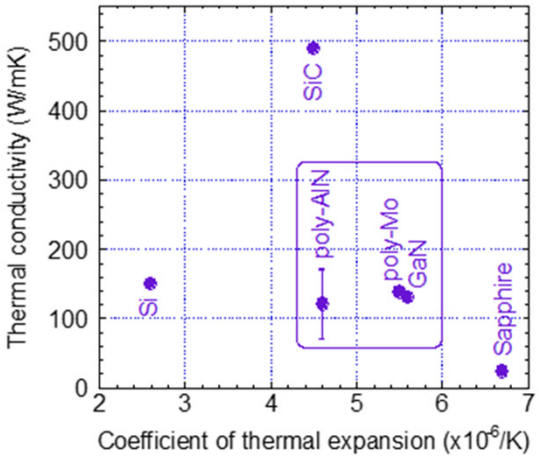
# LOOKING BEYOND SI
## CTE MATCHED SUBSTRATES

**Poly-AlN is in spec for wafer bow and leakage for a much thinner substrate compared to GaN-on-Si**

**Poly-AlN**

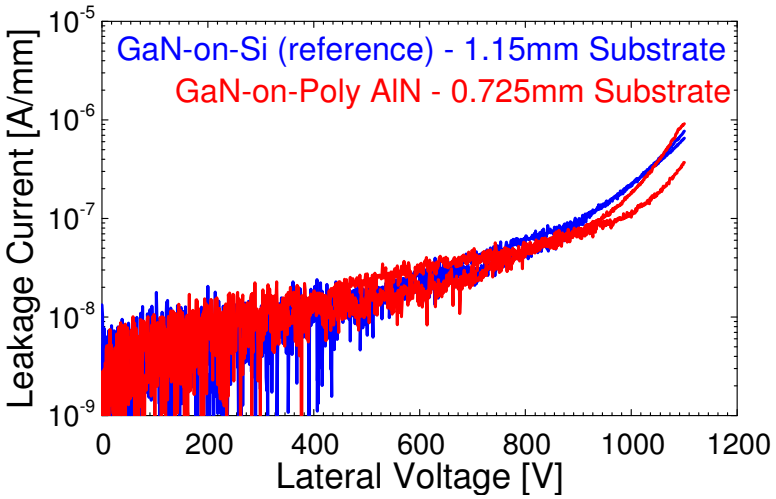



200mm GaN-on-Poly AlN: low wafer bow and low leakage for a substrate of 0.725mm versus 1.15 for GaN-on-Si




- poly-AlN: much better thermally matched compared to Si and **similar to SiC**

**Lateral breakdown**




imec

# SEMI-VERTICAL DEVICES

# NOVEL DEVICES 200mm

## SEMI-VERTICAL DEVICES

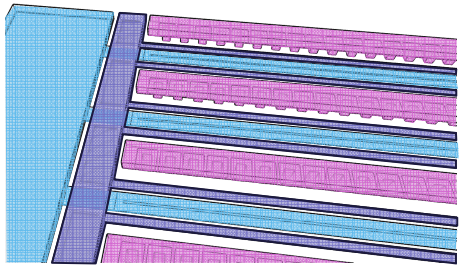
### Vertical Devices

- High voltage over drift region
  - No impact on foot print
  - No surface electric fields
  - No high voltage over the back-end
  - Potential to achieve avalanche rating
- Conceptually different from HEMT :
  - No 2DEG → no high electron mobility
  - On-state through inversion layer formation
  - Requires N+, N- and P+ doped epi layers

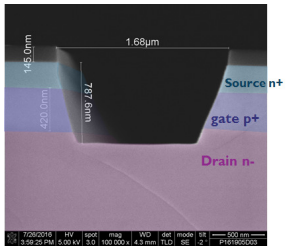
### Semi-vertical devices

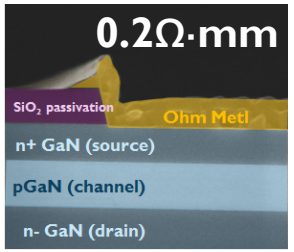
- **200mm Bulk GaN** is **not available** or prohibitively expensive
- **200mm Semi-Vertical Device Technology** at imec
  - Preparation of modules and device understanding
  - Might not have commercial finality, rather path towards full vertical devices
  - Fully Planar technology
  - Explore the limits of current epitaxial technology for vertical device stacks
  - "n+ I" substrates for semi-vertical devices

Device Design



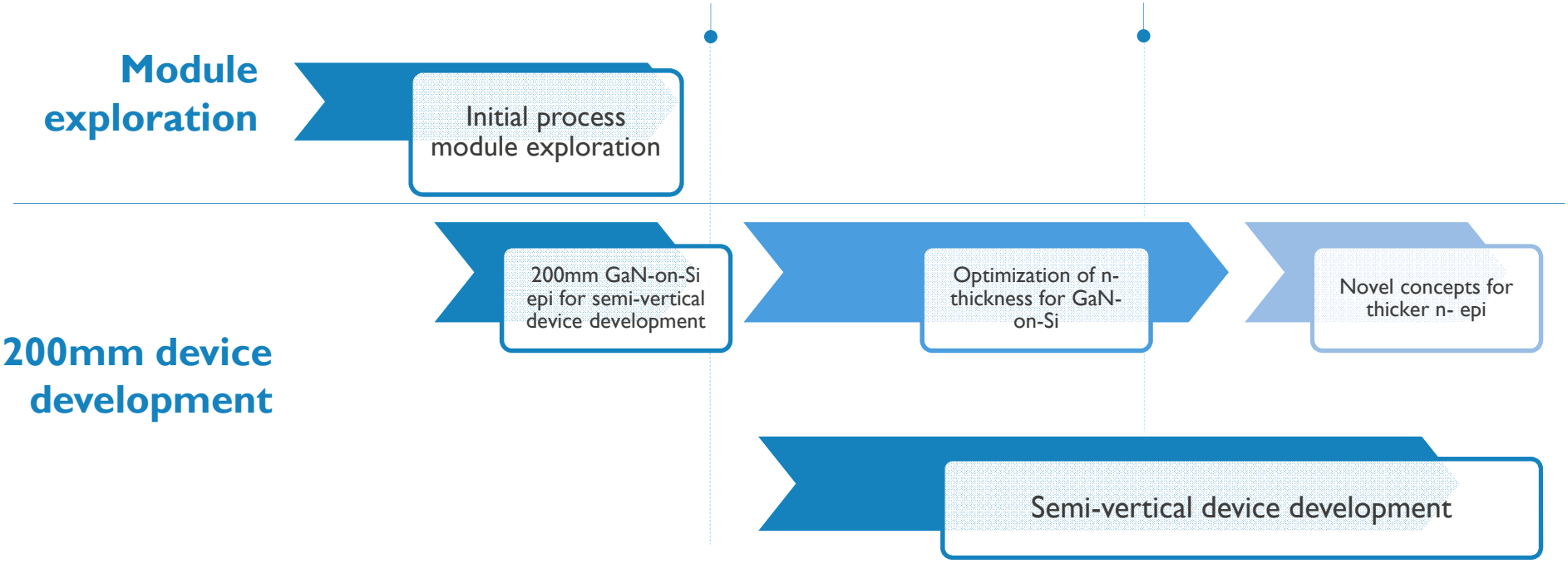
Epitaxy & Process integration



# PROCESS DEVELOPMENT TIMELINE

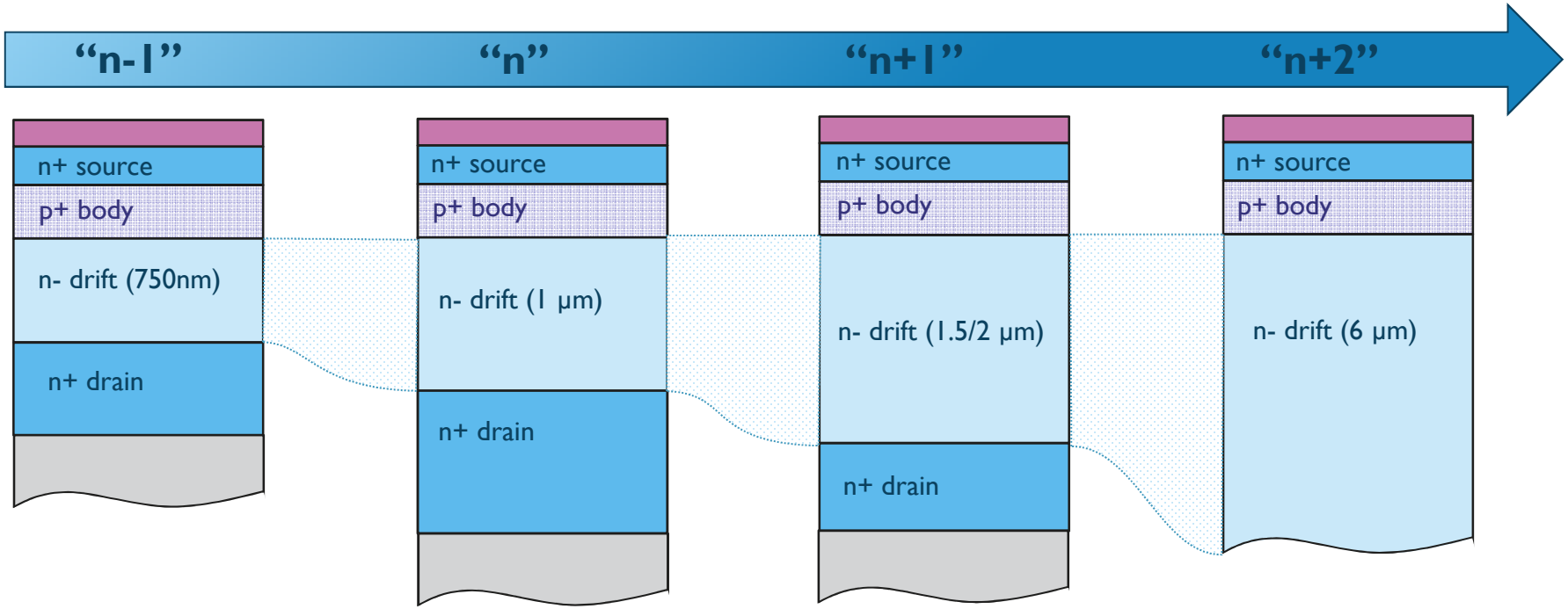
## PATH TOWARDS 200mm SEMI-VERTICAL DEVICES




imec

# NOVEL DEVICES

## EPITAXY FOR SEMI-VERTICAL DEVICES




- Continuously pushing the boundary of epitaxial growth of semi-vertical device stacks
  - Current drift layer thickness 1µm with 1.5-2µm achievable thickness

imec

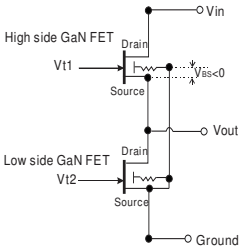
# CO-INTEGRATION

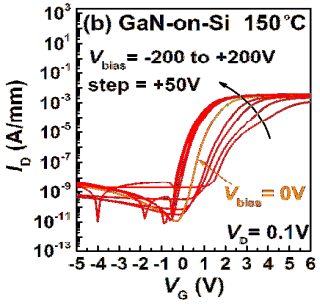
# NOVEL CONCEPTS

## HIGHER LEVEL OF INTEGRATION: COST REDUCTION ON THE SYSTEM LEVEL

### Higher level of integration

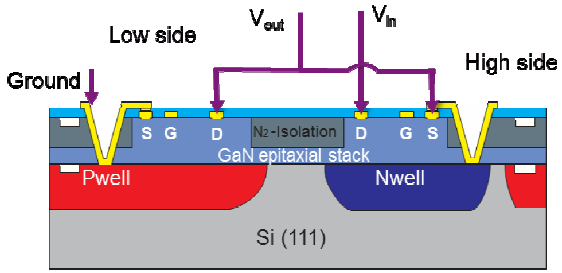
- Integration of high side and low side switches
  - Further cost reduction of the GaN technology
  - Reduction of interconnect parasitics (enable higher switching speed)
- Substrate reference is an issue



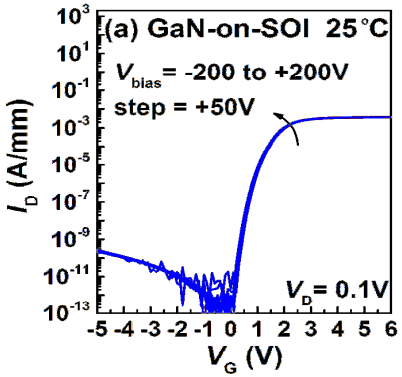

### Junction isolation

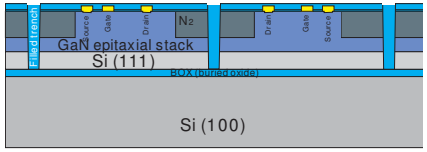
- Isolate devices from each other by fabricating p-well/n-well in the substrate.
  - Reference GaN transistor source to p-well or n-well
  - Parasitic pn-diode interfering with switching behavior




### Trench isolation

- Isolate devices from each other by fabricating trenches in the substrate
  - Good isolation can be achieved




imec PowerBase

# CONCLUSIONS

# CONCLUSIONS

- 200mm GaN epitaxy and e-mode device technology established
  - Solved the issue of growing thick epi-layers on 200mm, qualified for 650V.
  - State of the art performance for 200V and 650V devices
  - Increasing reliability yield and performance of components (increase TRL level)
- Looking ahead to the future
  - Technology exploration for next generation substrates and epitaxy
    - Increase breakdown strength of GaN-on-Si
      - Thinner buffer with equivalent breakdown, decreasing cost and increasing yield
    - Novel substrates to enable next-gen applications
  - Next generation devices
    - (semi-)vertical devices
    - Higher levels of integration through isolation techniques


embracing a better life