GaN from an epitaxy perspective

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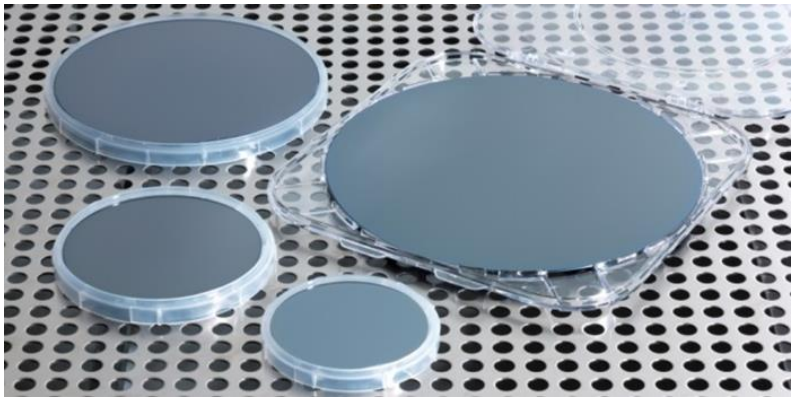
About EpiGaN

We supply industry-leading **GaN-on-Si and GaN-on-SiC epiwafers** to the semiconductor industry enabling the next generation of **power switching** and **RF power** devices and systems.



Product Highlights:

- **Power Switching:** leakage < 10 nA/mm@650V, breakdown > 1000 V, record R_{on}*A of 1.6 mΩcm^2
- **RF Power:** f_t = 100 GHz (l_g of 60nm), g_m > 600mS/mm, P_{CW} > 4.5W/mm@40GHz
- **Sensor** applications enabled by bulk resistivity > 10^{12} Ohm/sq

Topics - NEREID workshop

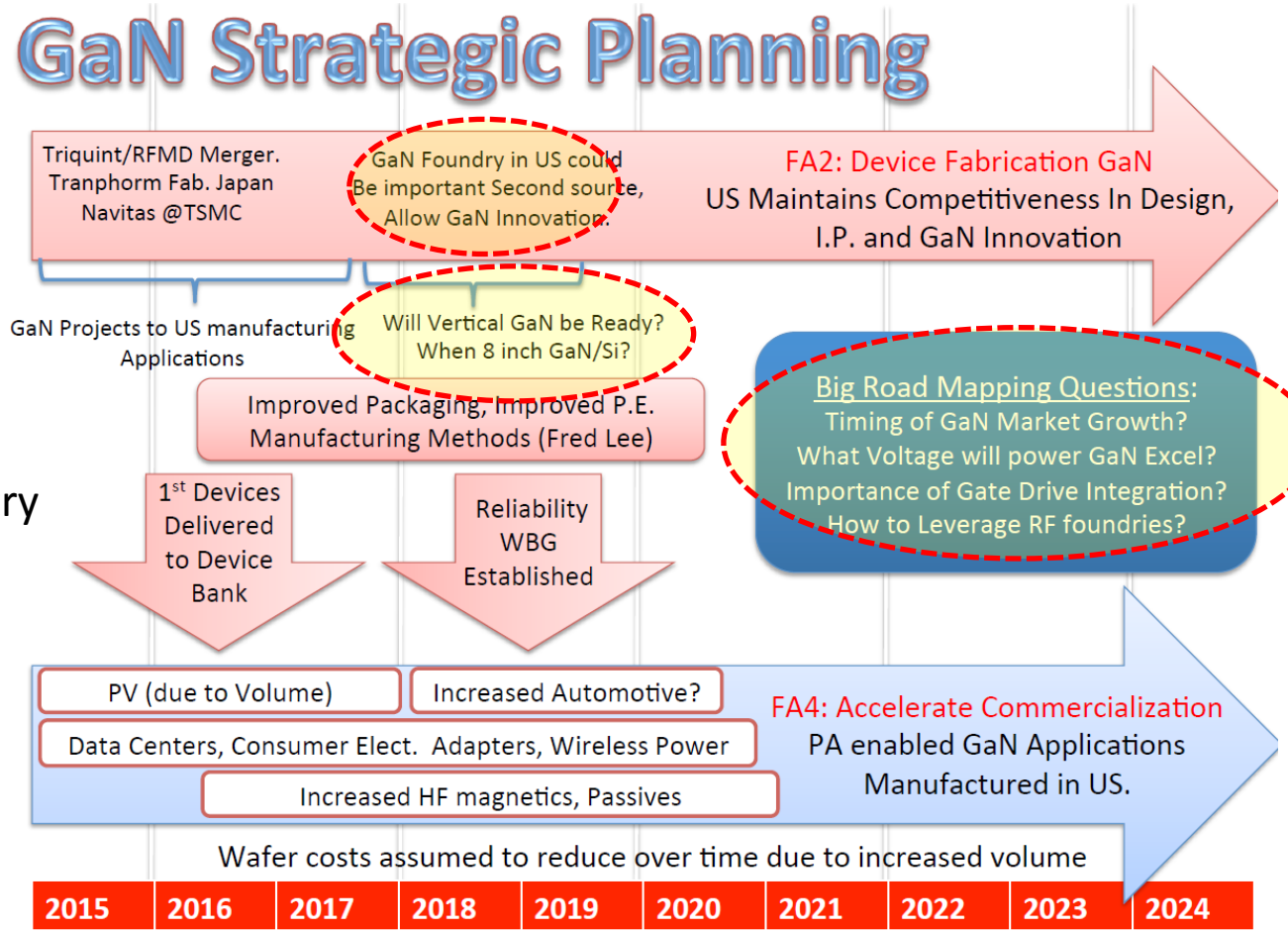
Thoughts on **GaN material** from different angles:

- Application requirements
  - RF, power, (chemical sensing, MEMS, opto)
- Substrate specific challenges
  - (Al_2O_3,) Si (SOI), SiC, GaN bulk, AlN bulk
- MOCVD reactor technology
  - design choices, cleaning, throughput, mono/multi, metrology
- Epitaxial technologies
  - Quality improvement (defects, structures, …)
  - Selective regrowth
- Business models

Power America public roadmap

POWERAMERICA

Draft Public Roadmap
May 2016



US current status

Very advanced GaN RF industry (for defense)

Lagging behind for power switching

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GaN Material Advantages per Application

Power Switching

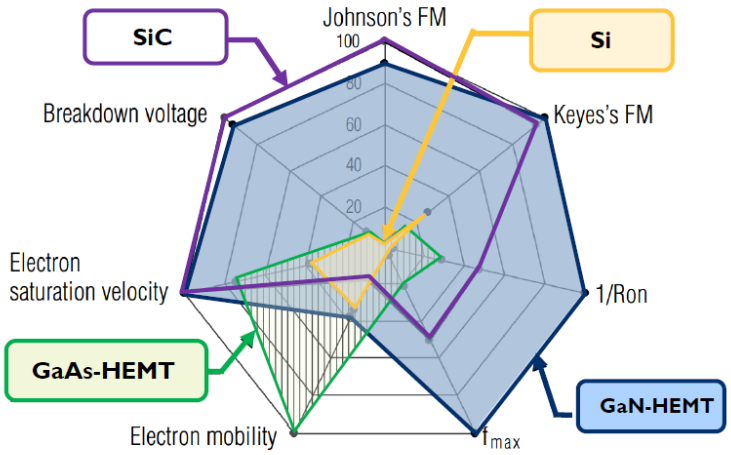
- R_{on}: up to 3 Orders oM improvement over Si
- No reverse recovery charge
- Very high dV/dt (~ 100V/ns)
- Frequency operation >> 100kHz => smaller & lighter systems
- High temperature capability

RF Power

- Excellent PA **linearity**, **PAE** and **P_{out}** per gate periphery
- High $L_{gate}/d_{barrier}$ aspect ratio to reduce short channel effects
- Two flavours:
  - *High-end* GaN on SiC
  - *Low-cost* GaN on Si

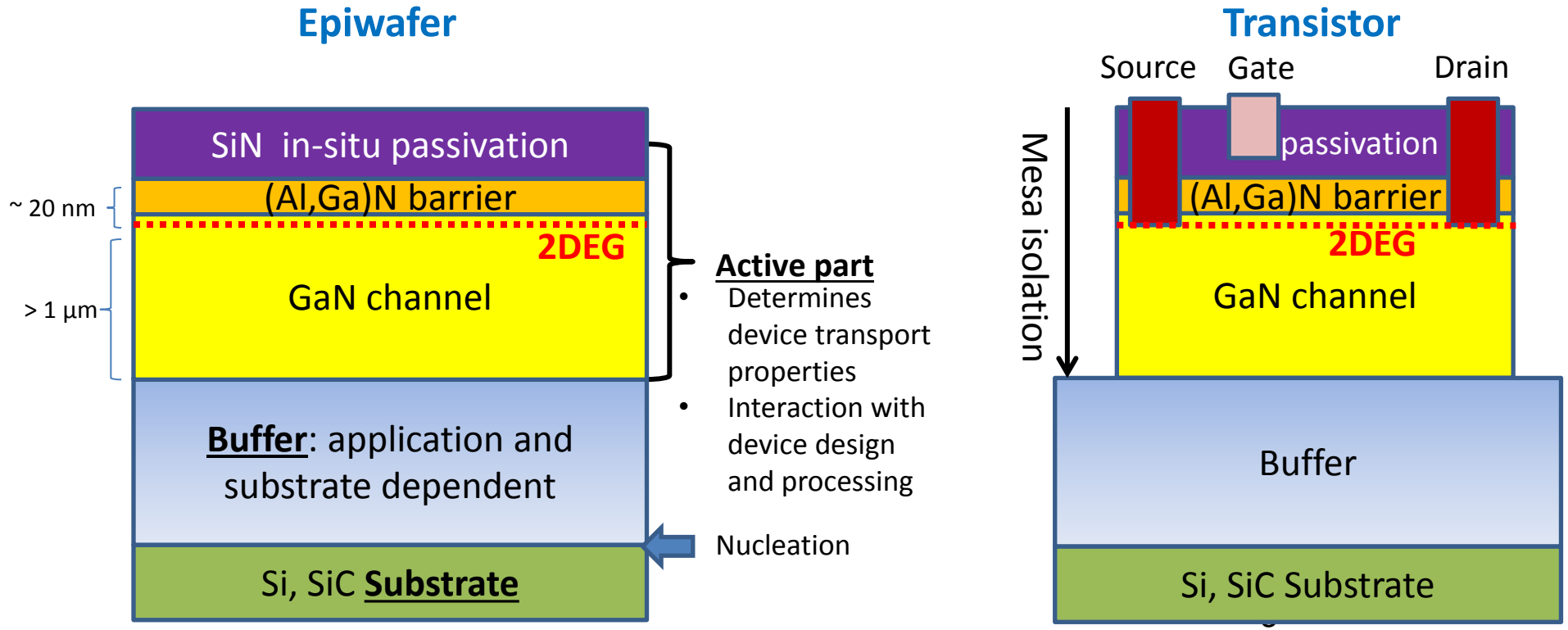
Sensors, MEMs, …

- Higher sensitivity
- Chemical inertness
- Temperature stability
- On-chip integration of multiple functions



Courtesy of Yole Development

Epiwafer stacks versus HEMT device



GaN material on the market today

One of the main questions is the choice of the substrate:

	RF	Power	Sensing	laser/LED
GaN-on-Si	2" to 200mm	2" to 200mm	R&D	R&D
GaN-on-SiC	2" to 6"	too high cost?		2" to 6"
GaN-on-sapphire	prev. gen.		R&D	2" to 200mm
GaN-on-GaN				2"

The choice of the substrate is determined by

- Cost
- Performance level (e.g. for defence/space)
- History

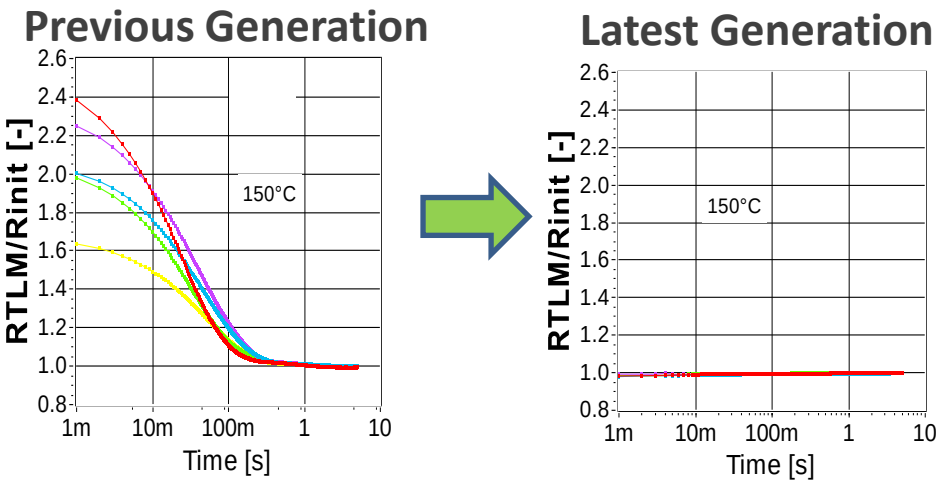
Power switching - Application requirements

- Power switching with GaN on Si
  - **Status**:
    - Quality commercial sources exist on 6”
    - reaching 1µA/mm^2 at ~ 800V, no current collapse
  - **Vertical leakage and breakdown**
    - Thickness scaling: now ~ 4.5µm for 600V -> xxx µm for 1200V and beyond?
    - Symmetric IV behaviour for both polarities (enables integrated H-bridge)
    - Choice of buffer types (proprietary?): SL, graded, IL, C-doped, …
  - **Trapping effects in the buffer**
    - Causes current collapse
    - Fundamentals: point defects e.g. C, V_{Ga}
    - Mitigation by proprietary designs: e.g. impurity profiling
    - Growing understanding through modelling (e.g. U Bologna / U Padova)

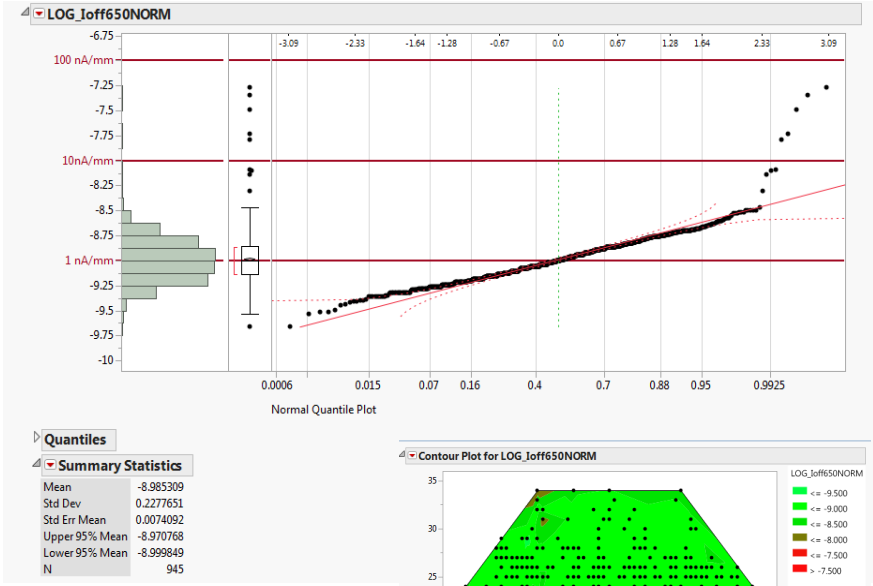
Power switching - Application requirements

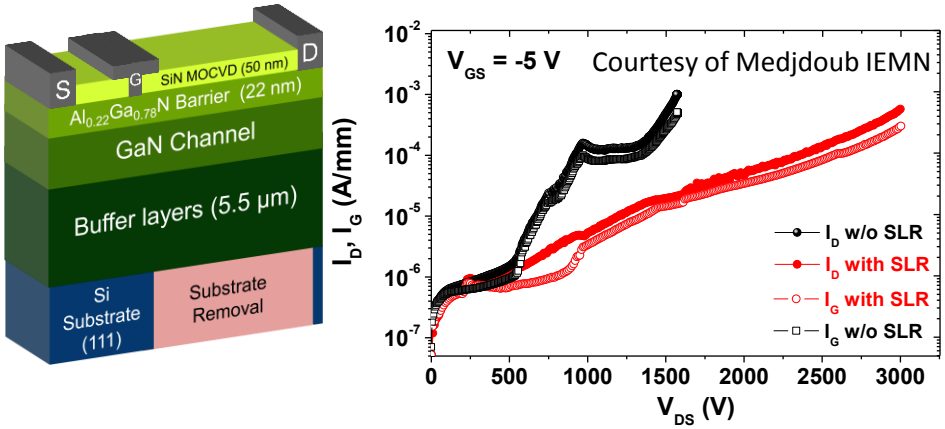
- Power switching with GaN on Si
  - **Semi standard substrates? Thickness may be an issue**
    - Tensile cooldown stress proportional to layer thickness
    - Matching compressive stress built up during buffer growth
    - => Risk of plastic deformation at growth temperature
    - => Wafer breakage
  - **Conduction loss reduction**
    - HEMT heterostructure engineering InAlN/AlN/…
  - **Cost road-map -> reactor design**
    - Throughput, yield, diameter scaling
  - **Enhancement mode** by p-(Al)GaN: doping levels, diffusion profiles
  - **Integration options** with Si CMOS (cf. TI, Dialog), e.g. for gate driver

Power switching – performance data



Elimination of HT current collapse





Uniform low leakage current across 6”

Si back end processing allows for **3000 V** operation

Current status of GaN-on-Si

Threats/weaknesses:

- The buffer stack is critical
  - Causes limitations for breakdown, current collapse, RF loss
- High density of threading dislocations & point defects
  - Critical threshold values to achieve reliable devices have not been identified
  - Mechanisms not fully understood
- Drive towards thicker epilayers for power
- Cost roadmap

Strengths/Opportunities:

- Main (proven?) choice for power, increasing interest for RF
- Scaling diameter is on-going (now at 200mm)
- Si fab compatibility
  - substrate thickness and contamination
- Easy back-side processing
  - E.g. TSV, local substrate removal, replacing Si by diamond
- Novel integration options, e.g. through SOI, 3D stacking, …
  - Gate drivers, RF digital front end and RF filters, …

Current status of GaN-on-SiC

Threats/weaknesses

- Reliable roadmap for cost ?
- Diameter scaling to/beyond 6” ?
- Some issues with processing:
  - Usually in dedicated III-V fabs on 3” or 4”
  - TS(iC)V, wafer thinning

Opportunities/strengths

- The established technology for RF (DC-100GHz)
  - For high end space/military, also for commercial applications (e.g. Sumitomo: JPN base stations).
  - Mature technology: MMIC-level
  - Little interest from power switching
- Established value chain (epi / foundry / system)

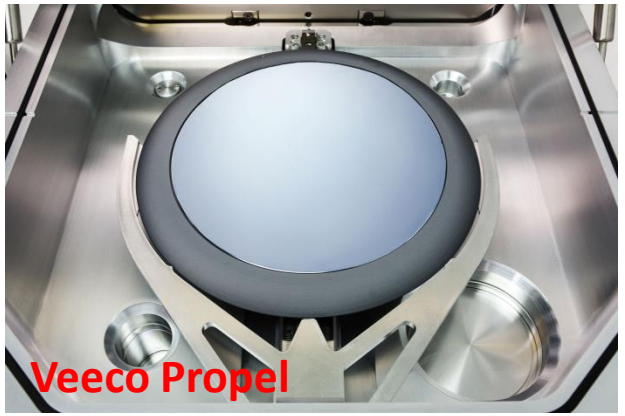
Topics for epitaxy development

- Quality improvement for enhanced reliability
  - Reduction of TD density
    - Nucleation, buffer designs
  - Understanding of fundamental behaviour
    - structural & crystal investigations
    - Modelling
- Higher voltage: thicker / better buffers
  - 600V -> 900V -> 1200V
- Low Rsheet heterostructures
  - E.g. InAlN ~ 220 Ohm/sq
- Selective regrowth
  - n-GaN for ohmic contacts
  - p-GaN for e-mode gates, vertical transistors
  - For combined GaN/CMOS
  - Requires integration in device process flow

Cost: Directions in Reactor technology

YIELD & THROUGHPUT

- MOCVD or MBE or HVPE or …
  - MOCVD for the mainstream
  - MBE for regrowth?
- Reactor design (=> yield)
  - Gas injection
  - Heating strategy
  - Internal geometry (multiwafer / single wafer)
  - Wafer handling
- Reactor cleanliness
  - Essential to achieve yield of GaN on Si
- Throughput
  - Cycle time: growth rate, cleaning process
  - Multiwafer versus single wafer tools
  - Automation for wafer handling & process control
- Metrology
  - In feedback loop for automated process control
- Target: < 500$ / 6”



Topics for the roadmap

- Diameter upscaling
  - to 200mm; even 300mm?
- Higher voltage capability for GaN-on-Si with lower R_{sh}
- Cost road-map
  - for SiC substrates
  - for GaN epitaxy
- Clarify the impact of crystal quality on reliability
- RF: GaN-on-X is the technology of choice for 5G
  - Metric: PAEfficiency at 30GHz
- Co-integration with Si CMOS
- Novel substrate materials