# BCD Smart Power Roadmap Trends and Challenges

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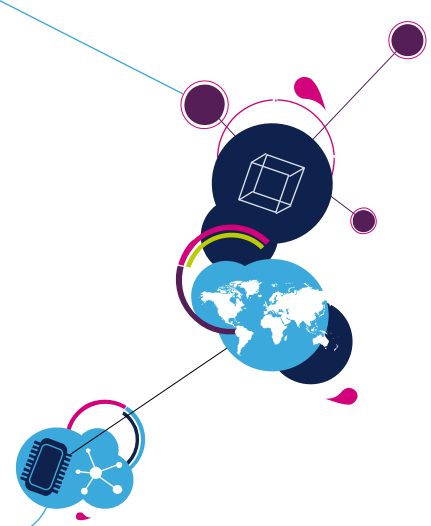
**NEREID WORKSHOP ‘Smart Energy’**

**Bertinoro, October 20th**



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# Outline



- Introduction
- Major Trends in Smart Power ASICs
- An insight on (some) differentiating enablers
  - Power Devices evolution
  - Enhanced Programmability (ePCM)
  - High Voltage applications
- Challenges & Conclusions

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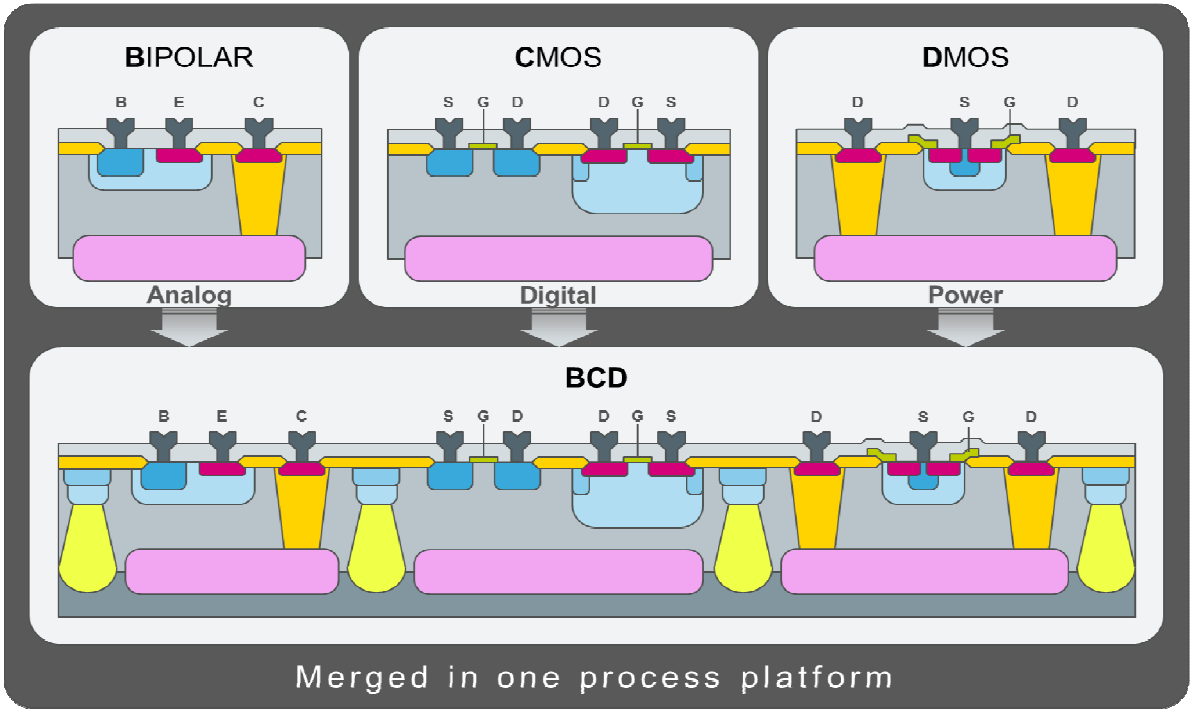
# What is BCD ?



## A concept introduced by ST in the mid-80s [1][2][3] widely used today in the industry



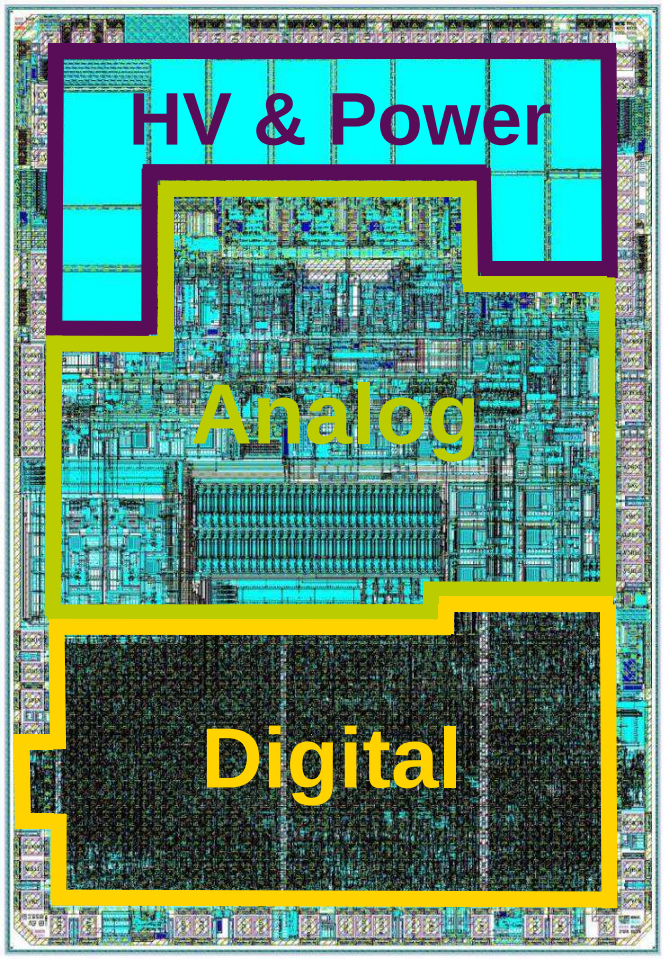

[1] ***Single Chip Carries Three technologies***, Electronics Week, December 10, **1984**

[2] *C. Cini, C. Contiero, C. Diazzi, P. Galbiati, D. Rossi, "**A New Bipolar, CMOS, DMOS Mixed Technology for Intelligent Power Applications"**,* ESSDERC '85 Proceedings, Aachen (Germany), September **1985**

[3] *A. Andreini, C. Contiero, P. Galbiati, "**A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic and DMOS Power Parts**",* IEEE Transactions on Electron Devices, Vol. ED-33 No.12, December **1986**

# Analog + Digital + Power & HV on one chip






**High Voltage & Power** section (DMOS) to drive external loads

**Analog** blocks
to interface the external world to the digital systems

**Digital** core (CMOS)
for signal processing

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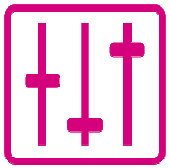
# ST BCD Roadmap Strategy

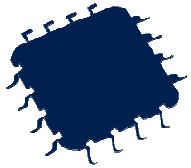




*Process customization by application & Differentiation*
***Introduction of innovative modules and materials***

*Performance Improvement & Area Saving : Power Evolution*
***New power architectures to maintain best-in-class performances***
***Leverage Power Discrete experience***

*Performance Improvement & Area Saving Lithography Nodes Evolution*
**Area reduction trend from lithography and increased wafer size thanks to ST's experience in Advanced CMOS**



*System Miniaturization & Area Saving: Assembly & Packaging*
**Secure optimized finishing solution compatible with state of the Art assembly/Packaging technology**

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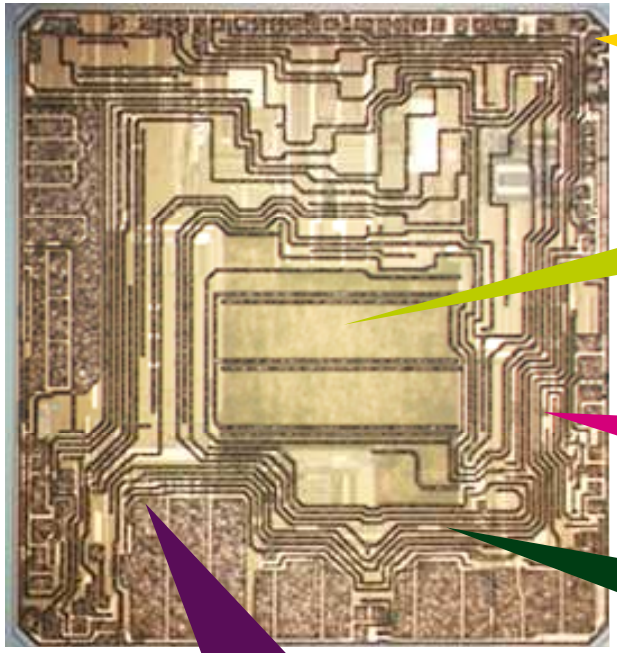
# Trends in modern Smart Power ASICs





**ISOLATION & INTEGRATION SCHEMES**
- **Junction Isolation**
- **Deep Trench Isolation**
- **SOI**

**LOGIC CORES**
- CMOS density

**SCALING BENEFIT** from **Litho Node Evolution**

**ANALOG FEATURES**
- Optimize Analog CMOS
- **Enrich Basic Device Offer** (NVM, Active, Passive)

**LARGE CURRENT ROUTING**
- **Thick Copper Metallization**
- **Bonding over Active Areas**

**POWER DEVICES**
- Specific ON resistance
- Specific Gate Charge
- Robustness

**POOR IMPROVEMENT** from **Geometry Scaling**

**Innovative Architecture** to **Optimize Performance**

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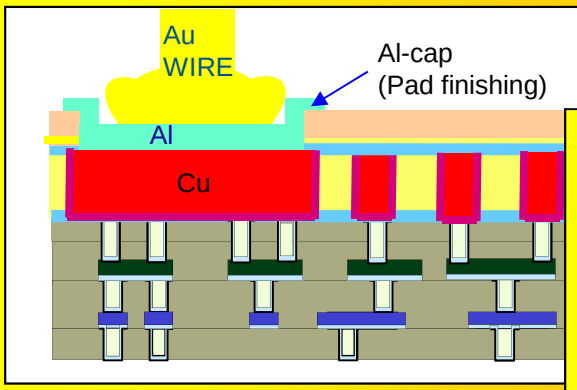
# Thick Cu Metallization schemes

## for High Current, High Power, Robust Bonding over Active Areas

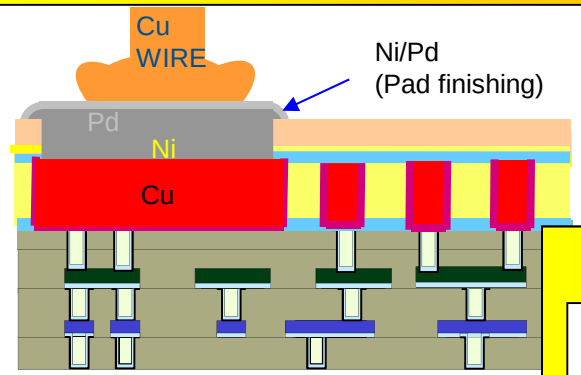


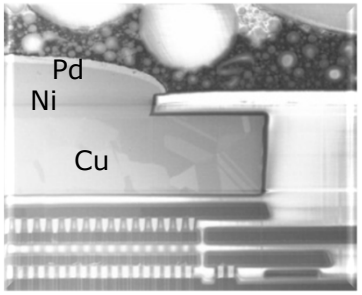
- **Ni/Pd Pad Finishing** for
  - Robust Bonding over Active Areas
  - Extended Temperature (>>150C) Reliability

### Cu-Damascene + Al-cap

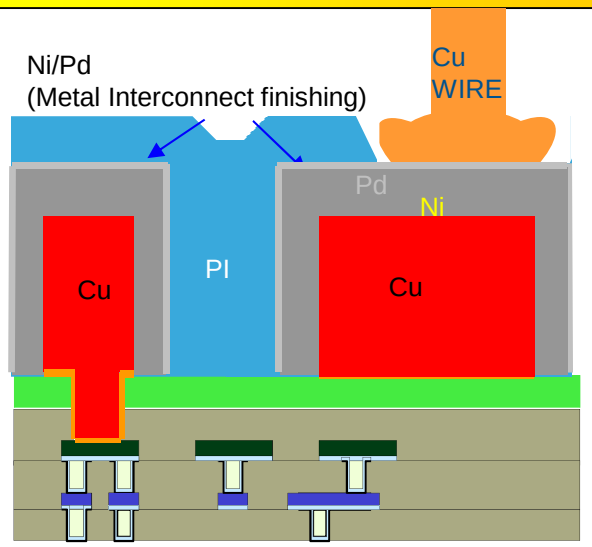



### Cu-Damascene + Ni/Pd

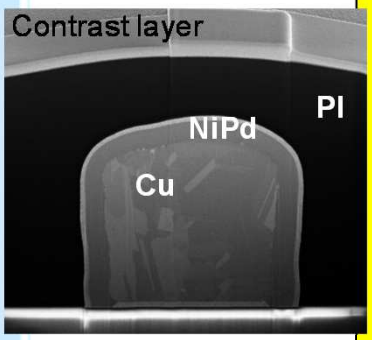



### Cu-RDL (Cu + Ni/Pd)



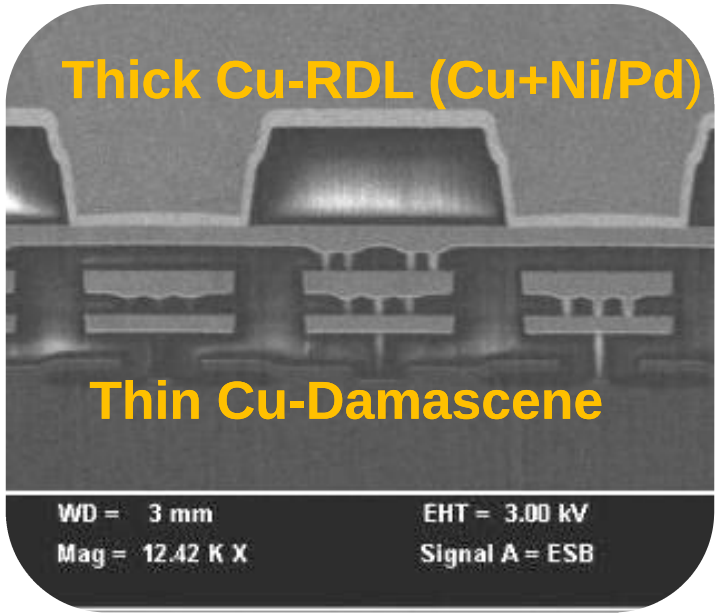

- **Thick Cu Metallization**
  for High Current / High Power
- **Cu-Damascene**:
  - lower thickness
  - finer pitches
- **Cu-RDL**:
  - higher thickness
  - larger Cu-wire diameter on active Areas
  - Lower Process Complexity



# Roadmap Evolution : Full Copper BEOL

Thin Damascene-Cu + Thick Cu-RDL






**Al BEOL**

**0.16µm FEOL & BEOL**
3 thin Al + 1 thick Cu metals
CMOS: 100Kgates/mm2

**Cu BEOL**

**0.16µm FEOL & 0.11µm BEOL**
3 thin Cu + 1 thick Cu metals
CMOS: 130Kgates/mm2

- +25% Increase of Logic Gate Density

**Al BEOL** ➡ **Cu BEOL** ➡ Increase of Energy Capability Robustness in Repetitive Power Pulsing working condition (ex.: Automotive ABS, Injector Valve driver ICs) where:

- High temperature gradients are generated inside power components
- The associated thermo-mechanical stress produces plastic deformation of metal layers and risk of loss of integrity of dielectrics

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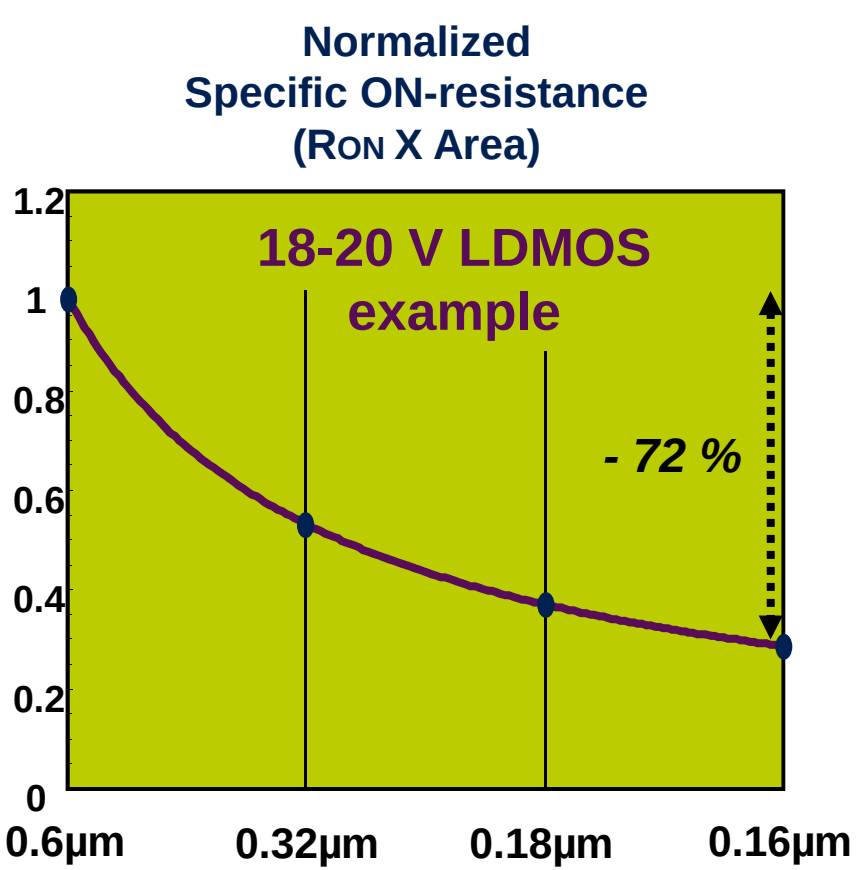
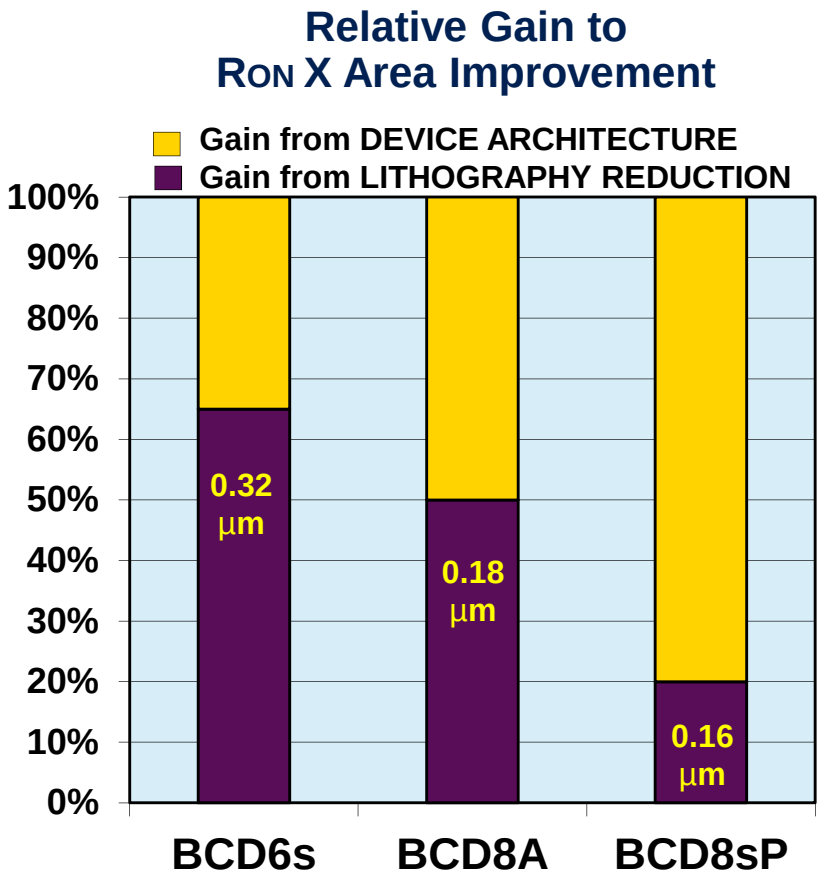
# Power Device Performance vs Lithography



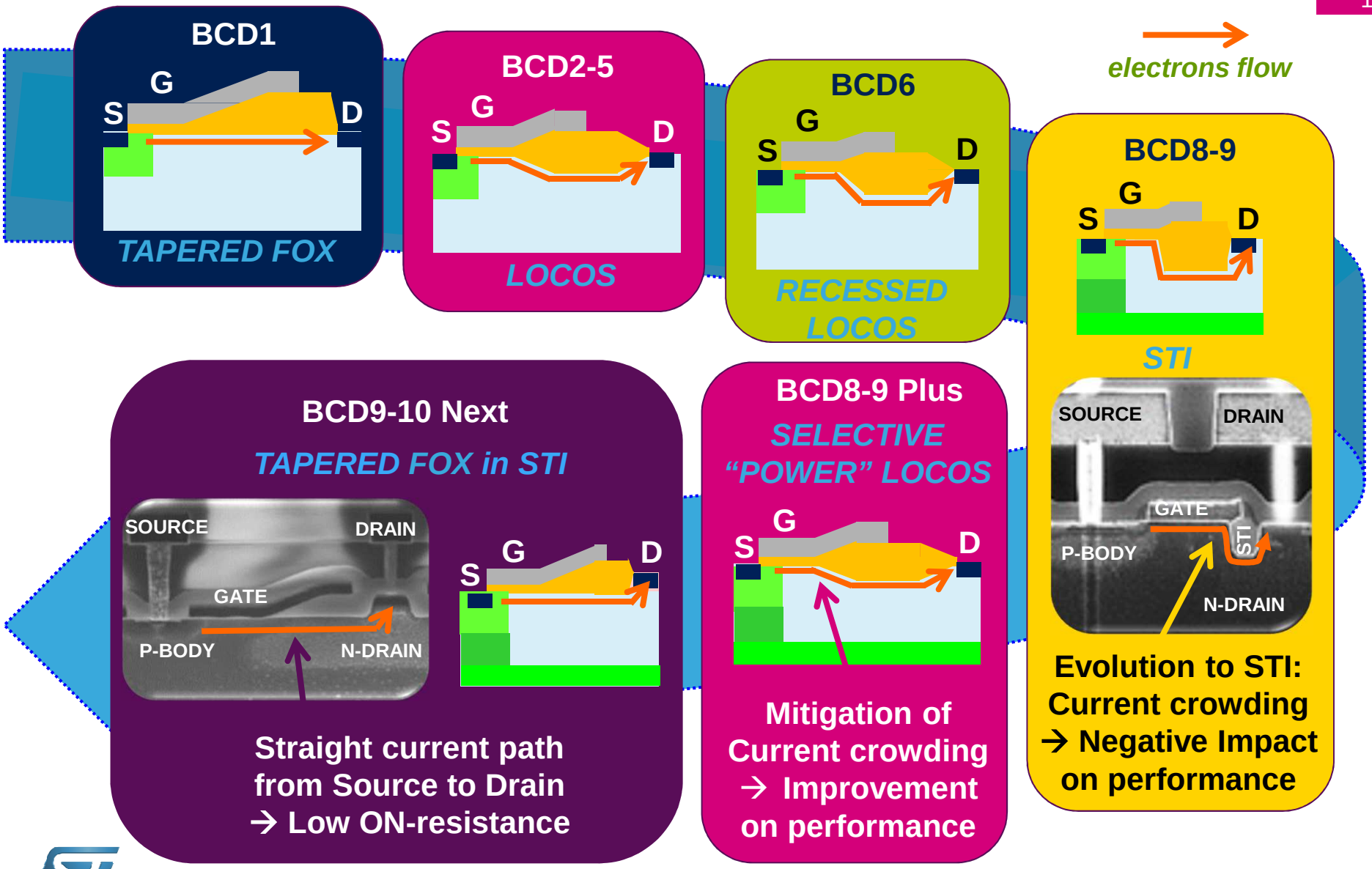
**POWER DEVICES AREA scaling down depends more and more on DEVICE ARCHITECTURE than on Lithography Feature Reduction**



# Evolution of Integrated Power Device Architecture

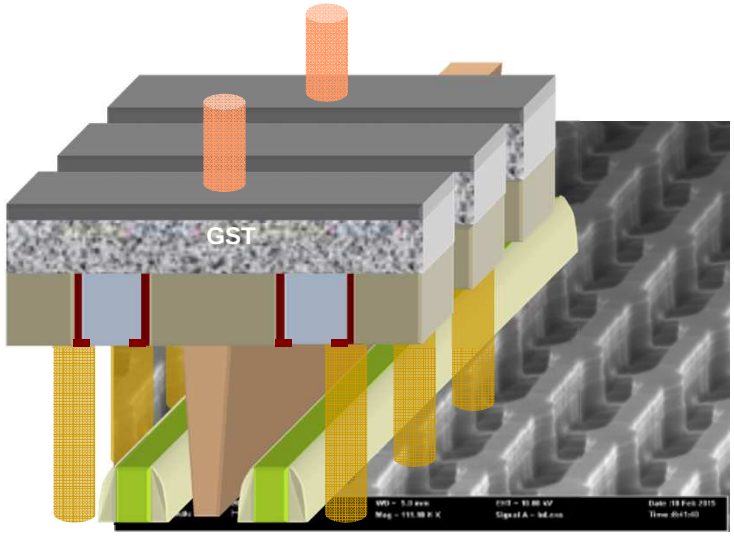




# Enhanced Programmability:
## embedded Phase Change Memory(PCM) value



- Microcontroller integration on Advanced Power ASIC (Motor Controller, Digital Power Managemnt, Wireless Chargers, Automotive Body) requiring ‘cheap’ NVM solution
- Novel Memory cell has been developed based on Phase Change Memory (PCM) materials




ePCM (Phase Change Memory)
in 110nm/90 nm BCD Platforms
for SOC applications

**Fully integrated Motor Driver**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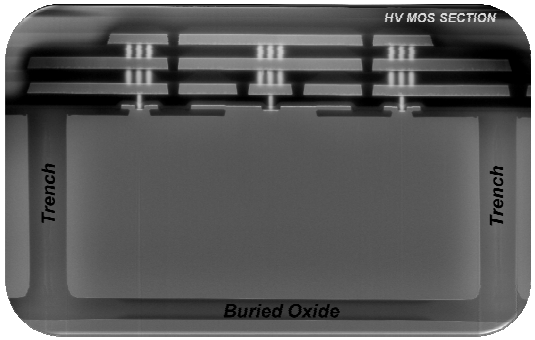
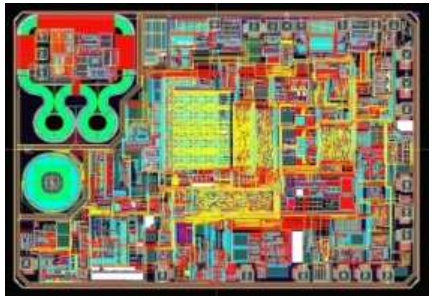
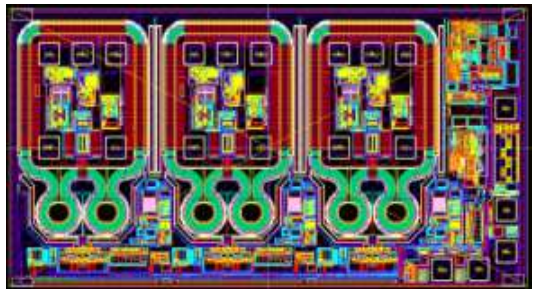
# Differentiation in Advanced BCD Technology
# …….not only Power & Litho……..



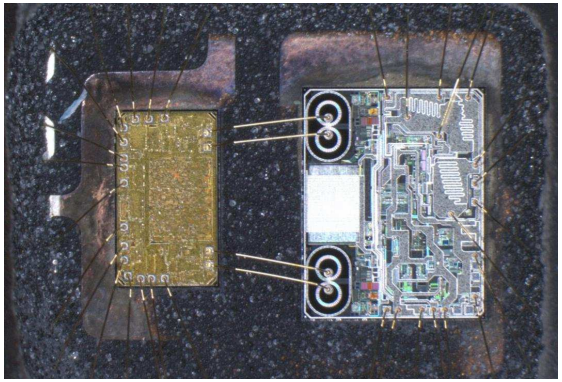


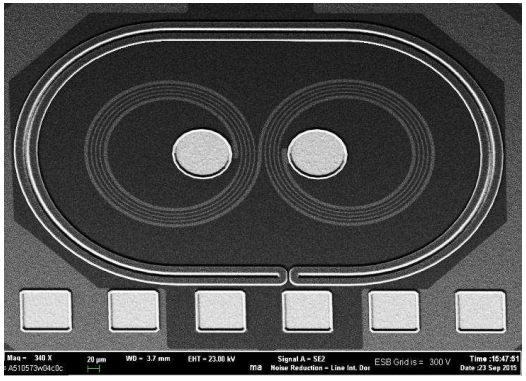

HV on SOI (200V to 300V)
on 0.16um BCD Platforms





HV (600V to 1200V) Gate Drivers
on 0.32um BCD Platforms





Galvanic Isolation (4KV to 6KV)
on 0.32um – 0.16um BCD Platforms

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# Next BCD development Challenges



## Lithography Scaling

- VLSI materials compatibility
- 300mm fabs availability
- Process complexity

## Power: $R_{ON}$ X $Q_G$

- New architectures ?
- New Materials ?
- SOA tailoring? Aging models?

## Future System Needs

High Efficiency High switching f

Galvanic Isolation

Wide and different voltage rating

COST, COST COST!


## System Partitioning

- SiP: cost or performance?
- Thermal management
- Logic or Power intensive?

## Differentiation

- New Memory
- High Performance Passives
- ‘Very’ High Voltage applications

# Conclusions



- ***Smart Power BCD Technology  is 'slowly' evolving towards Advanced CMOS Platforms***
- ***Process customization and differentiation are key to boost technology platform competitiveness***
  - ***New Specific Modules (Cu RDL and DTI)  in volume production***
  - ***New Power device architecture  as cost redution enabler and to meet high efficiency/ high frequency Power management***
  - ***New features availability to enable new function integration***

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