ON Semiconductor®

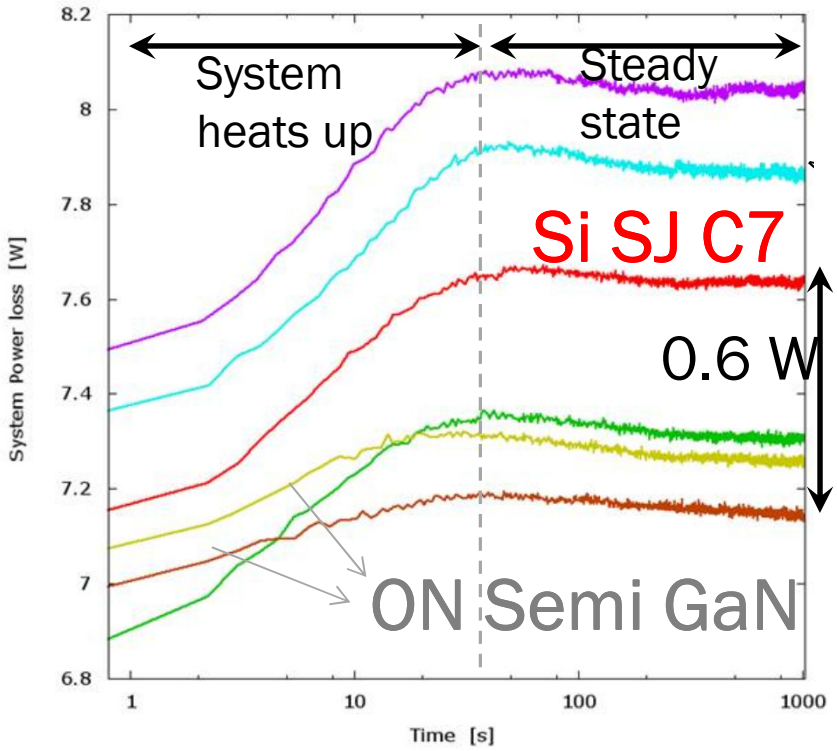
NEREID Roadmapping Workshop

Bologna, 20-21 Oct 2016

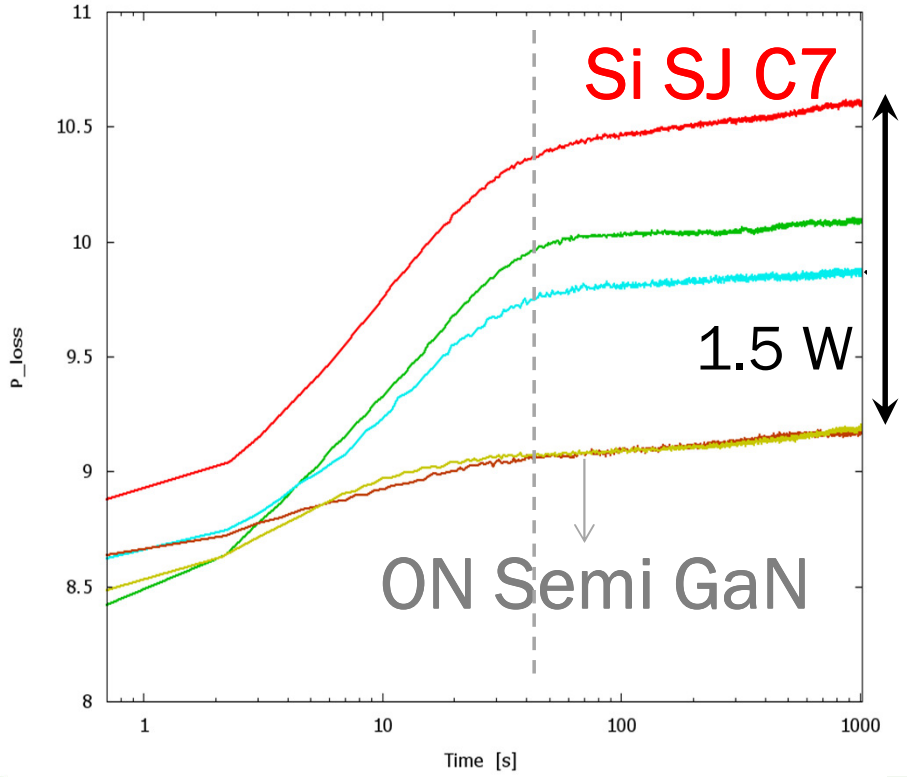
Energy Efficiency : GaN 1st Gen vs Si SJ

- 300W boost converter data (100→400V)
- Power loss in the total system. All devices assembled in surface mount packages.

- 100 kHz



- 200 kHz

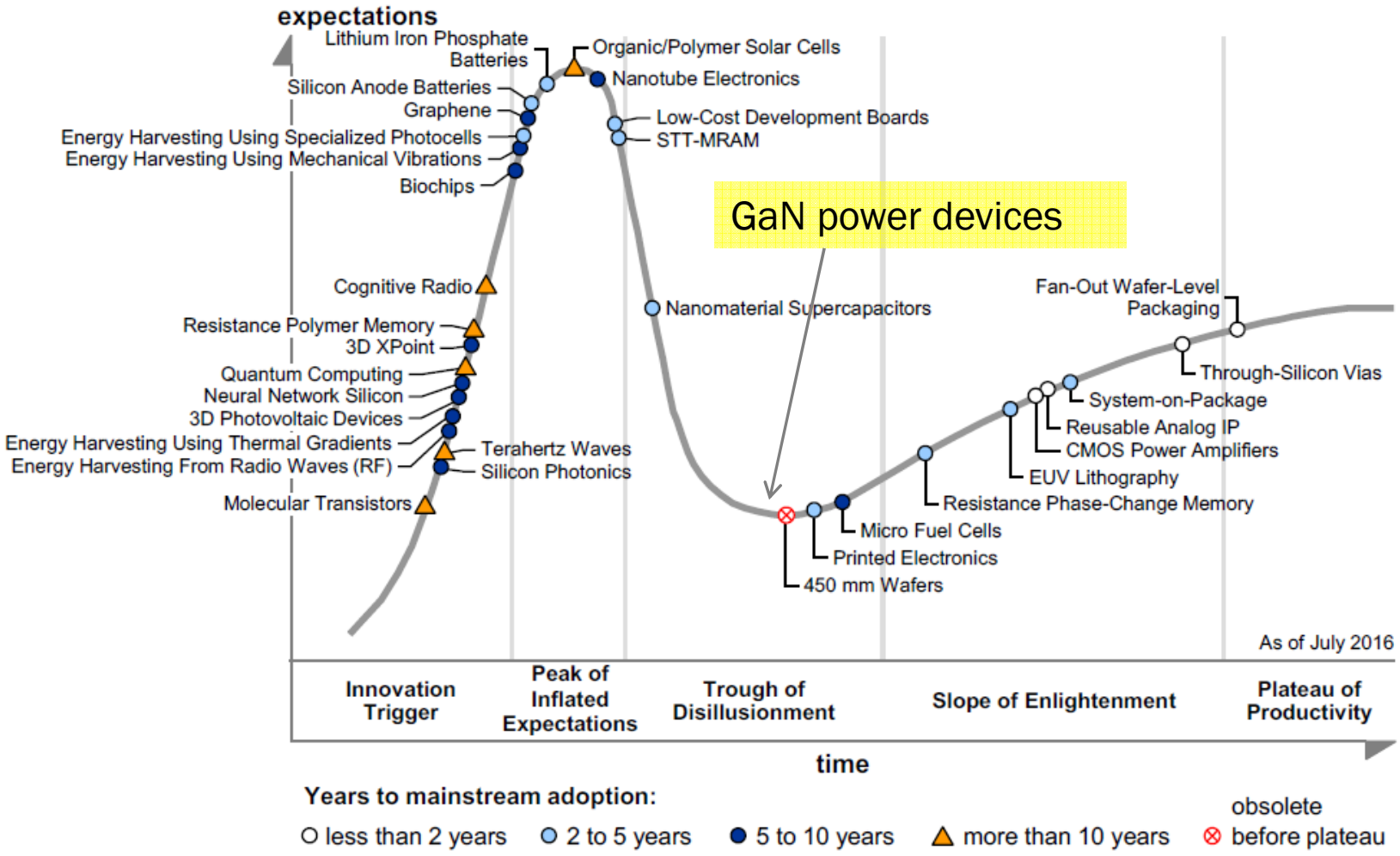


Goal

- What are the (potential) **roadblocks** hampering AlGaN/GaN power devices to be a **commercial success** ? (0-2 yrs out)
  - It is not their outstanding technical performance.
  - Cost
  - Reliability/Robustness
- Focus for **near future** developments (2-5yrs out)
  - Higher Voltage (1.2kV)—Thicker buffers, substrate removal, others
  - Higher currents
  - Bi-directional switches (AC-AC matrix convertors)
  - Co-integration (logic—power). All-GaN or hybrid.
- **Far Future**–New materials (5-8yrs out)

Hype Cycle for Semiconductors and Electronics Technologies

Figure 1. Hype Cycle for Semiconductors and Electronics Technologies, 2016



Source: Gartner (July 2016)

Where is the money ? → 600V class

- Total Power Semiconductor market ~25B$
  - Si SuperJunction market ~2.2B$ in 2020
  - IGBT market ~1B$ in 2020
- By 2020, GaN is expected (hoped) to take 25% of Si SJ market **[but depends on when cost parity with Si is achieved]**

Efficiency is key…
but cost is king

Potential GaN roadblocks (1)

- Customers want cost parity at the device level
  - Replace e.g. Si SJ device by a GaN device that yields at par or better system efficiency
- GaN-on-Si wafer cost is (too) high
  - Multi-wafer reactors/New concepts
  - Growth on CTE matches substrates (poly-AlN, …)
  - Others….to reduce growth time and DD
  - Au-free processes (standard Si CMOS fabs)
  - 150mm versus 200mm (vs 300 mm ?). Is there a cost advantage ?

What about reliability ??

Potential GaN roadblocks (2)

- GaN Reliability is different from Si (JEDEC) and is not well enough understood.
  - JEDEC is a minimum requirement, but we need more (GaN specific testing like Dyn Ron)
    - What tests ?
    - What failure modes ?
    - Recoverable vs permanent ?
    - What acceleration models ?
    - Distributions of failures ? Statistical models ?
  - Need for standardization committee/specs
    - Recently started by JEDEC

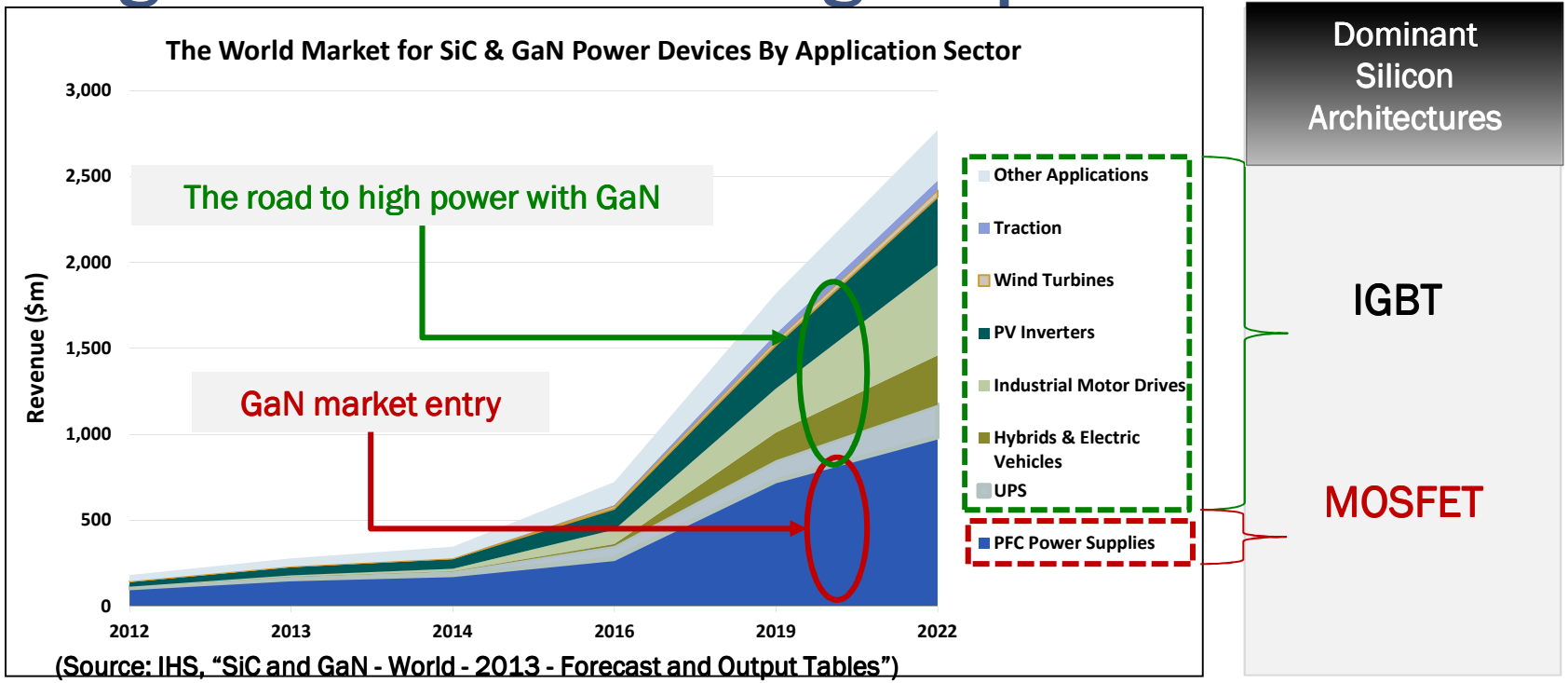
Potential GaN roadblocks (3)

- True E-mode versus cascode D-mode
  - Maximum gate overdrive/gate leakage for E-mode
  - What true E-mode approach ? Industry seems to converge to pGaN, but not commonly accepted.
  - dV/dt control of midnode voltage in cascode ? EMI ?
  - Cost E-mode versus D-mode
- GaN devices benefit more at higher frequency
  - Passives and EMI are limiting factors.
- (Lack of) Robustness and short circuit capability

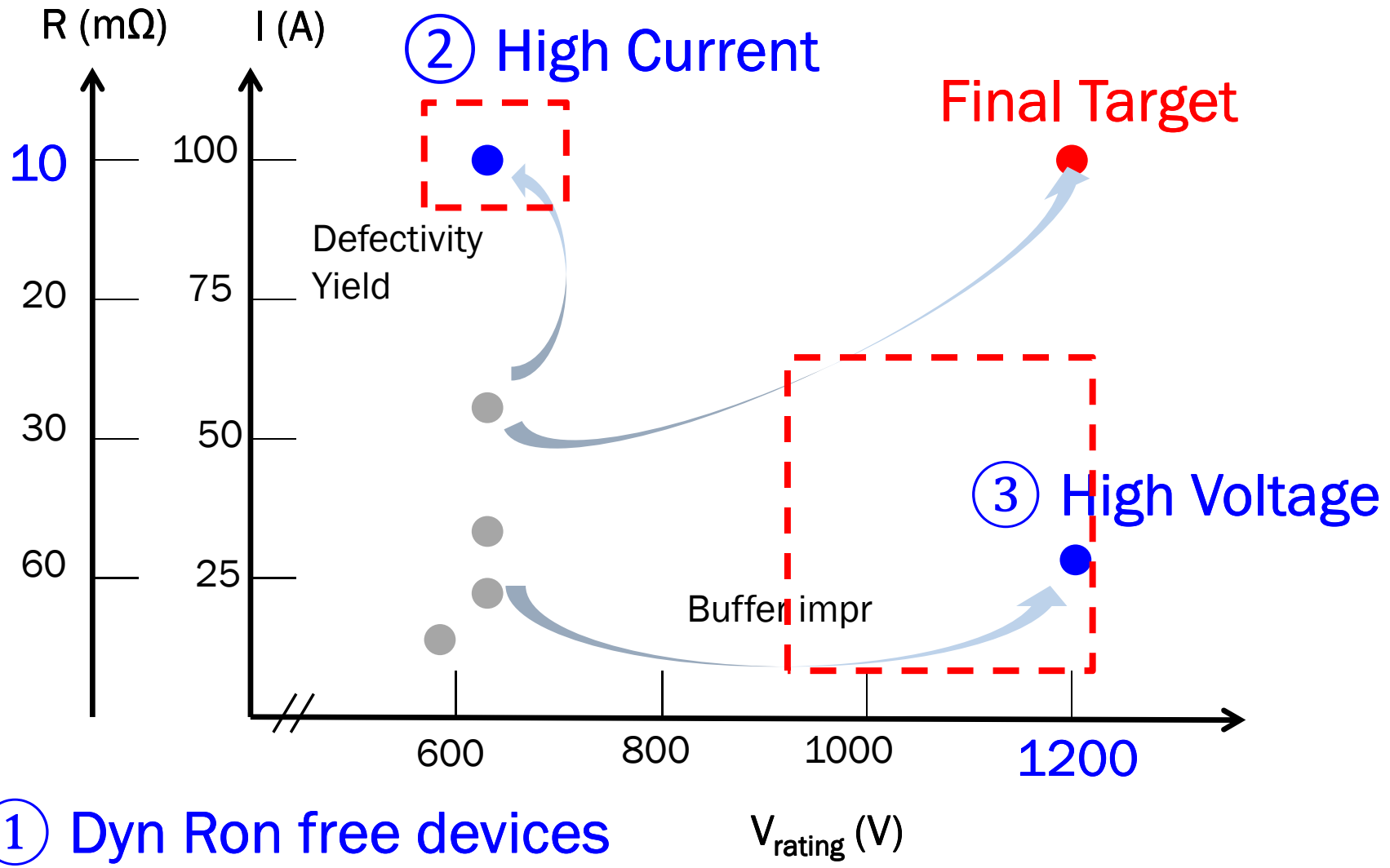
What's next ? (2-5yrs out)

Application Landscape

- GaN has proven efficiency/performance gain over Si SJ and SiC for low power (<5kW), 600V, see also https://www.littleboxchallenge.com/
- Large market also for higher power



Target setting



2-5yrs out

- Si substrate removal (HV and low cost)
- GaN modules
- Co-integration of logic with power devices
  - All-GaN
  - GaN with Si ((100) vs (111))
- Bi-directional switches

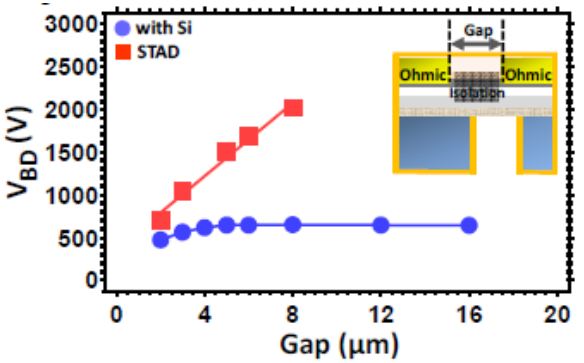
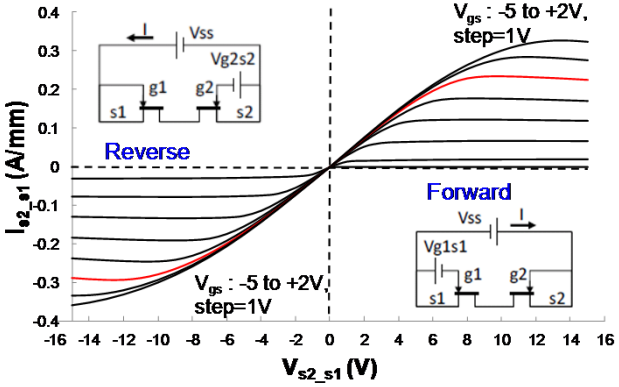
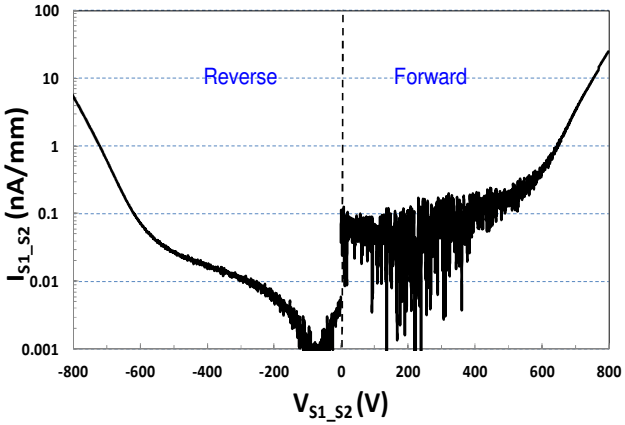
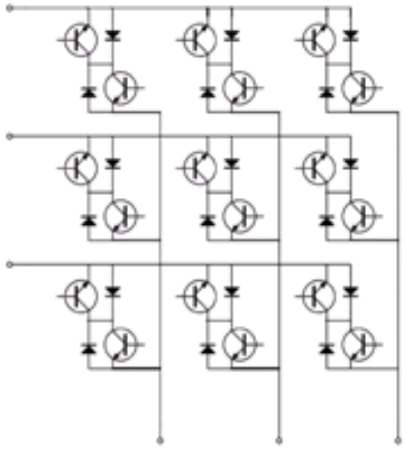


Figure 3 – Buffer V_{BD} versus Ohmic gap. A linear dependency of V_{BD} on gap is measured after trench processing (compared to a saturated V_{BD} of 650 V before processing) with extracted electric field strength of 2.5 MV/cm. The buffer isolation test structure is shown in the inset.







2-5yrs out

- All-GaN Smart Power technolog

Integrated Voltage Reference and Comparator Circuits for GaN Smart Power Chip Technology

King-Yuen Wong[1], Wanjun Chen[1,2], Kevin J. Chen[1]
[1)] Department of Electronic and Computer Engineering,
Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong
[2)] State Key Laboratory of Electronic Thin Films and Integrated Devices,
University of Electronic Science and Technology of China, Chengdu 610054, China

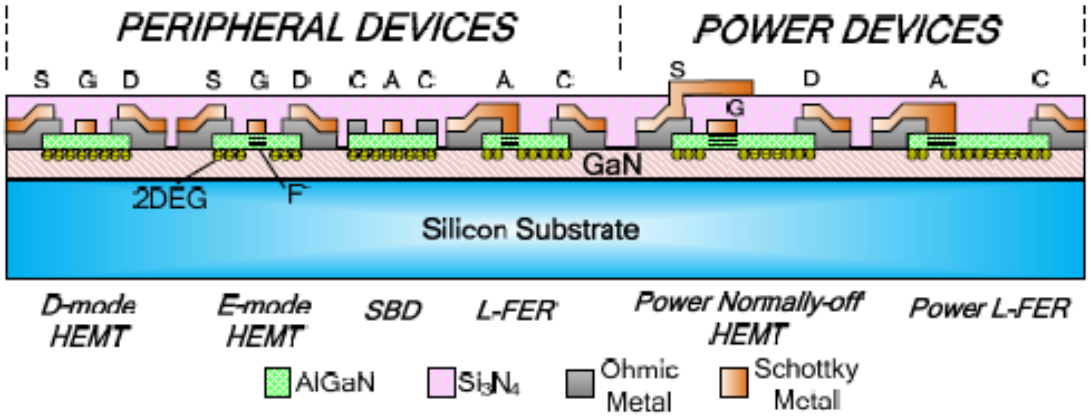


Fig. 1. Schematic platform of GaN smart power technology: integration of low-voltage peripheral and power devices.

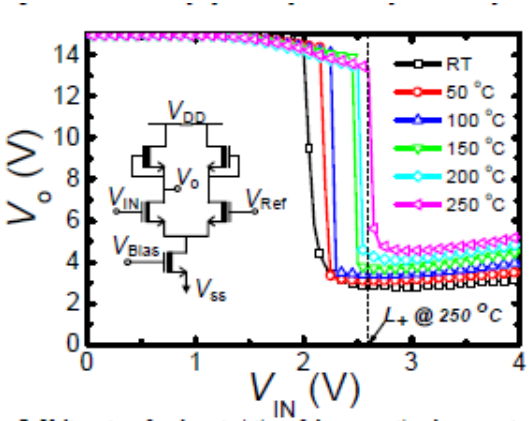


Fig. 7. Voltage transfer characteristics of the conventional comparator at different temperatures (measured at V_{DD} = 15 V and V_{Ref} = 2 V).

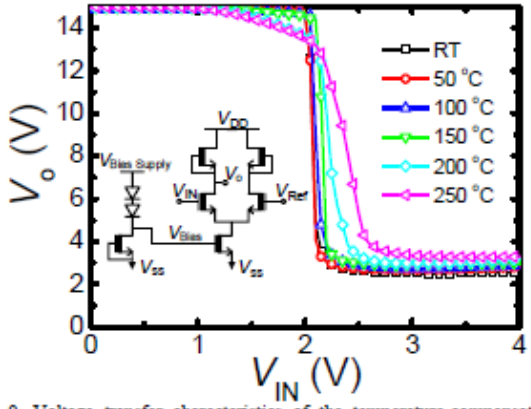


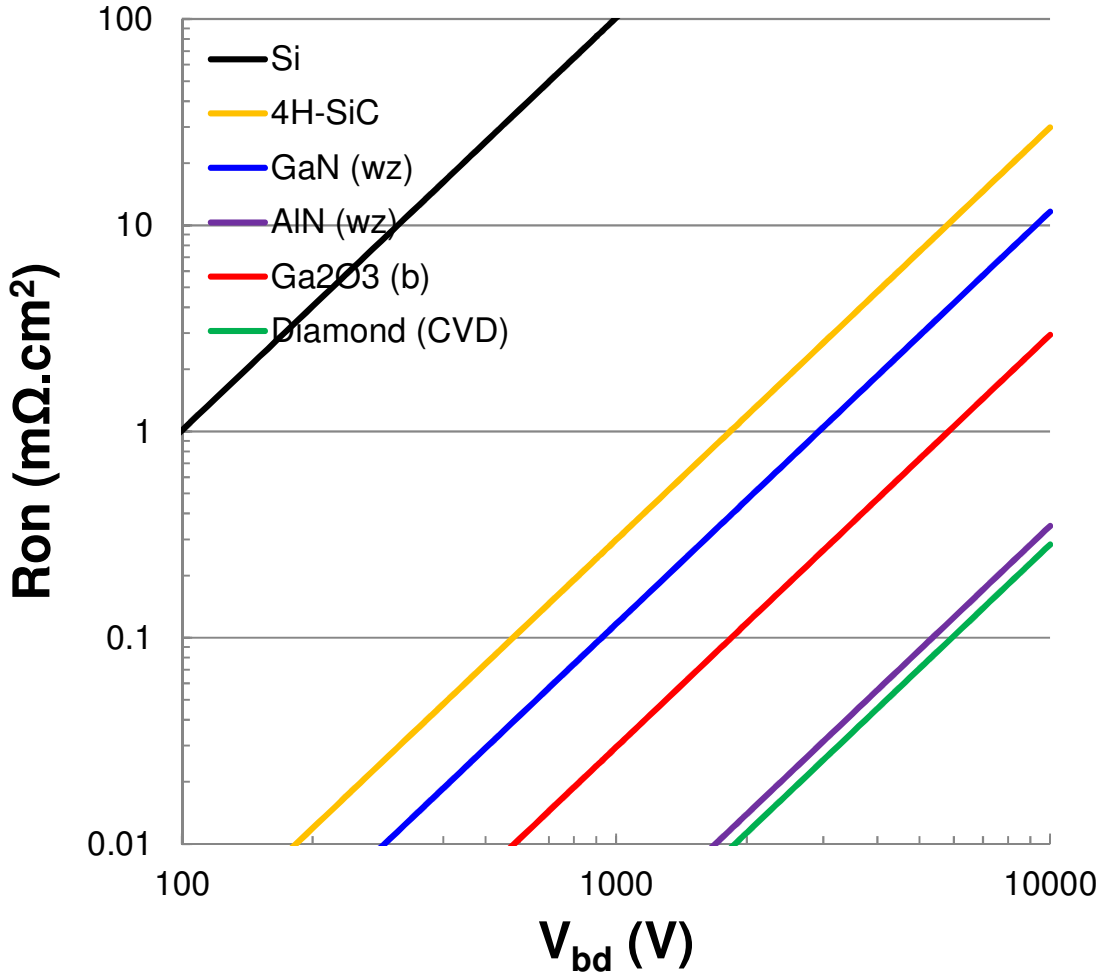
Fig. 9. Voltage transfer characteristics of the temperature-compensated comparator at different temperatures (measured at V_{DD} = 15 V, V_{Ref} = 2 V and $V_{Bias\ Supply}$ = 2.95 V).

Future work (3-5 yrs out)

- Homo-epitaxy/Vertical devices (3-5 yrs out)
  - SiC super Junction ?
  - Vertical GaN : Can it ever be cost-competitive to SiC ?
- U-WBG materials (5-8 yrs out)
  - AlGaN
  - AlN
  - Ga_2O_3
    - beta phase can be grown from the melt
    - Alfa phase allows to grow ternary structures
  - Diamond
  - ....

Novel Materials … Figure of Merit

- Figure of merit is deceiving



- U-WBG materials
  - No p-type doping ?
  - What market ? Very high voltage ? (small market)
  - Cost !!!
  - **Energy efficiency cradle to grave ?**