WP4 Functional diversification
Task 4.2 Smart Energy

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1st Domain Workshop

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WP4 Energy diversification

- WP4 will define the **strategy** for a roadmap for those **technologies** that **extend the field of application** of semiconductor technologies by **adding new functionalities or extend application range**.
- These technologies, falling under the denomination of “More than Moore”, do not scale simply with geometrical size, and are widely diversified; **therefore new metrics will have to be identified for the roadmap**. It includes two main Tasks:
- T4.1 Smart Sensors
- **T4.2 Smart Energy**

Task 4.2 Smart Energy

Industrial Co-Leader			
WP4	4.2 Smart Energy	W. Dettmann	Infineon
General and Domain Workshops			
WP4	4.2 Smart Energy	Mikael Östling	KTH
WP4	4.2 Smart Energy	Steve Stoffels	IMEC
Domain Workshops			
WP4	4.2 Smart Energy	Gaudenzio Meneghesso	UniPD
WP4	4.2 Smart Energy	Peter Moens	On Semi
WP4	4.2 Smart Energy	Joff Derluyn	EpiGaN
WP4	4.2 Smart Energy	Anton Bauer	Fraunhofer IISB
WP4	4.2 Smart Energy	Thomas Harder	ECPE Directoe
WP4	4.2 Smart Energy	Thomas Detzel	Infineon Villach
WP4	4.2 Smart Energy	Peter Steeneken	NXP
WP4	4.2 Smart Energy	Giuseppe Croce	STMicroel
WP4	4.2 Smart Energy	Braham Ferreira	TU DELFT

WORKSHOP

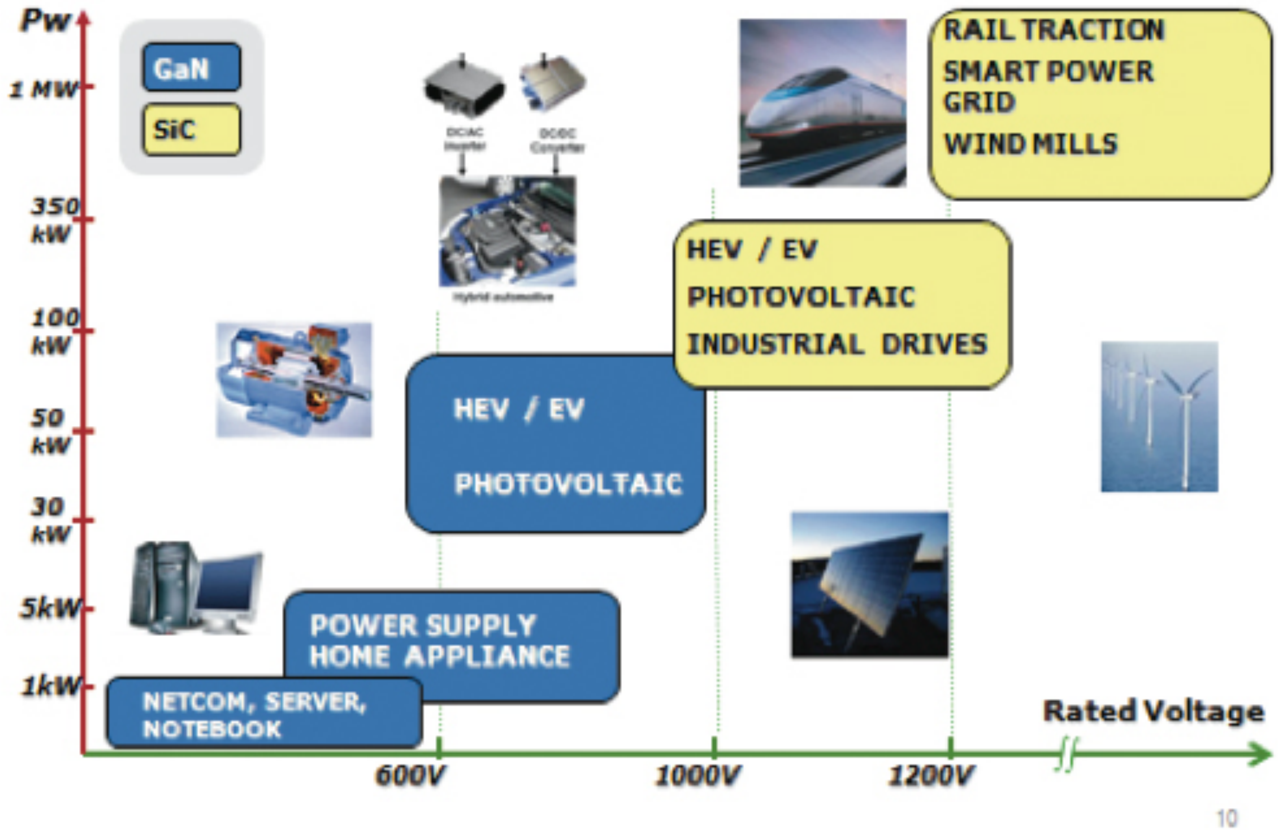
	NEREID Workshop 4 – Task 4.2 "Smart Energy" Chairman: Gaudenzio Meneghesso – IUNET Italy
09:00 – 09:10	Gaudenzio Meneghesso, University of Padova "Opening of the Workshop"
09:10 – 09:30 09:30 – 09:50 09:50 – 10:10 10:10 - 10:30	Mikael Östling, KTH, "SiC power switch device status and predictions". Peter Moens, ON Semi "Status and oulook of GaN power devices from an industry perspective" Giuseppe Croce, STMicroelectronics "Smart Power Technology Roadmap and Trends" Thomas Detzel, Infineon "GaN in a Silicon world: Competition or Coexistence?"
10:30 – 11:00	Break
11:00 – 11:20 11:20 – 11:40 11:40 – 12:00 12:00 – 12:20 12:20 – 12:40	Joff Derluyn, EPIGAN, "GaN from the epitaxy perspective" Steve Stoffels, IMEC "Outlook for 200mm E-mode device technology" Anton Bauer, Fraunhofer IISB "Potential of SiC for Automotive Power Electronics" Thomas Harder, ECPE, "WBG System Integration" Braham Ferreira, TU Delft "International Technology Roadmap for Wide Band-gap Power Semiconductor ITRW"
12:40 – 14:00	Lunch
14:00 – 17:30	Discussion for road-mapping ONLY for NEREID experts and members Coffee break during the discussion

Task 4.2 Smart Energy: Objectives

- To identify the **best application of Power Si and wide band-gap semiconductors** devices (WBS) and provide a clear indication on **where these devices will be disruptive** in their applications;
- Highlight all the **technological** and **material** issues that need to be solved in order to guarantee a large market penetration of these devices;
- To provide a roadmap for the “standard” Si-based technology and the market penetration of WBS devices taking into account **cost/benefit analysis**, the degree if maturity and its expected evolution.

Task 4.2 Smart Energy : WBS

To identify the **best application of wide band-gap semiconductors** devices (WBS) and provide a clear indication on **where these devices will be disruptive** in their applications;



Task 4.2 Smart Energy : WBS

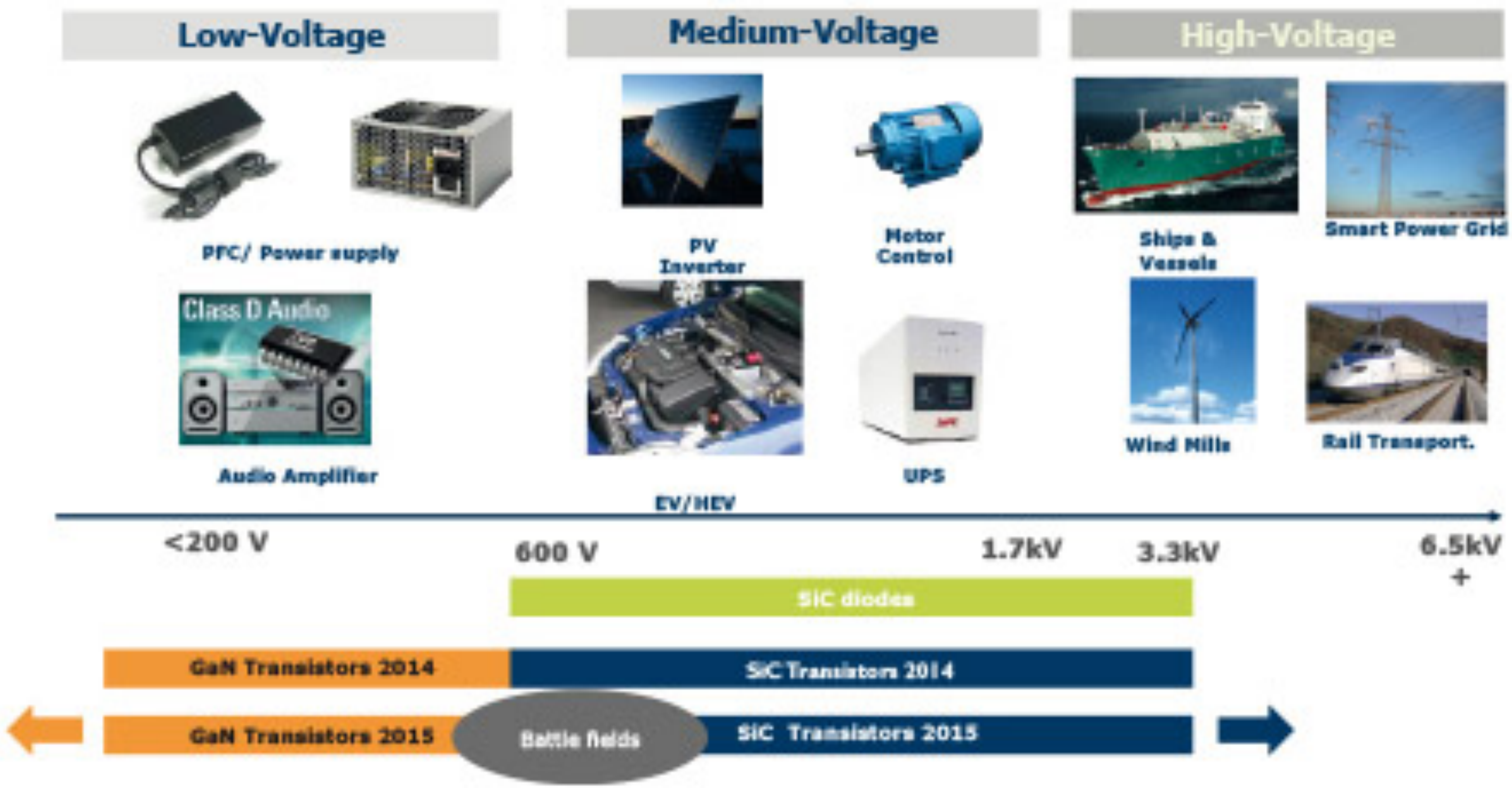
To identify the **best application of wide band-gap semiconductors** devices (WBS) and provide a clear indication on **where these devices will be disruptive** in their applications;

- Power conversion
- Power circuits, esp for EV/HEV, HVDC and PV
- Smart grids
- Compact convertors
- Wireless chargers
- Envelope trackers
- New topologies benefiting from low Qrr and fast switching
- High temperature operation
- High power RF
- ……..

WP4.2 - Market

WBG Market segmentation: GaN versus SiC, as a function of voltage range

(Source: *GaN and SiC for power electronics applications report*, July 2015)



Task 4.2 Smart Energy : WBS

wide band-gap semiconductors:

Fast switching is the key for **size and weight reduction** with WBG power semiconductors **leading to several issues**: **EMC, low parasitic inductances of the packaging and interconnection technologies, power losses related to passive components, need for system integration solutions, optimised switching cell, integrated drivers**, ...

As a consequence, the extreme miniaturization of power electronic systems leads to **higher power density** which requires **new improved cooling techniques**, but also leads to higher operation (and junction) temperature.

Issues related to high temperature power electronics: advanced materials and processes for **packaging** and **interconnection** (chip level and system level), **polymer moulding & encapsulation**, substrates, **temperature range for passive components**, **robustness and reliability**, ...

Task 4.2 : Issues

Highlight all the technological and material issues that need to be solved in order to guarantee a large market penetration of these devices;

Technological and material issues

- Material (substrates, quality, reproducibility, supply chain, wafer size, maximum thickness for heteroepitaxial growth)
- Processing issues (contacts, gate, isolation)
- Normally off operation (hybrid or intrinsic)
- Isolated gate (MIS) devices
- Sustainable breakdown, Operational (rated) voltage
- Robustness (UIS, short circuit) & Reliability
- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)ù
- Gate drivers
- …….

Task 4.2 : Roadmap

- To provide a roadmap for the standard Si-based technology and the market penetration of WBS devices taking into account **cost/benefit analysis**, the degree if maturity and its expected evolution.

Roadmap and cost/benefit for WBS

- Large wafer sizes, multi-wafer reactors
- New circuit topologies
- Novel device topologies (lateral vs vertical)
- Novel substrates (bulk GaN/alternative carriers)
- Reliability and stability of WBS
- New technologies at the interfaces for lower costs and higher reliability

Key figures of merit devices :

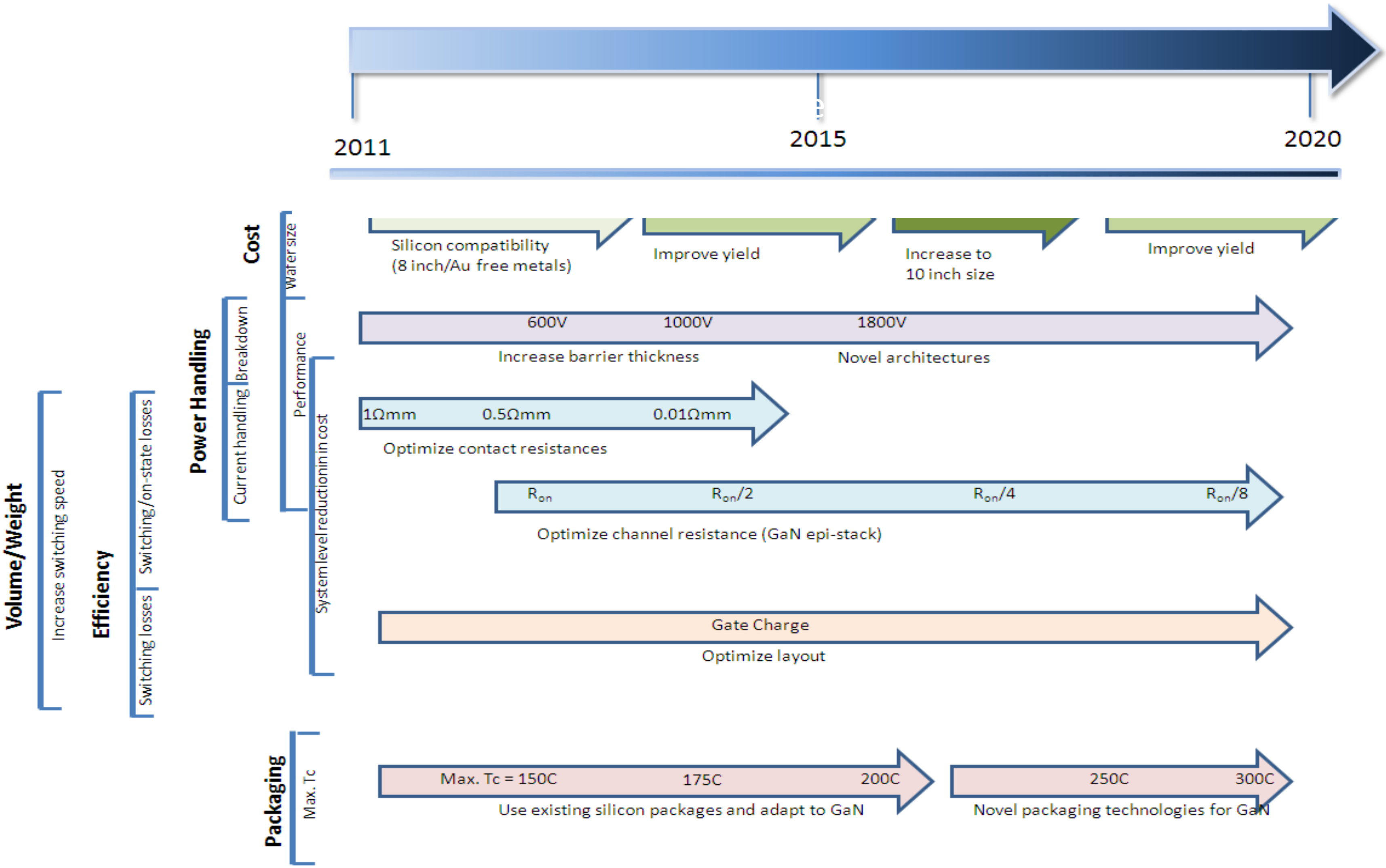
Device level

- Normally off – Vth > 2V
- Low gate leakage at maximum gate voltage
- Breakdown Voltage 650 V, 1200 V devices
- Ron vs Qg (efficiency vs speed)
- Dyn $R_{DS,ON}$ < 20% at maximum voltage
- Reliability/robustness > 20year
- Maximum operating channel temperature

System level point of view:

- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)
- Gate drivers

Timeline



2011
2015
2020
Cost
Wafer size
Silicon compatibility
(8 inch/Au free metals)
Improve yield
Increase to
10 inch size
Improve yield
Power Handling
Breakdown
Performance
600V
1000V
1800V
Increase barrier thickness
Novel architectures
Current handling
1Ωmm
0.5Ωmm
0.01Ωmm
Optimize contact resistances
R_{on}
$R_{on}/2$
$R_{on}/4$
$R_{on}/8$
Optimize channel resistance (GaN epi-stack)
System level reduction in cost
Gate Charge
Optimize layout
Volume/Weight
Increase switching speed
Efficiency
Switching/on-state losses
Switching losses
Packaging
Max. Tc
Max. Tc = 150C
175C
200C
Use existing silicon packages and adapt to GaN
250C
300C
Novel packaging technologies for GaN

Task 4.2 : Roadmap

Technologies and Performance criteria	Time horizon Short (<3 years) - Medium (<6 years) - Longer (>7) terms		
	<3	<6	>7
SiC devices (high voltage)			
Maximum current (A/mm)	200	300	400.
Maximum Voltage (V)	10 kV	20 kV	30 kV
Power dissipation (W/MM)	N/A (no microwave devices) …………		……………
Switching speed (kHz) (with better materials and longer lifetime we can not expect too much faster devices but instead much lower On-resistance)	100	200	200
Power consumption	…………	……………	…………
…….	…………	……………	…………
………			

Task 4.2 : Roadmap

Technologies and Performance criteria	Time horizon Short (<3 years) - Medium (<6 years) - Longer (>7) terms		
	<3	<6	>7
GaN devices			
Maximum current (A)	……100…….	……200………	…>200………
Maximum Voltage (V)	……650…….	……1200………	…1200………
Power dissipation (W/MM)	………….	……………	………….
Switching speed (kHz)	………250….	…500…………	……>750…….
Power consumption	………….	……………	………….
…….	………….	……………	………….
………			

Task 4.2 : Roadmap

Technologies and Performance criteria	Time horizon Short (<3 years) - Medium (<6 years) - Longer (>7) terms		
	<3	<6	>7
Passives			
Max operating Freq.	....	....	....
Power dissipation (W/MM)	....	....	....
Switching speed	....	....	....
Power consumption	....	....	....
....	....	....	....
....			

Task 4.2: Roadmap

Technologies and Performance criteria	Time horizon Short (<3 years) - Medium (<6 years) - Longer (>7) terms		
	<3	**<6**	**>7**
Packaging			
Power dissipation (W/mm)	………….	……………	………….
Switching speed	………….	……………	………….
Power consumption	………….	……………	………….
…….	………….	……………	………….
………			