Tunnel FETs trends and challenges

NEREID Nanoscale FET Workshop

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-NEREID H2020 ICT CSA-

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Introduction: Challenges of nanodevices

We are facing **dramatic challenges** dealing with future nano-scale devices:

- Performance
- *Power consumption ↑*
- **Many new materials** and **device architectures** needed (transistors, memories)
- Device integration (2D, 3D)
- **Interconnects** (Traditional, Optical, RF, carbon/2D materials)
- Ultimate technological processes (EUV, immersion multiple patterning, multi ebeam, imprint lithography, self-assembly)
- **Novel functionalities** (sensing, EH, RF) using **nanodevices** and **nanomaterials**

Big challenges to continue More's law:

Node-to-Node Transistor scaling:

- 50% area reduction
- 25% performance increase @ scaled V_{DD}
- 20% power reduction
- 30% cost reduction
  - every 2-3 years

⇒ Novel Lithography, Materials, Architectures, Physics, State variables… using **green & sustainable technologies** / power_scarce & toxic materials

⇒ Several 10^9 devices/circuit in Electronics: complex

⇒ Human kind: $100x10^{12}$ Synapses/Bacteria in brain/gut: **extremely complex (**sustainability **/** link with toxicity**)! Very far from this performance/low power!**

Why « very low power »?

- Cost of energy
- Climate warming / Pollution
- Restricted energy reserve
- Electronics: signicant part and ↑↑
- Battery lifetimes
- Future autonomous ULP systems

Introduction-Challenges

- ↑ **40%** energy consumption / 20 years

- ICT ~ **2 à 3% of worldwide CO2** emission
  (~ air transport)

- ICT ~ **15% of electricity consumption** (x3 next 20 years)

- In **2 days** ~ information generated until 2003
  (Eric Schmidt, Google CEO, 2010)

- **1 Google search** ~ energy consumption in 1h with energy saving bulb (source: Strato)

Introduction-Challenges

- 2 ZB : all recorded data in 2011
- **a day in digital world :**

  -10 K new Wikipedia articles
  -100 K hours of video posted on Youtube
  -400 M Tweets
  -500 M SMS
  -500 M Facebook connections
  -5 G searches on Google
  -150 G emails exchanges
  -40 TB of data collected at LHC (large hadron collider)
  15 PB / year later

Possible solutions for reducing energy dissipation in switching logic devices

-**Since the 90nm node Vdd scaling has been slowdown** leading to *accelerated energy consumption and heating*: move from constant field toward *constant voltage scaling*

=> end of λ^3 reduction of stored energy (and energy dissipated)

-**In 2005** the *increase in microprocessor frequency abruptly ceased*, integration level continue to increase and parallel processors were proposed to ↑ performance and/or ↓ power

-**Leakage current and power** dramatically increase (*can be > dyn.P*)

⇒ **2 paths for reducing energy dissipated** (most critical challenge):

- **Conventional logic**: reduction in stored energy (~CV^2 => dec. of C or V) and **I**leakage using new physics/materials/devices
- **Adiabatic/reversible logic**: E_{diss}=1/2 CV^2 (RC/ts) (ts: charging time of C) => the clock must be slow ts>>RC

Possible Solutions

- Reduction of energy consumption : **main challenge for future electronic systems**

  => A number of innovations will be needed:

  -**transistor and memory technologies**
  -**circuit design techniques**
  -**systems architectures**
  -**embedded software**

Possible solutions

- **Ex : Transistors :** energy consumption ~ 10^4 kT
  => limit ~ kT.

  => could be reached with nanodevices using **new physical concepts/materials and technology breakthroughs**

  => strong ↓ static and dynamic circuit consumption, with e.g.:

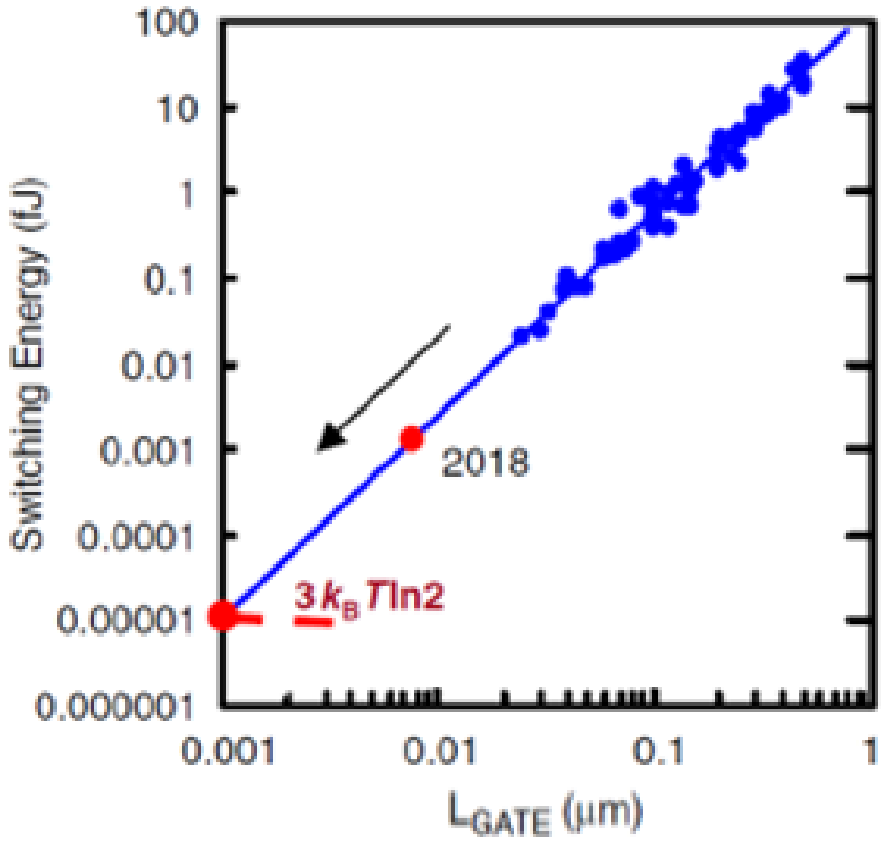
  -electron transport (*Nanowires, Tunnel FET* …)
  -spin (*SpinFET*…)
  -electromechanical properties (*NEMS*…)
  -combination with alternative materials: *Ge, III-V, Fe, Graphene*...

- **Ex : Memory**

  => alternative solutions with other state variables:
  => *PCM, RRAM, MRAM*…

Present switching Energy:

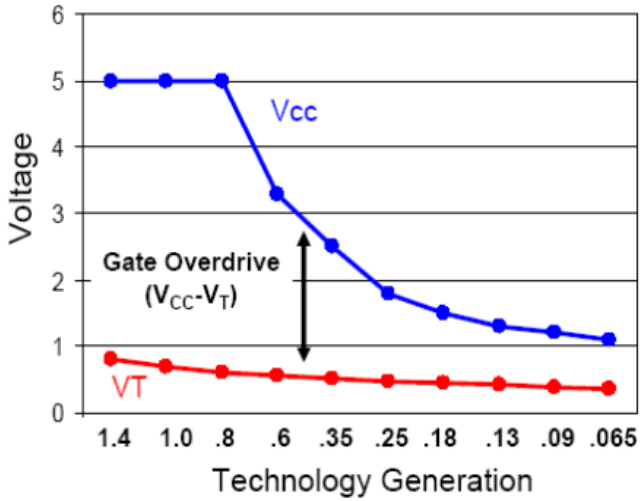
=> very far from kTln(2)



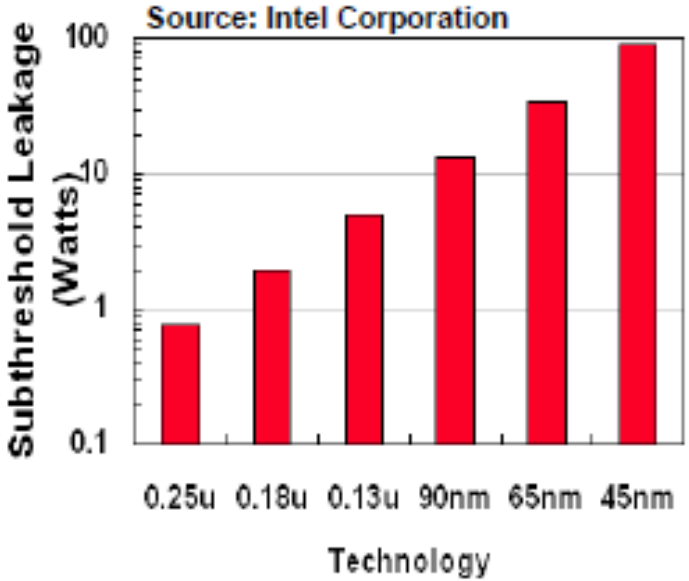
Practical cases:

Slowdown of Vdd scaling and increase of subthr. Leakage:

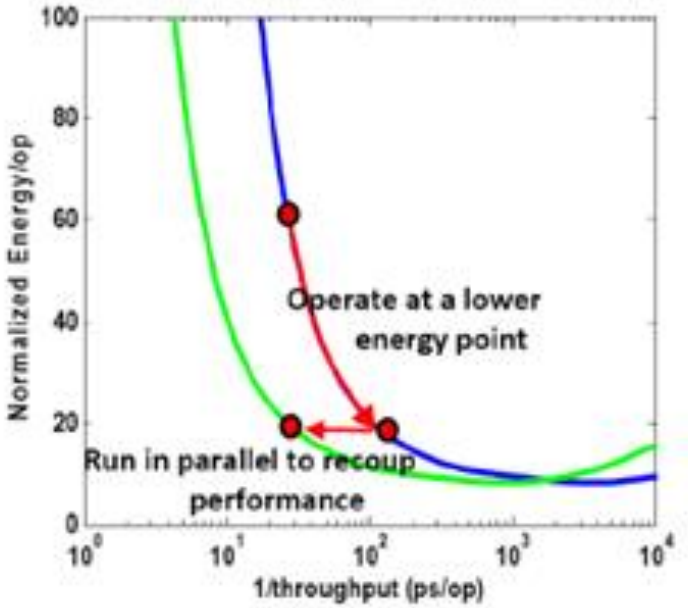
=> ↑ *of dynamic and static power consumption*



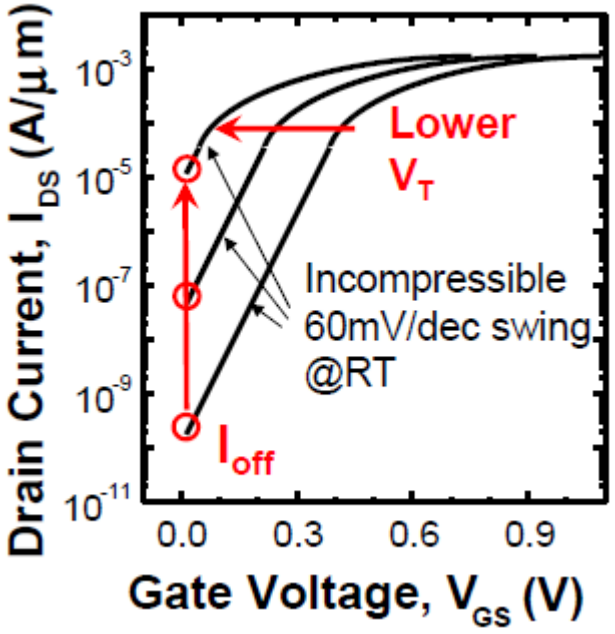
(P. Packan (Intel), 2007 IEDM Short Course)



Parallelism (multi-core) is a key technique to improve system performance under a power budget

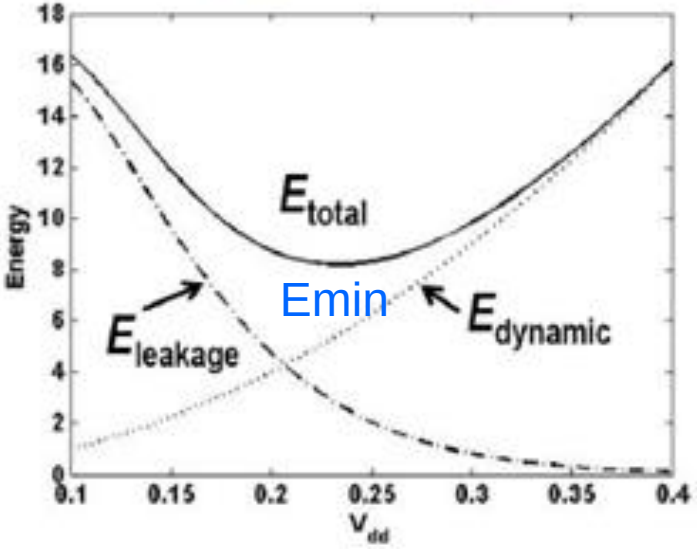


Power challenge due to subthreshold slope limit and lower limit in energy per operation



Reducing threshold voltage **by 60mV** increases the leakage current (power) **by ~10 times**

CMOS has a fundamental lower limit in energy per operation due to subthreshold leakage



Emin ~ C . S^2

Vddmin ~ S

(Hanson, IEEE TED 2008

Possible solutions for reducing sub. Swing

-Solutions for reducing S:

$$S = \frac{\partial V_g}{\partial(\log I_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_S}}_{m} \underbrace{\frac{\partial \psi_S}{\partial(\log I_D)}}_{n} = (1 + \frac{C_s}{C_{ins}}) \frac{kT}{q} \ln 10$$

m **less than 1** ***n*** **less than (kT/q)ln10**

⇒ Decrease of the transistor body factor **m**: **UTB/MG/NW/CNT/Graphene (m~1)** or **m<1**: **NC-FET, MEMS/NEMS …**

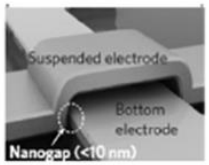
⇒ Reduction of **n**: modification of the **carrier injection** mechanisms (or **low T°**):

I.I., BTBT …

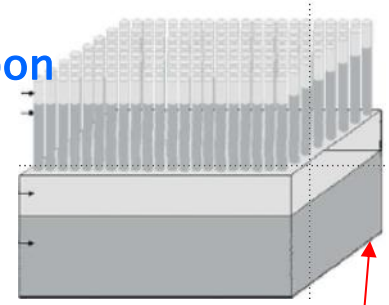
Nanoscale FET roadmap for low energy, scaling, high perf., new functionalities

… IC evolution …

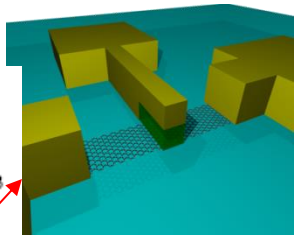
NEMS



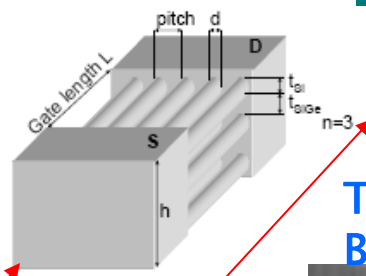
NW/Carbon-based MtM



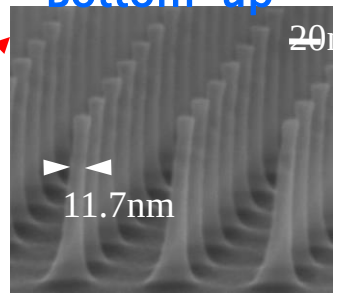
Graphene/2D-FET

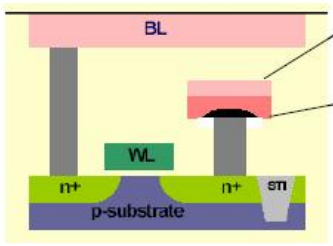


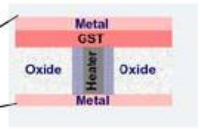
3D-NW

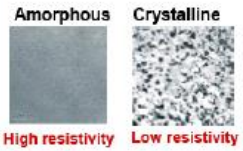


Top-down/ Bottom-up



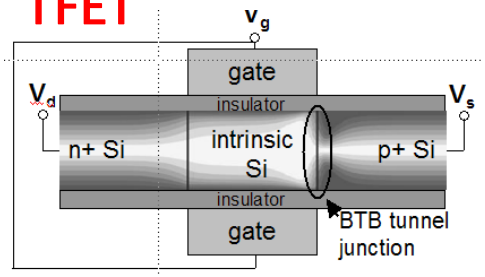


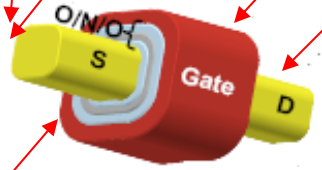




Non-charge/ PCRAM

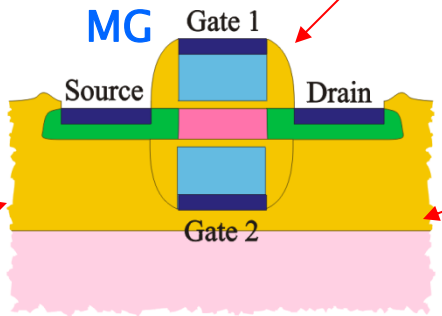
TFET

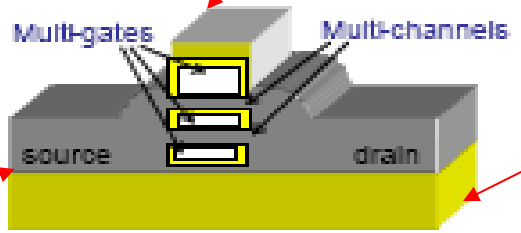




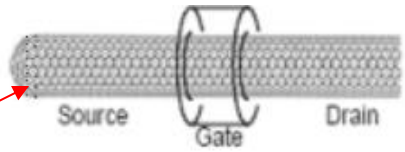
NW/NVM

MG



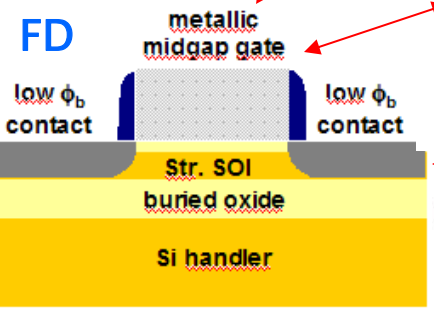


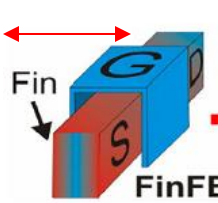
MC

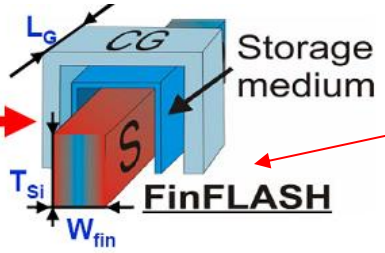


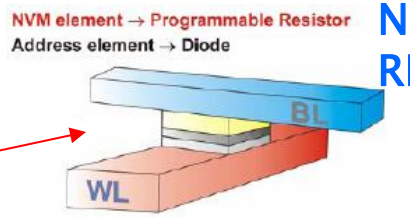
CNT

FD









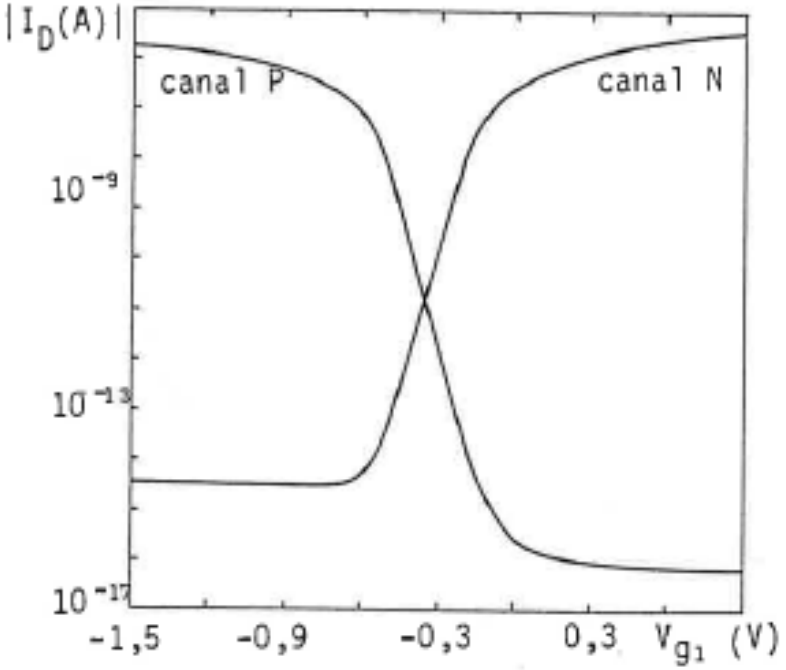
Non-charge/ RRAM

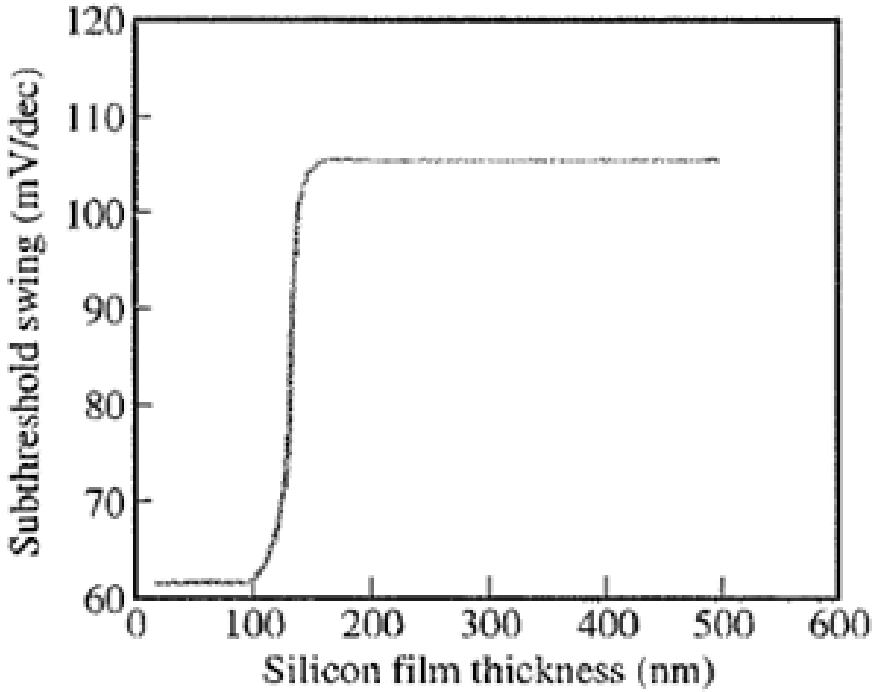
… IC evolution …

Subthreshold swing of FD SOI MOSFETs

⇒Down to 60mV/dec for UTB at 300K

*1st deep depleted SOI MOSFET, F. Balestra, ESSDERC'**1984** & SSE **1985** & PhD **1985,** JP. Colinge EDL **1986***





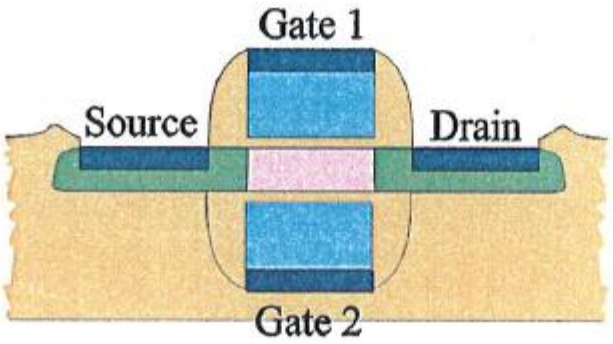
60 mV/dec numerical simulation (Balestra PhD'85)

60mV/dec experiment (Colinge EDL'86)

IMEP-LAHC

Multi-gate for very low power and HP:
Scaling (td, n), Power (S) & Performance (μ)

Very thin Si,
Ge or III-V film



High-k gate oxide
& metal stack

Double-
or multi-gate

Silicide Schottky
barriers

=> Fully Inverted MOSFET (Balestra EDL'**87**)

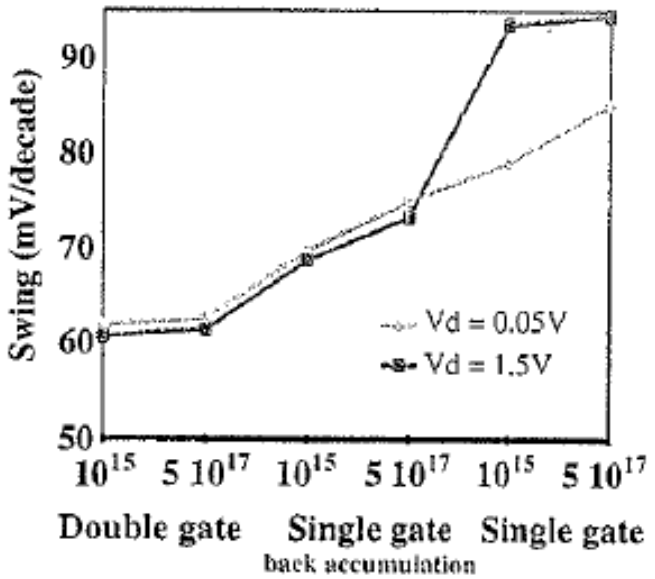
IMEP-LAHC

Subthreshold swing in double-gate SOI MOSFETs

E. Rauly, SSE vol. 43, 1999.

Numerical simulation of subthreshold swing for various types of extremely thin (tsi = 10 nm) SOI MOSFETs (Lg = 0.05 μm)

Single gate
(t_{ox1} = 3 nm and t_{ox2} = 0.38 μm),
double gate
($t_{ox1} = t_{ox2}$ = 3nm),
various dopings
(Na = 10^{15} cm^{-3} and Na = 5 10^{17} cm^{-3})

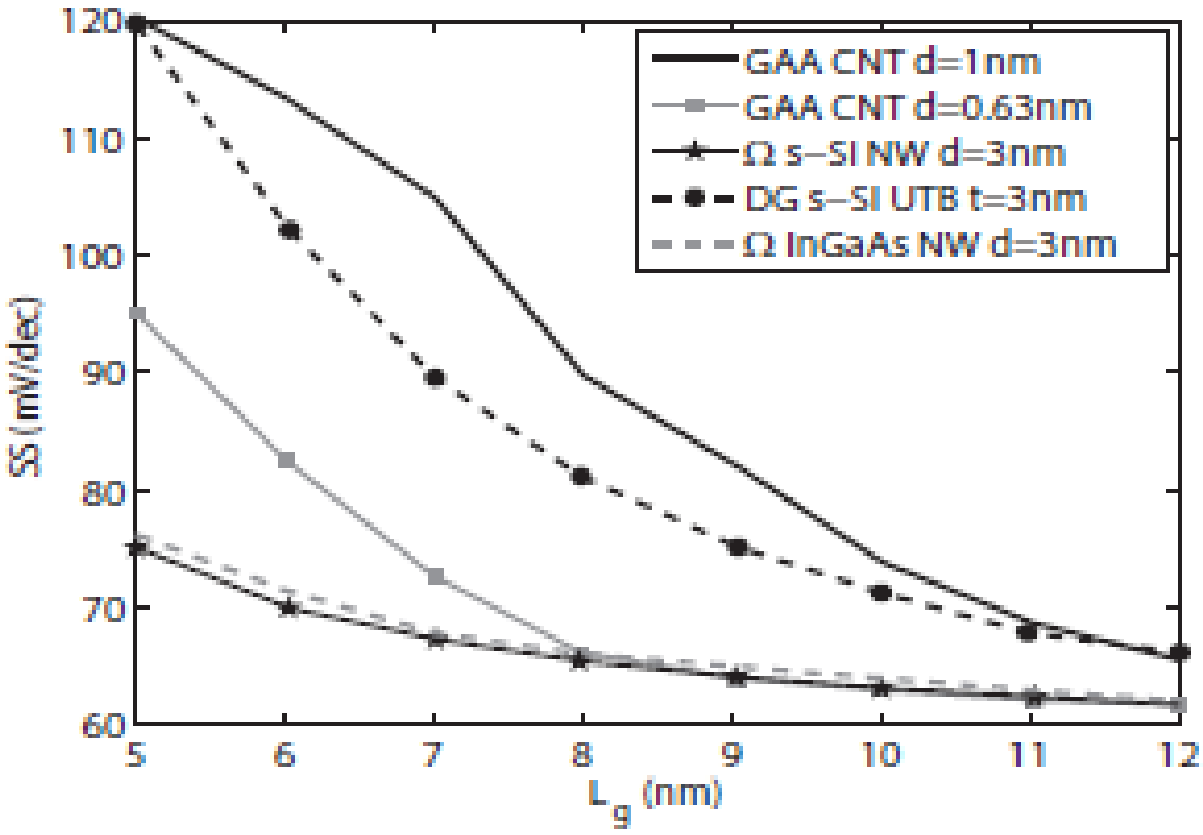


→ Improvement of the swing : - with reducing the Si film doping
- with a back gate accumulation (Vg2 = -40 V)
- for a double gate SOI MOSFET with volume inversion

Comparison of S for sub-10nm Lg for:

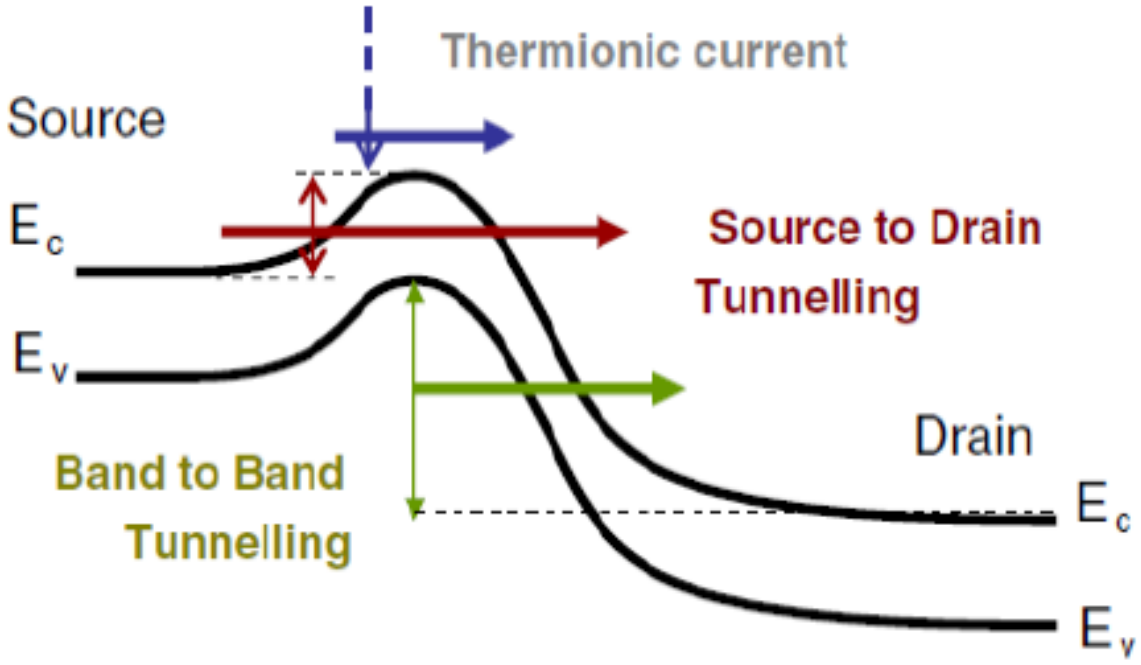
Ω-gate sSi and InGaAs NW, GAA CNT (≠d), DG sSi UTB

Very good S down to 5nm Lg, but…. >60mV/dec !



(simul. M. Luisier, IEDM11)

S/D and B to B Tunnelling



Solutions for reduction of S below 60mV/dec

-Strong reduction in Vdd and Emin possible using new physics/materials/devices with **sub-60mV/dec subthreshold swing** (*limit of MOSFETs at RT*):

⇒ **Energy filtering**: *Tunnel FET* (MOS- NW- CNT- or Graphene-based): BtB tunneling to filter energy distribution of electrons in the source (cuts off the high energy e/Boltzmann tail resp. for 60mV/dec): PB => Ion

⇒ **Internal voltage Step-up**: *Ferroelectric gate FET* (inducing a negative capacitance to ampify the change in channel potential induced by the gate): PB => long switching times

⇒ *TFET and FeFET* would greatly reduce energy dissip. in conventional and adiabatic logics

Reduction of S below 60mV/dec

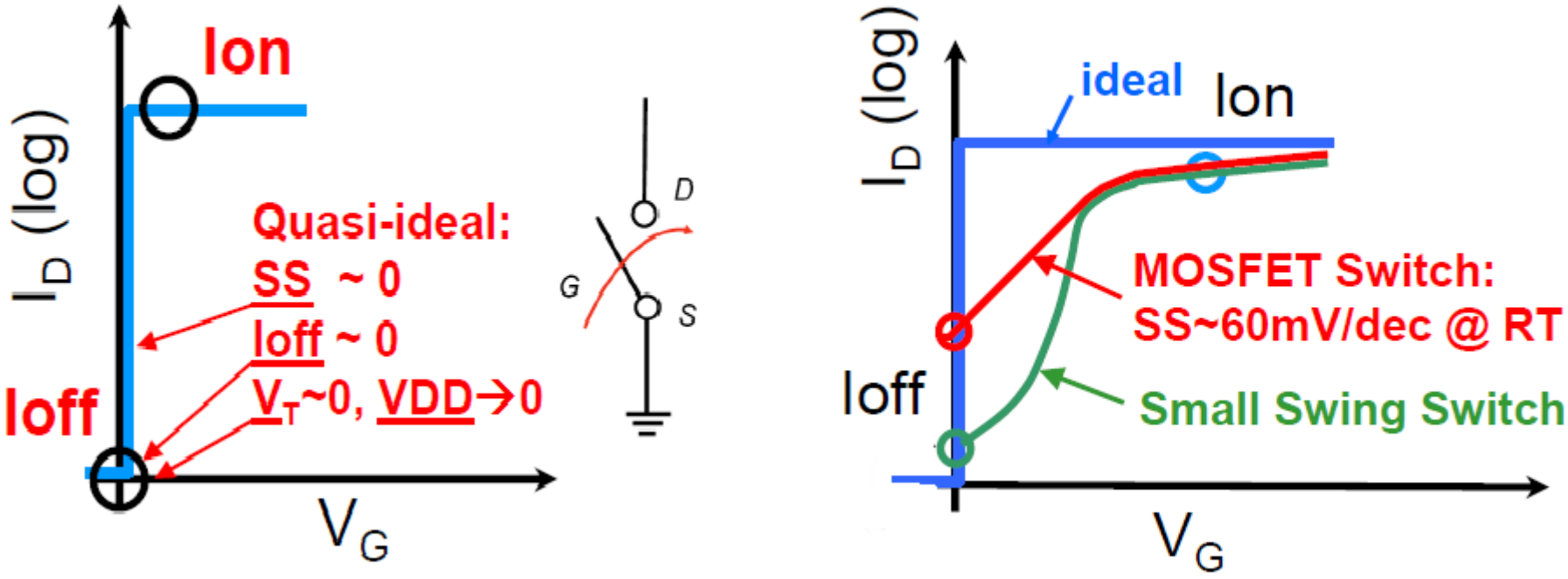
-Other alternatives:

*__MEM-NEMFET/relay__ (pb: voltage scaling, reliability)

*__I.I. Devices__ (pb: high V, reliability)

*Nanowire FETs with InGaAs-InAlAs **superlattice hetererostructure in the source** for filtering high energy electrons, leads to S=13mV/dec and Ion=4.5mA/μm at Vd=0.4V (simul.)

The quasi-ideal switch



- *Quasi-ideal binary switch:*

  - 2 stable states (off, on)
  - Ion: as high as possible
  - Ioff: as low as possible
  - abrupt swing (mV/decade)
  - very fast (<ns)

Small swing switch best parameters

To outperform CMOS:

-Ion: range of hundreds of μA

-S_{avg} far below 60mV/dec for at least 4-5 decades of Id

-Ion/Ioff > 10^5

-Vdd<0.5V

Reduction of S below 60mV/dec:
most promising => *TFETs*

-The most promising ones, **TFETs**, use **gate-controlled pin structures** with carriers tunneling through the barrier and not flowing over:

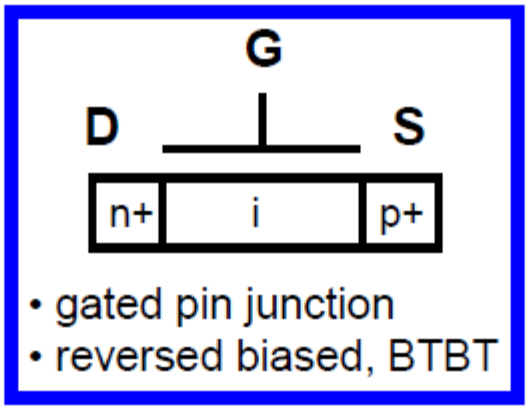
⇒ **Interband tunnelling** in heavily-doped p+n+ junction with a control of band bending with Vg and a reversed bias p-i-n

=> *Ambipolar effect* has to be suppressed by assymmetry in the doping level or profile, or the use of heterostructures

Tunnel FET

OFF-state

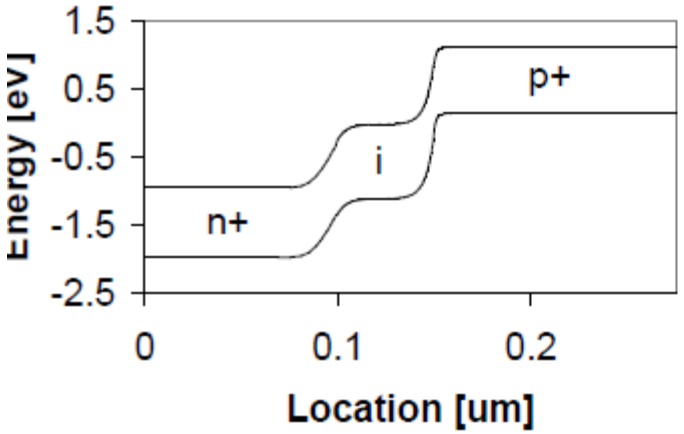
- V_d = positive
- V_g = 0
- **no current flows**

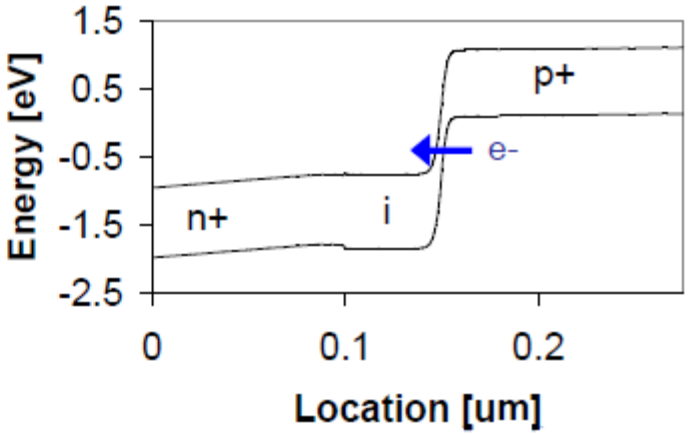


- gated pin junction
- reversed biased, BTBT

ON-state

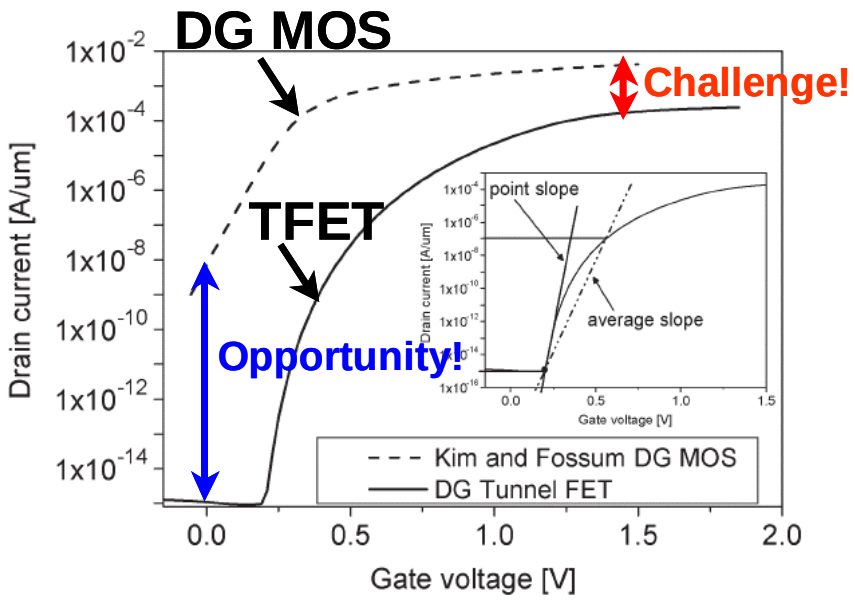
- V_d = positive
- V_g = positive
- **barrier thin, current flows**



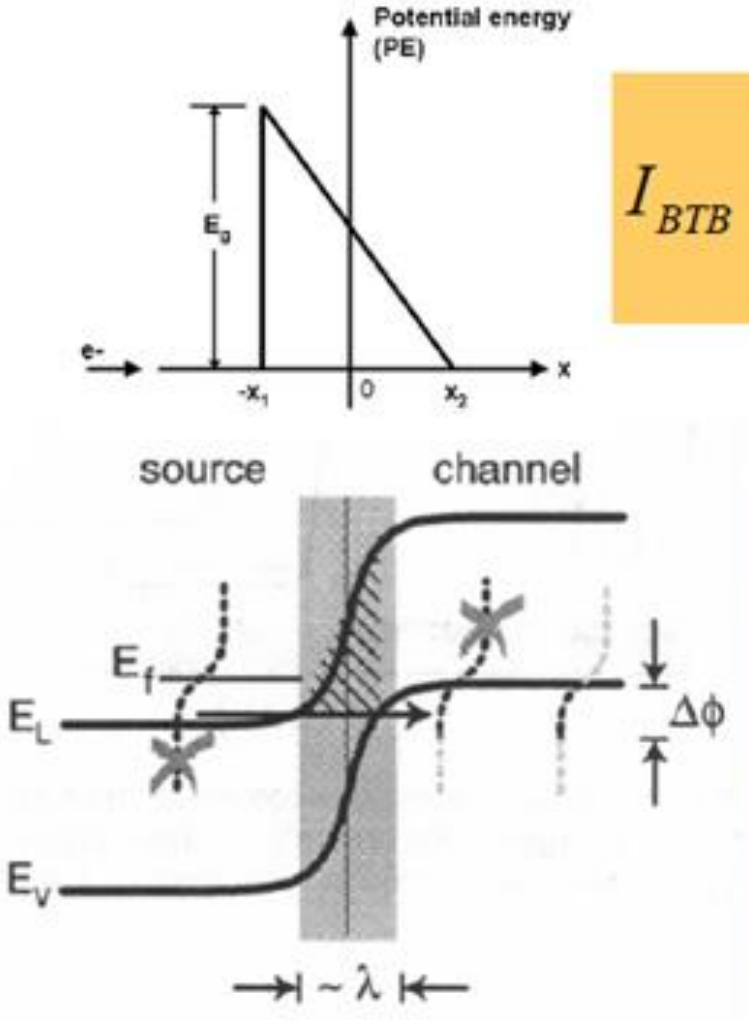


Tunnel FET

- **Opportunities**: reduce by decades standby power
- **Challenges** for Tunnel FETs:
  - bandgap engineering
  - *on-state* performance improvement needed
  - exploitation of innovative (nano)structures



Major parameter for BTBT: Transmission probability



$$I_{BTB} \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{1.5}}{3\eta(\Delta\Phi + E_g)}\right)$$

Parameter	Means of improvement
m^*	Small effective tunnel mass, SiGe, III-V, CNT
E_G	Source in SiGe, III-V heterostructures, strain CNT
λ	3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric

Optimisation of T_{WKB}:

-**Reduction of bandgap Eg, eff. mass m*, tunnel. length λ**
-Increase of ΔΦ

=> ↑ Ion, ↓ S for several decades of Id

•Eg, m*, ΔΦ : change of materials

•λ : change of device dimension, doping, gate capacitance, gate overlap on tunnel region, bandgap

=> Tox↓, high k, tsi↓, abrupt doping profile, high Source doping, MG, ≠ materials

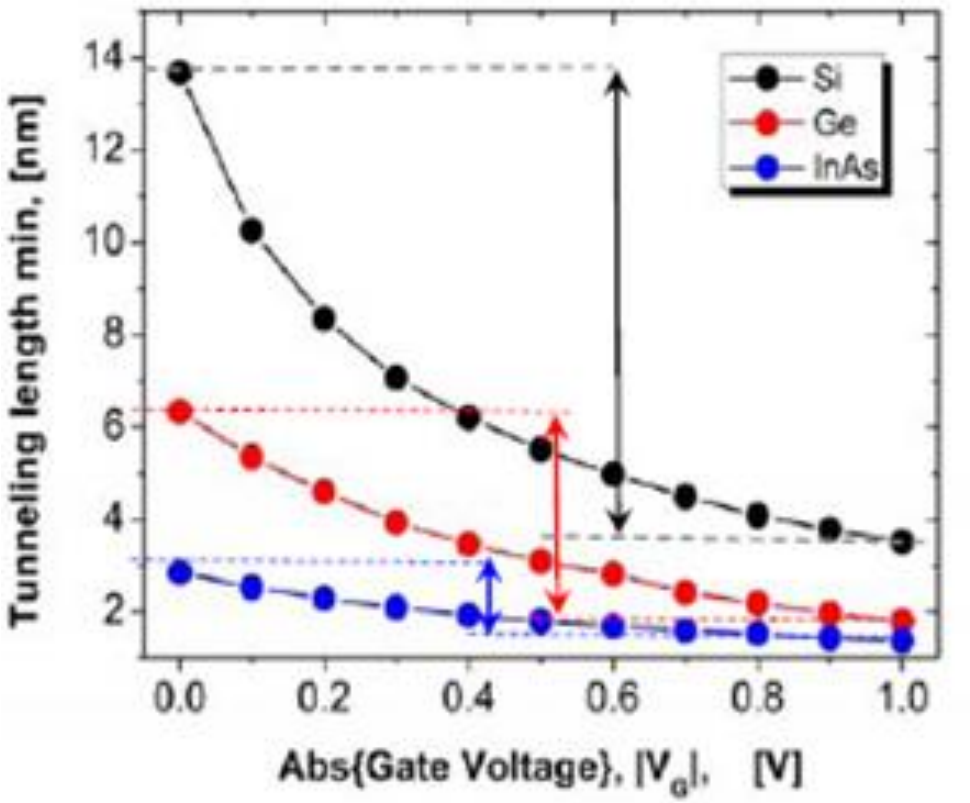
Optimisation of TFET:

-**Lg** has reduced effect compared with MOSFET

-**HeteroTFET**: small bangap at S and large bandgap at D

-**C-TFET** needed for logic circuits

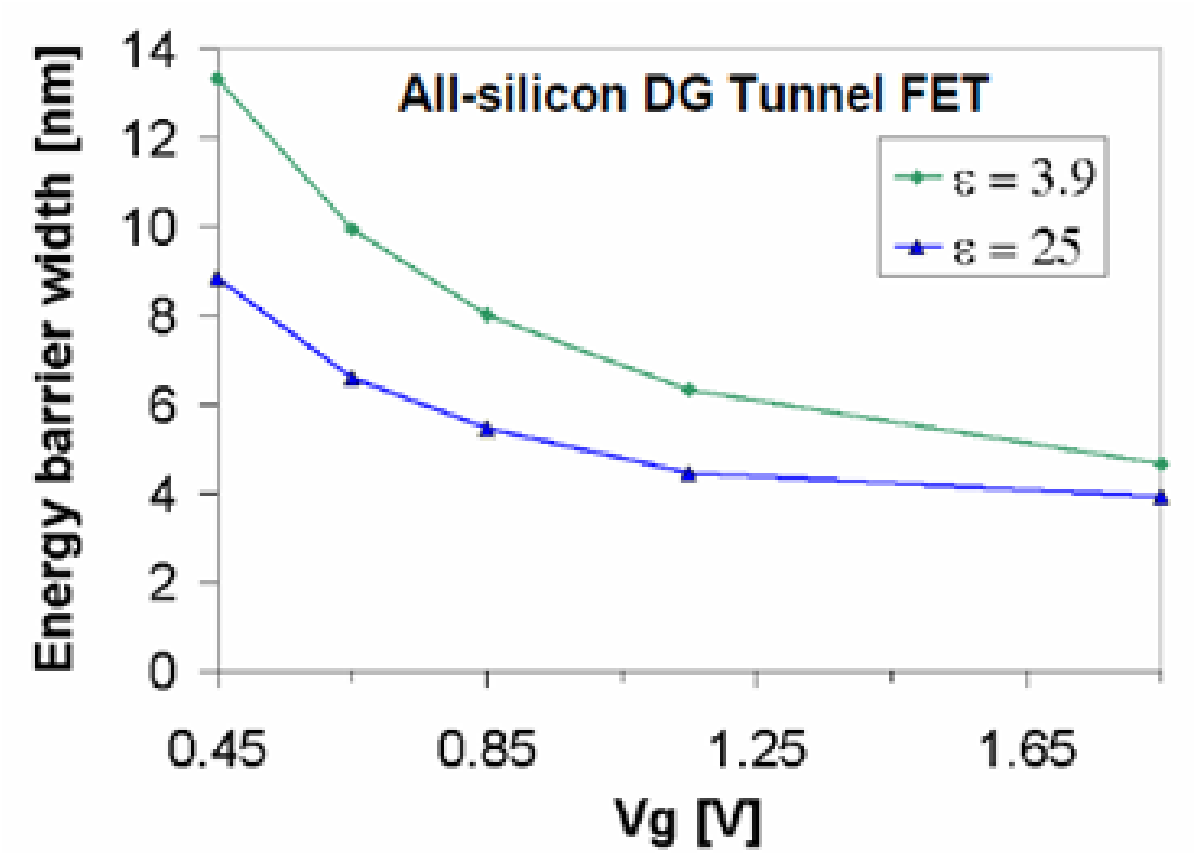
Impact of low bandgap Source on λ



(A. Ionescu, IEDM 2011)

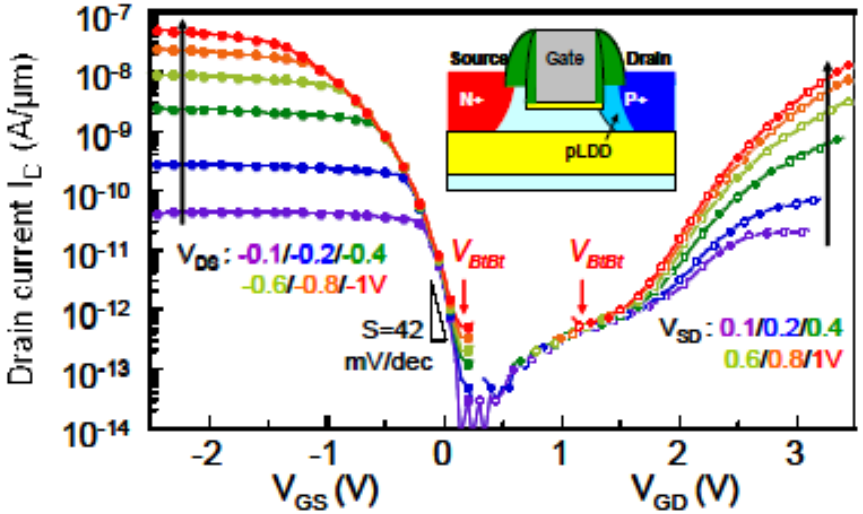
Barrier control: key for Tunnel FET operation:
Impact of high k dielectrics on λ

(A. Ionescu et al, ESSDERC 2009)

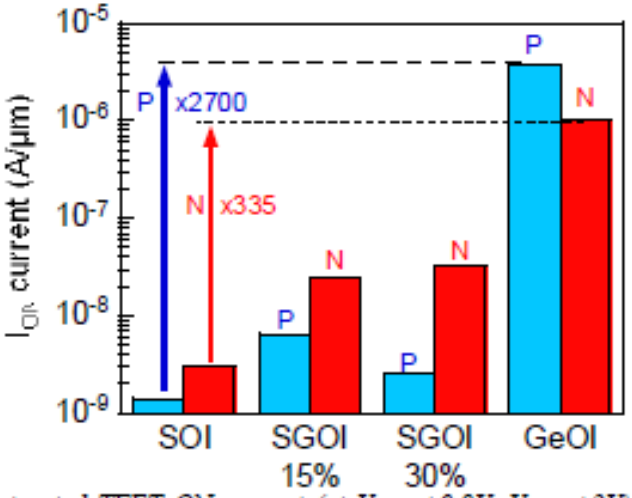


Tunnel FET on Si, SGOI, GOI

S=42mV/Dec, Ioff<0.1pA, *but Ion<0.1μA at Vd=1V*



$I_D(V_G)$ characteristics of a L_G=100nm SOI TFET in p (left) and n (right) channel operation modes (t_{Si}=20nm; P30: pLDD, 30nm 2nd spacers). Local subthreshold slope at low as 42mV/dec is measured. We define V_{BtBt} as the voltage at which band to band tunneling occurs.

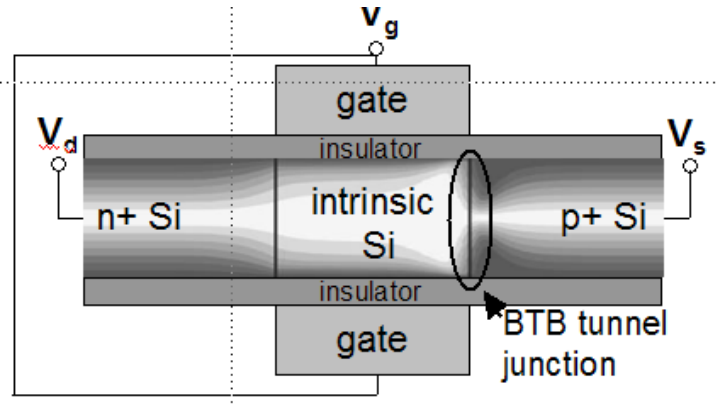


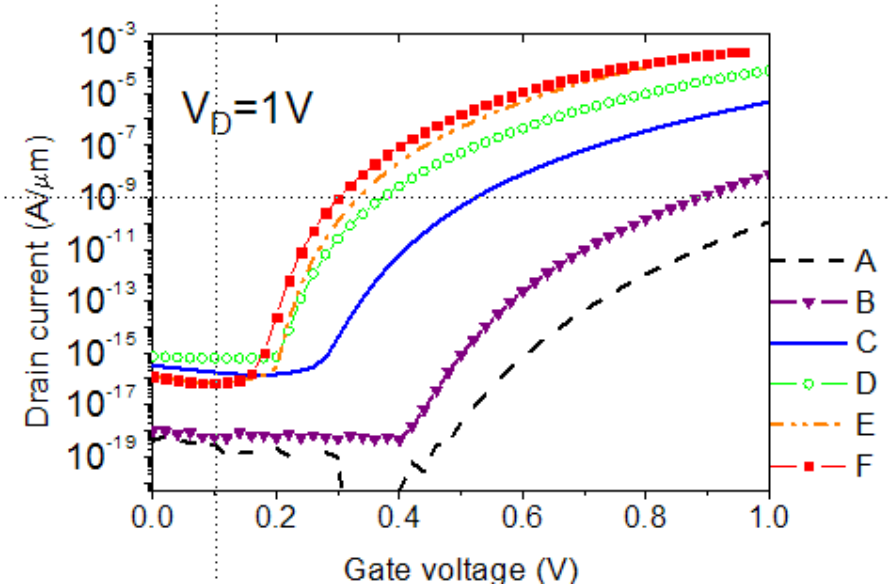
Extracted TFET ON current (at V_{DS}= ±0.8V, V_{GS}= ±2V) for 400nm gate length TFETs on $Si_{1-x}Ge_xOI$ (x_{Ge}= 0-15-30%, t_{SiGe}=20nm), and GeOI (T_{Ge}=60nm) substrates (in p & n modes).

(F. Mayer et al, IEDM 2008)

Technology boosters for TFETs:

High k, abrupt doping profile at tunnel junction, thinner body, high S doping, multi-gate, gate oxide aligned with i-region, shorter Lg/i-region





A) Single gate SOI; L=100nm, 3nm SiO_2

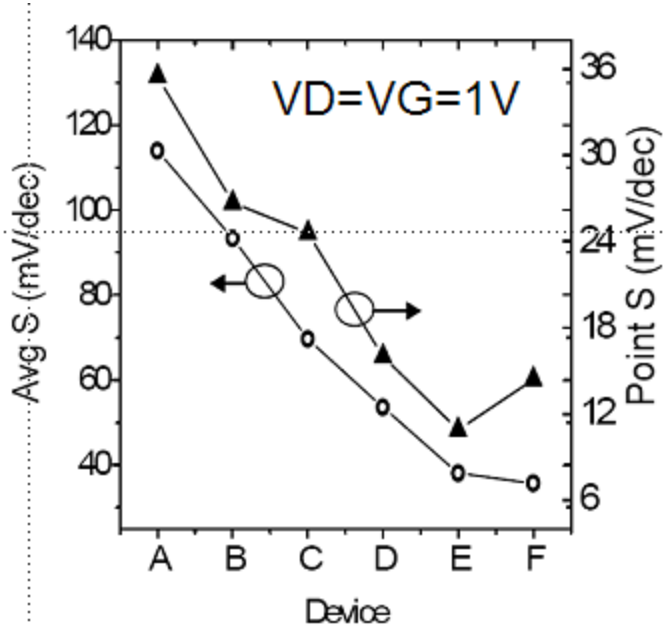
B) stress = 4 GPa at source junction

C) high-K gate dielectric

D) double gate

E) oxide aligned to i-region

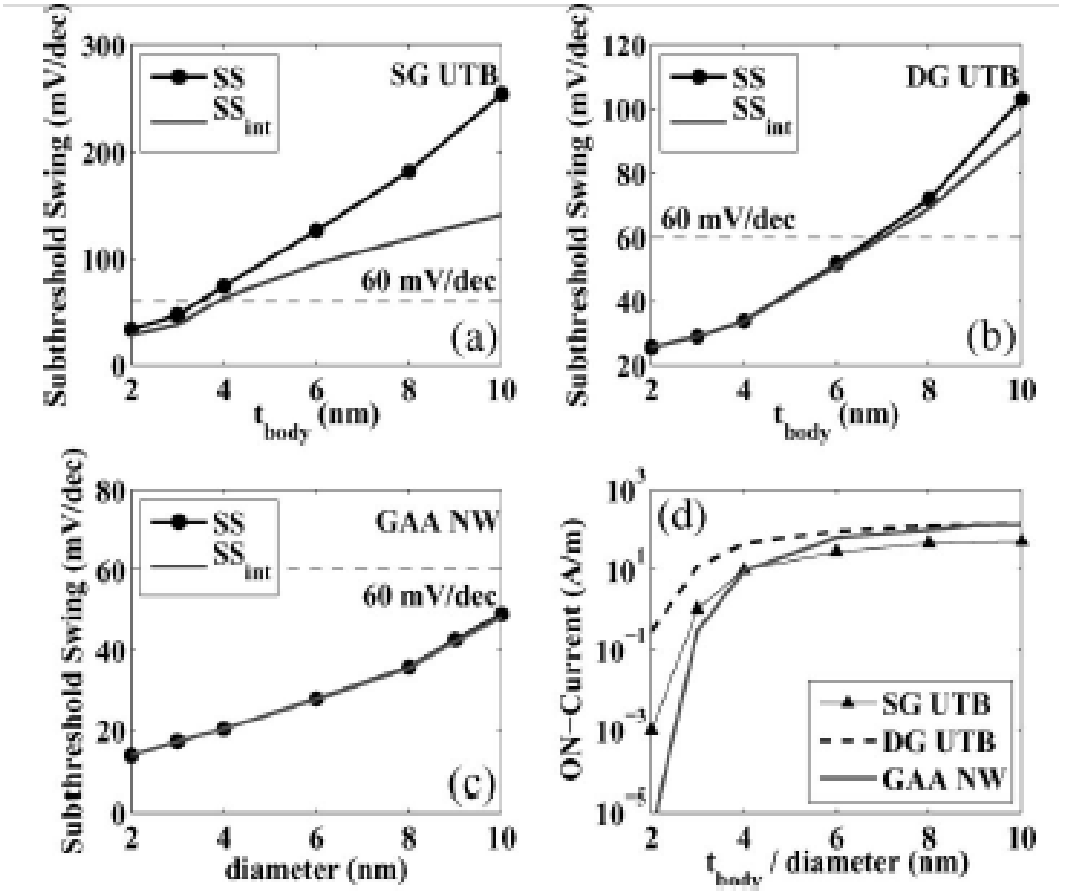
F) L=30nm



K. Boucart et al, ESSDERC'2009 & IEEE-EDL'2009 (simul.)

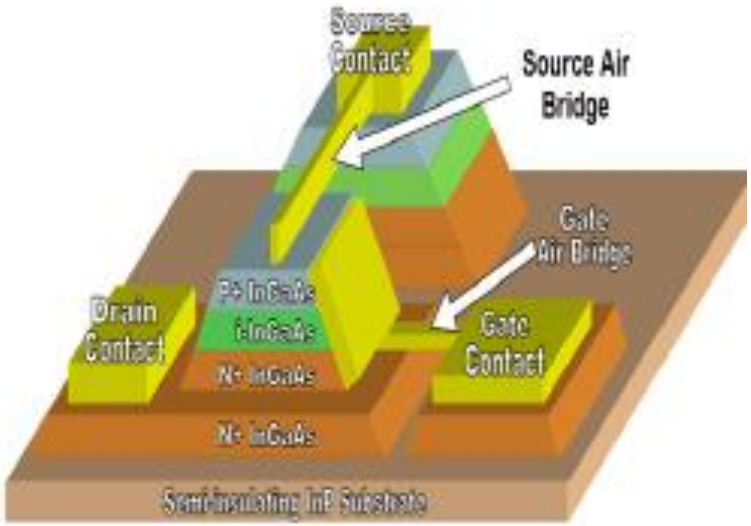
III-V channel TFETs

- * **InAs TFETs (SG, DG, GAA NW):** small bandgap and electron-hole effective masses inducing BTBT (Vg=Vd=0.2V) (*M. Luisier EDL 2009, Simul.)* :

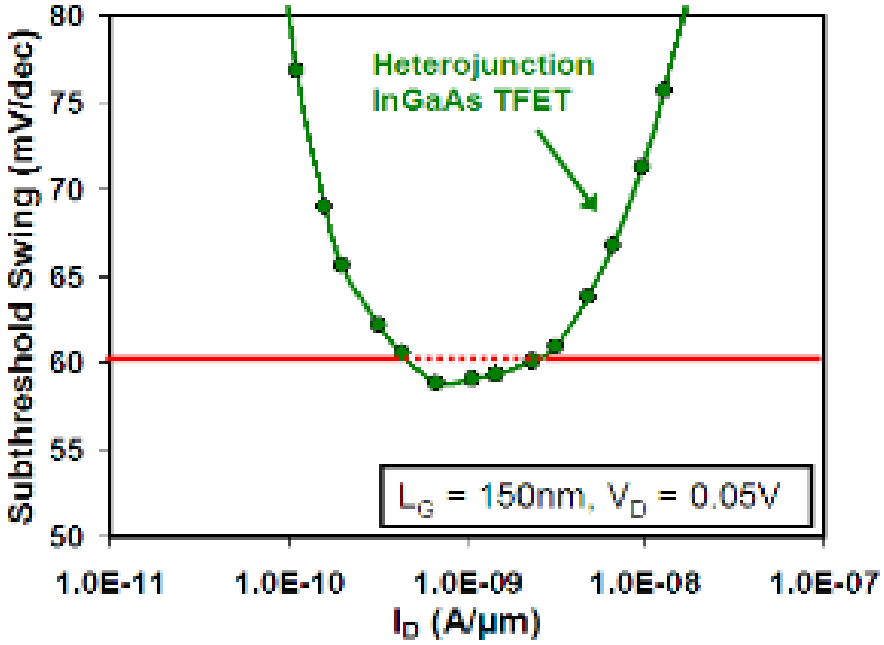


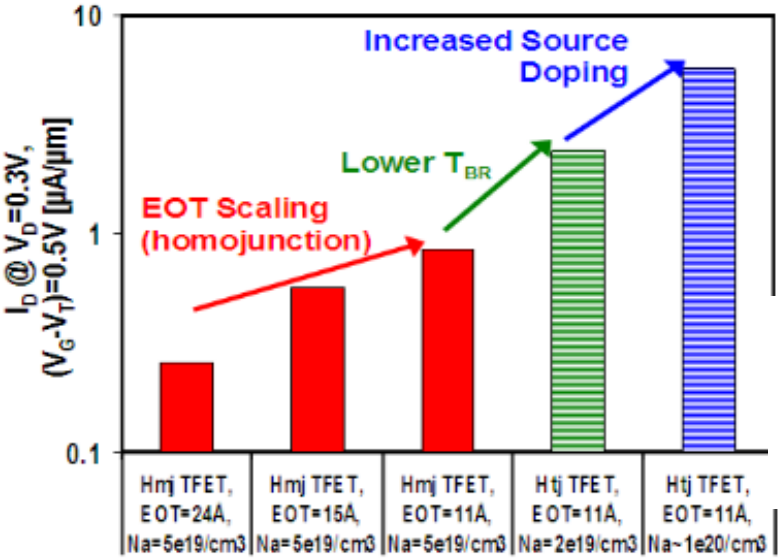
InGaAs Heterojunction TFET:

Id↑x20, **S<60**mV/dec with: EOT↓, ↑ S doping, lower tunnel barrier with heteroj.



G. Dewey
IEDM 2011

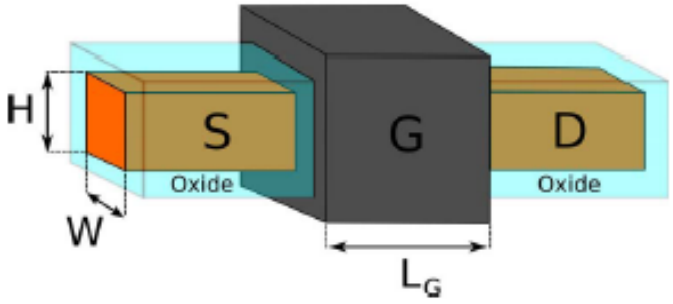




Drain current (I_D) at V_D = 0.3V and V_G-V_T=0.5V

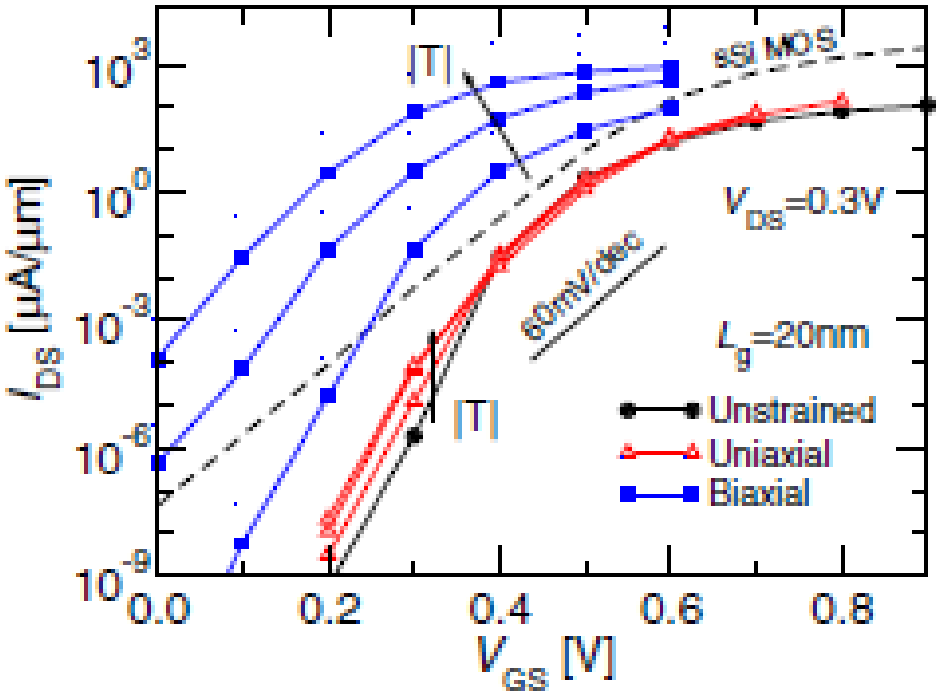
A combination of scaling the EOT in the homojunction (H_{mj})TFET (~3X I_D), lowering the tunnel barrier with heterojunction (H_{tj}) TFET (~3X I_D), and increasing the source doping in the H_{tj} TFET (~2X I_D) result in >20X combined improvement in the I_D of the III-V TFET

Strain InAs NW TFETs

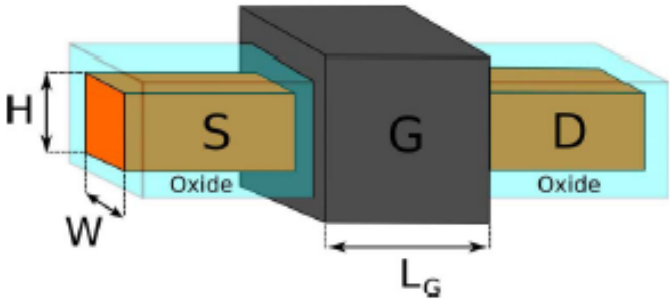


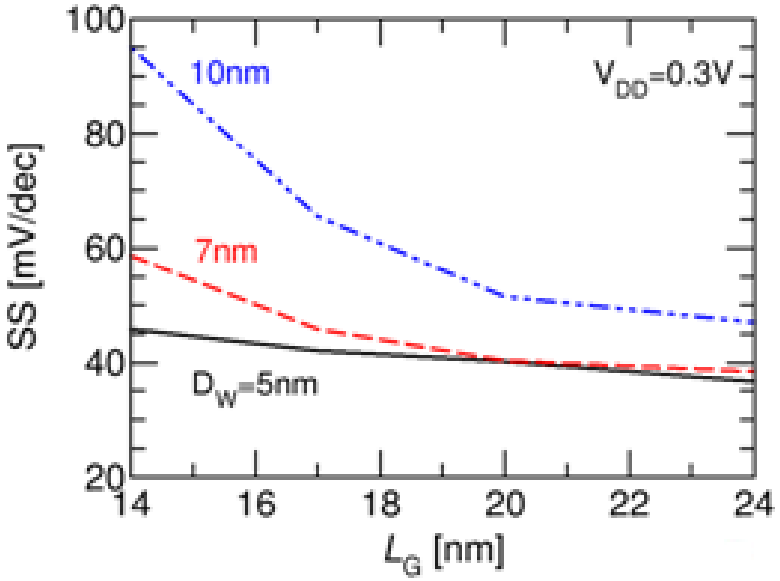
L_g [nm]	$W=H$ [nm]	L_{SD} [nm]	T_{ox} [nm]	N_S [cm^{-3}]	N_D [cm^{-3}]	Transport direction x
20	5	20	1	$5\cdot10^{19}$	10^{18}	[100]

F. Conzatti
IEDM 2011
(3D quantum transport simulation)



InAs NW TFETs

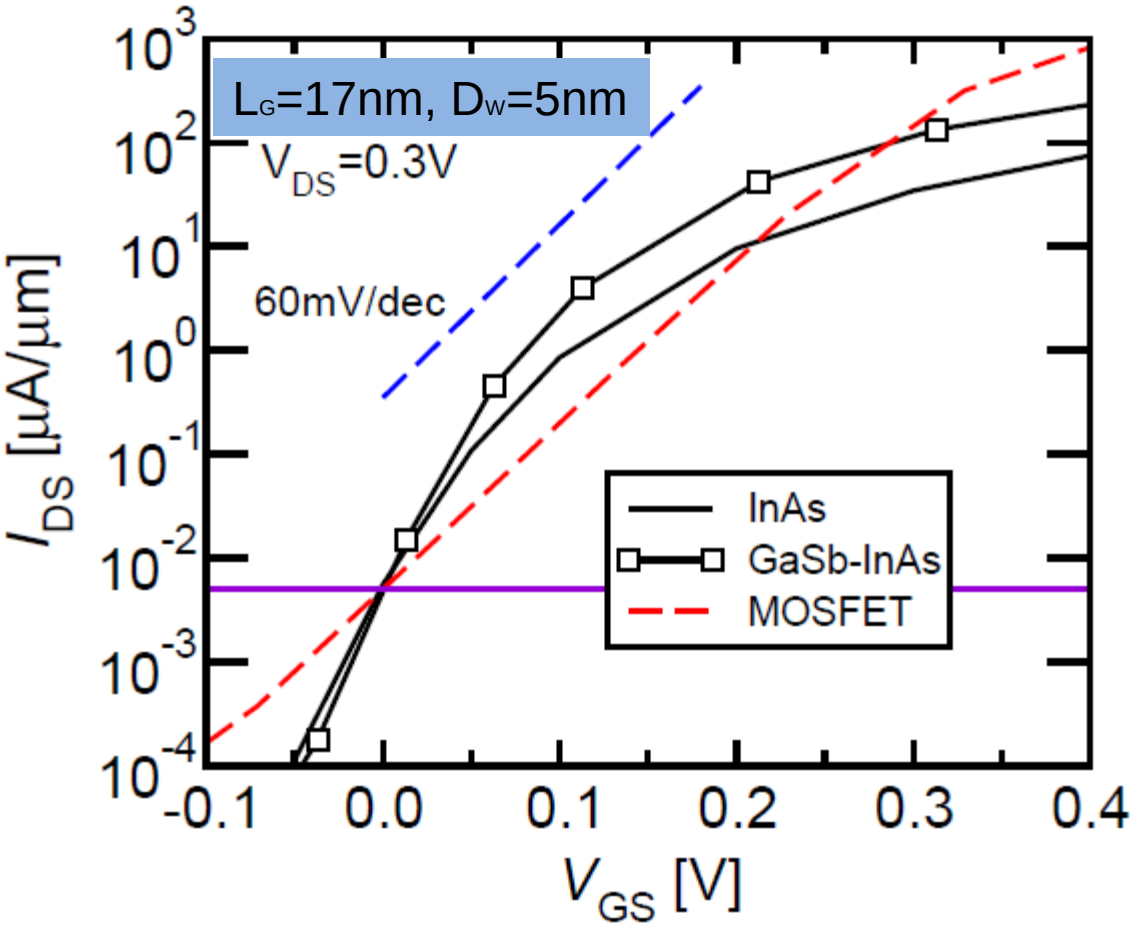




Subthreshold swing vs gate length for GAA InAs Nanowire TFETs for various wire diameters obtained by quantum simulation

F. Conzatti
IEDM 2011
(3D quantum transport simulation)

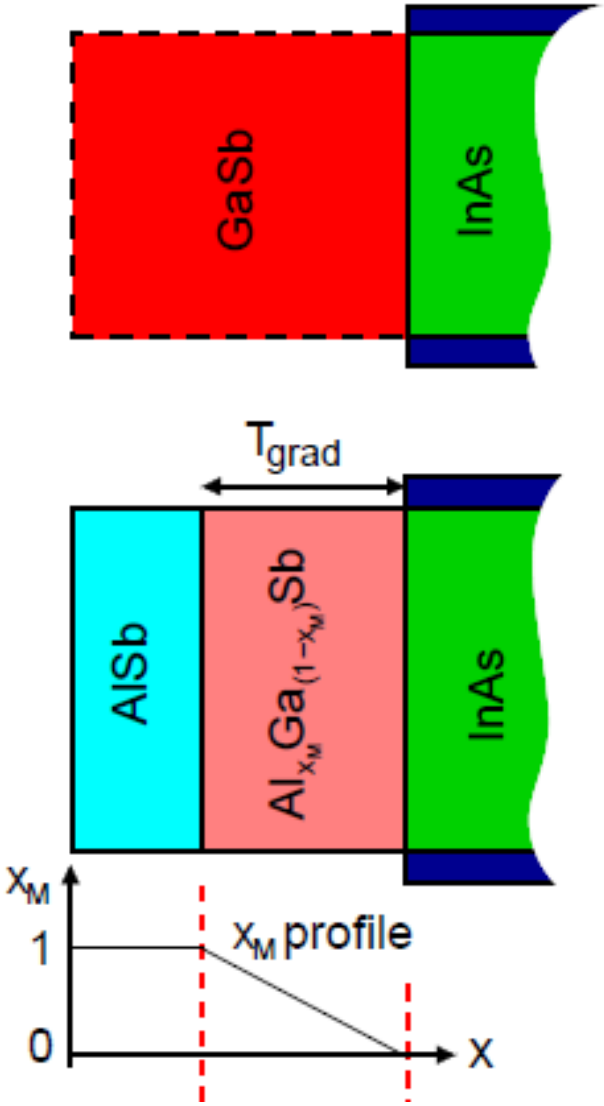
Comparison of **GaSb-InAs H-TFET** with **InAs TFET** and **InAs NW MOSFET**



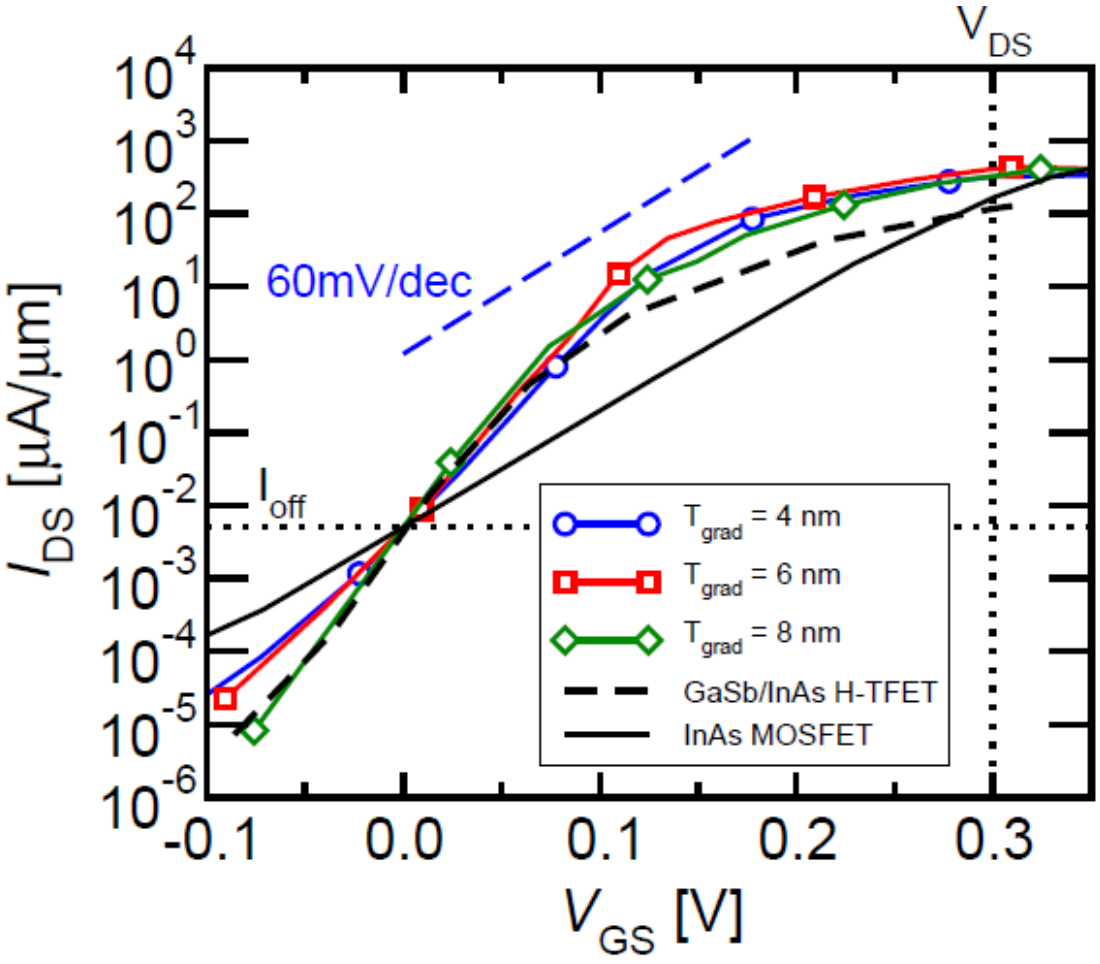
S. Brocard IEDM 2013 (3D quantum transport simulation)

=> Near-broken bandgap configuration at the source-channel interface, thus increasing I_{DS} significantly

H-GaSb/InAs TFET compared with **graded $Al_{xm}Ga_{(1-xm)}Sb$ source/InAs** NW H-TFETs



$Al_{xm}Ga_{(1-xm)}Sb/InAs$ H-TFETs
with 3 graded options



S. Brocard EDL 2014 (3D quantum transport simulation)

Substantial ↑ of Id, similar S as H-GaSb/InAs TFET

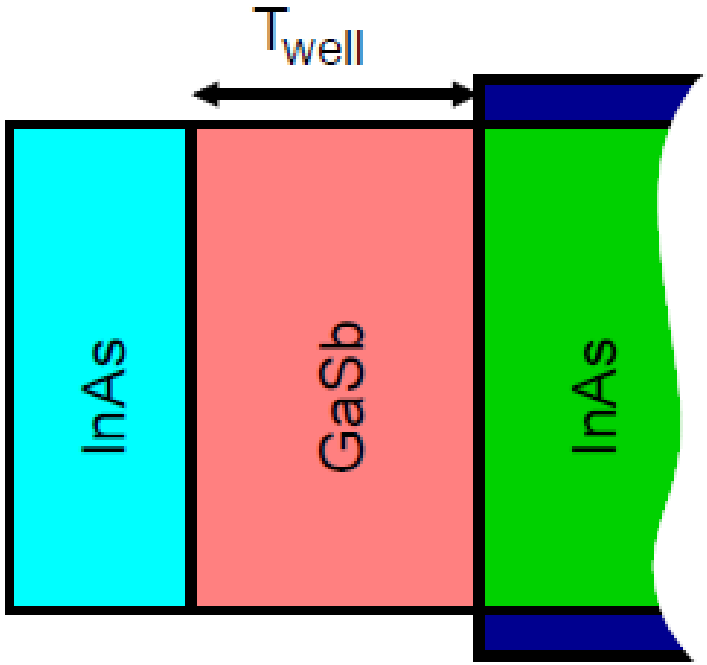
Ion *≈ Transmission x Fermi-Dirac occupation function f*

IMEP-LAHC

InAs-GaSb-InAs **Qantum Well** NW TFET

S: p-doped InAs + thin GaSb undoped

C: undoped InAs / **D**: n-doped InAs

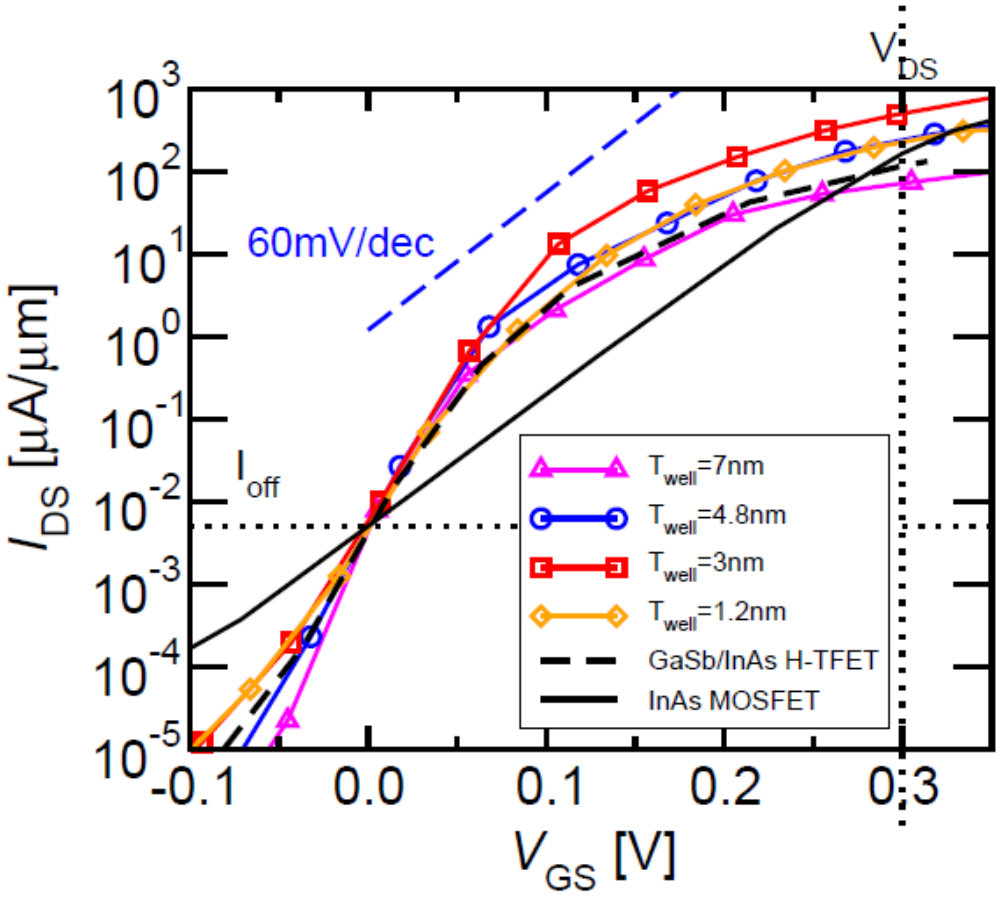


⇒ Strong concentration of **DOS at the edge between S and channel**

⇒ **Penetration of the electronic wave function** in the channel region

⇒ **Boost the band-to-band** current

InAs-GaSb-InAs **Qantum Well** TFET **vs Twell**

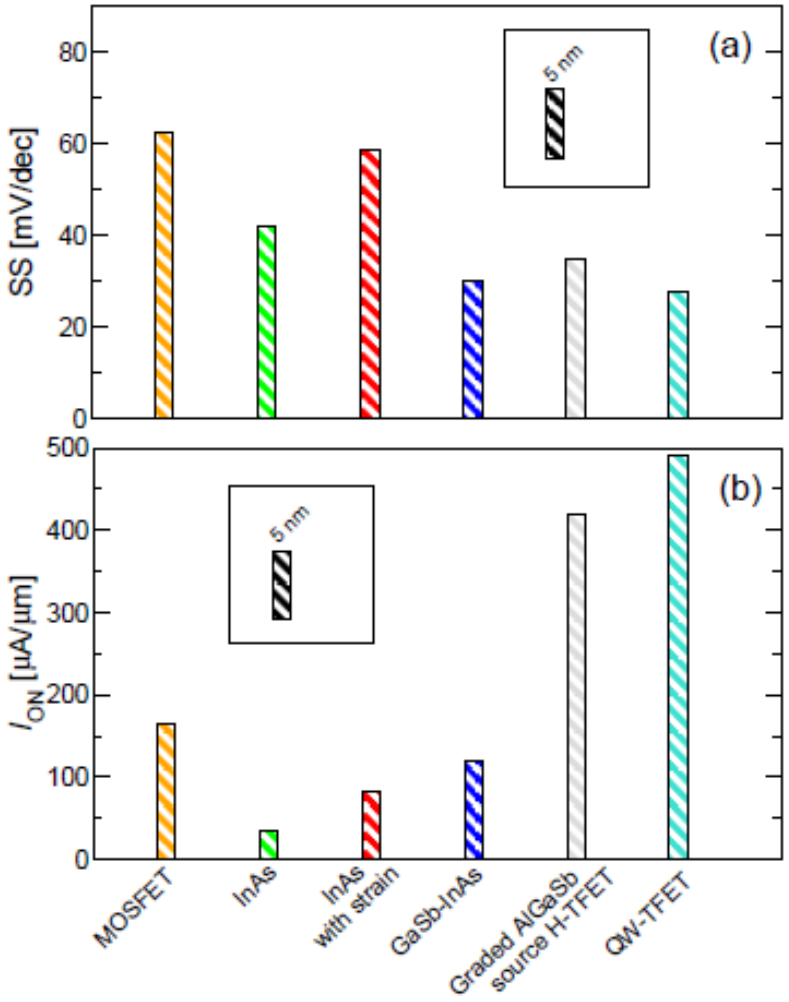


M. Pala
J. Elec. Dev. Soc., 2014.

Improvement of QW TFET / reference H-TFET => **optimum for Twell=3nm**

IMEP-LAHC

Comparison of all III-V TFET architectures



⇒ **QW-TFET best performance (InAs-GaSb-InAs Qantum Well)**

-Graded source H-TFET with Tgrad=5nm

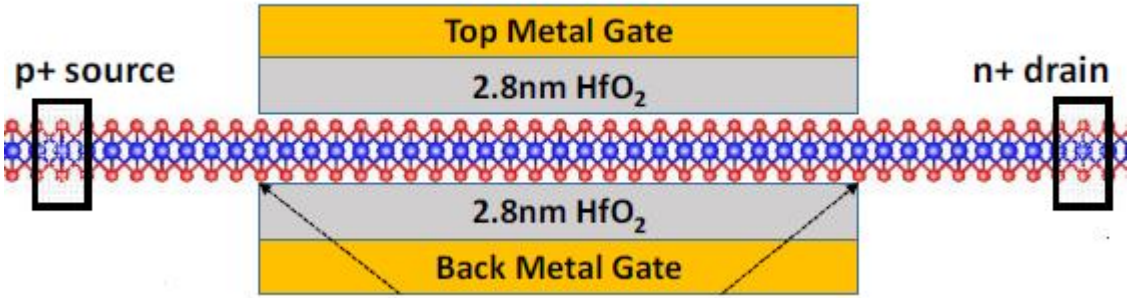
-Quantum well TFET with Twell =3nm

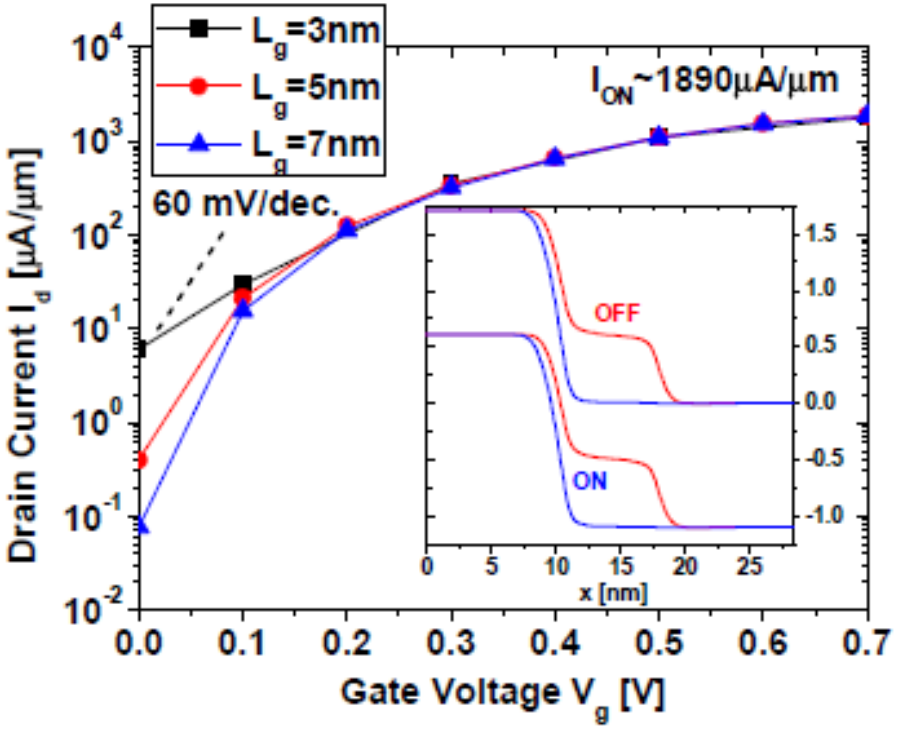
Dw=5nm, Lg=17nm, Ion at Ioff=5nA/µm

IMEP-LAHC

2D/WTe2 TFET

(Ab-initio quantum simulation, *X.-W. Jiang - IEDM'15*)





Best results for TMD layers obtained with **WTe2 TFET** for HP and LOP applications

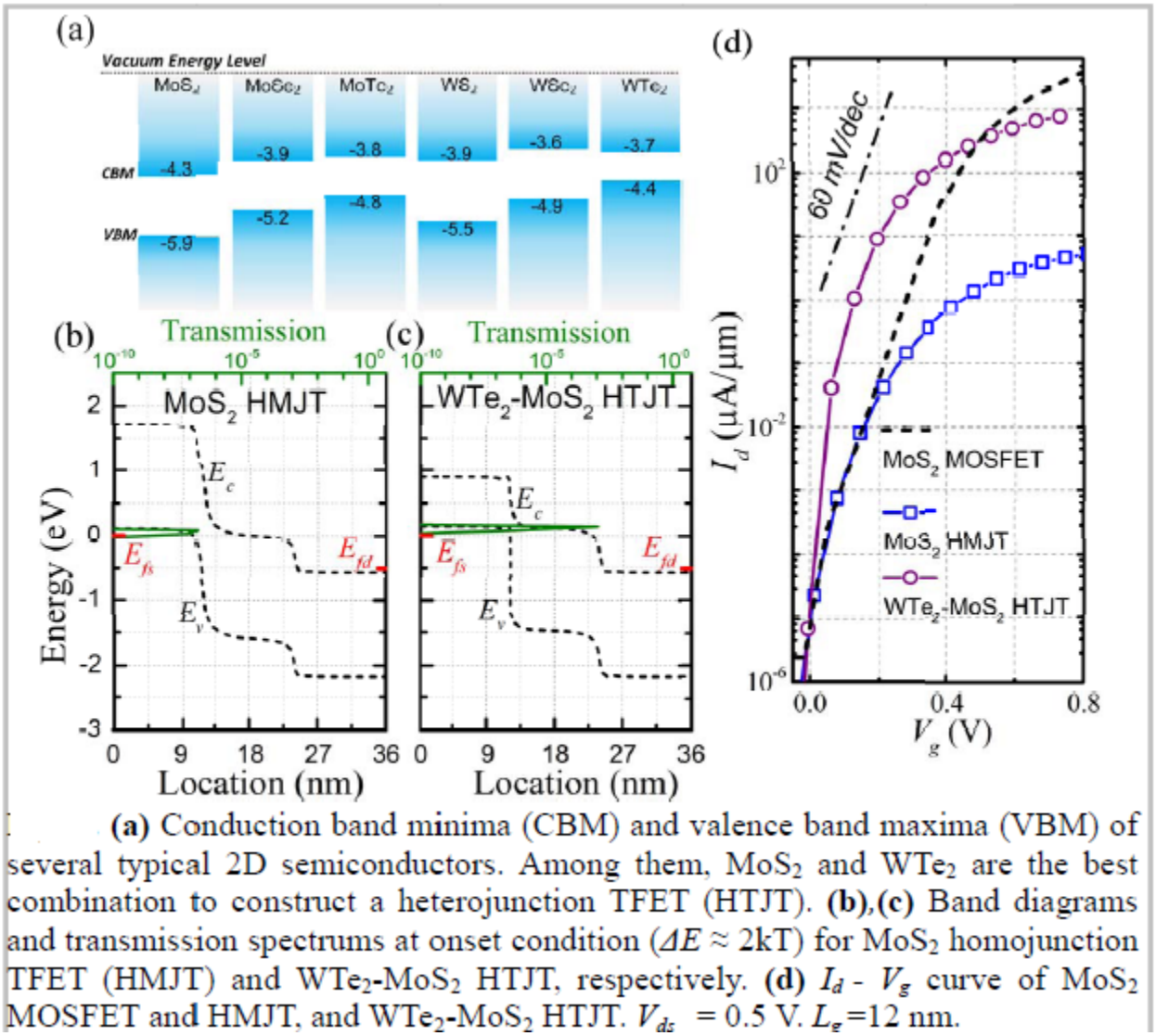
Vd=0.5V, S/D doping $10^{13}cm^{-2}$

Performance for Lg=7nm close to ITRS HP 2024 requirement

Ioff degradation for Lg<5nm

Comparison of Homojunction and heterojunction 2D TFET

(NEGF quantum simulation, *W. Cao - IEDM'15*)

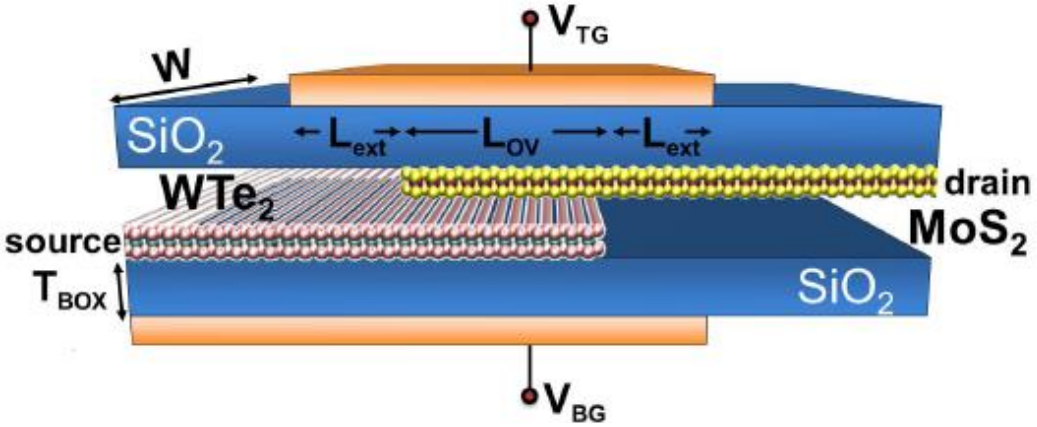


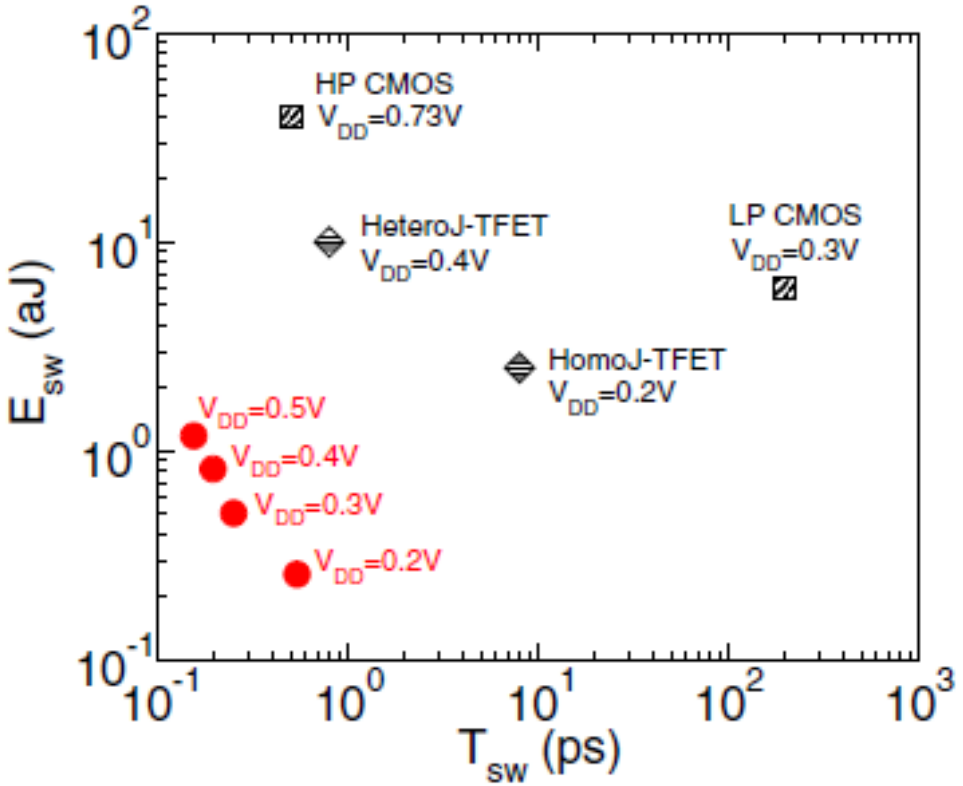
(a) Conduction band minima (CBM) and valence band maxima (VBM) of several typical 2D semiconductors. Among them, MoS_2 and WTe_2 are the best combination to construct a heterojunction TFET (HTJT). **(b),(c)** Band diagrams and transmission spectrums at onset condition ($\Delta E \approx 2kT$) for MoS_2 homojunction TFET (HMJT) and WTe_2-MoS_2 HTJT, respectively. **(d)** I_d - V_g curve of MoS_2 MOSFET and HMJT, and WTe_2-MoS_2 HTJT. V_{ds} = 0.5 V. L_g=12 nm.

Best results for
Heterojunction
WTe2-MoS2 TFET

2D (MoS2-WTe2) TFET

(Quantum simulation, *J. Cao- IEDM'15*)



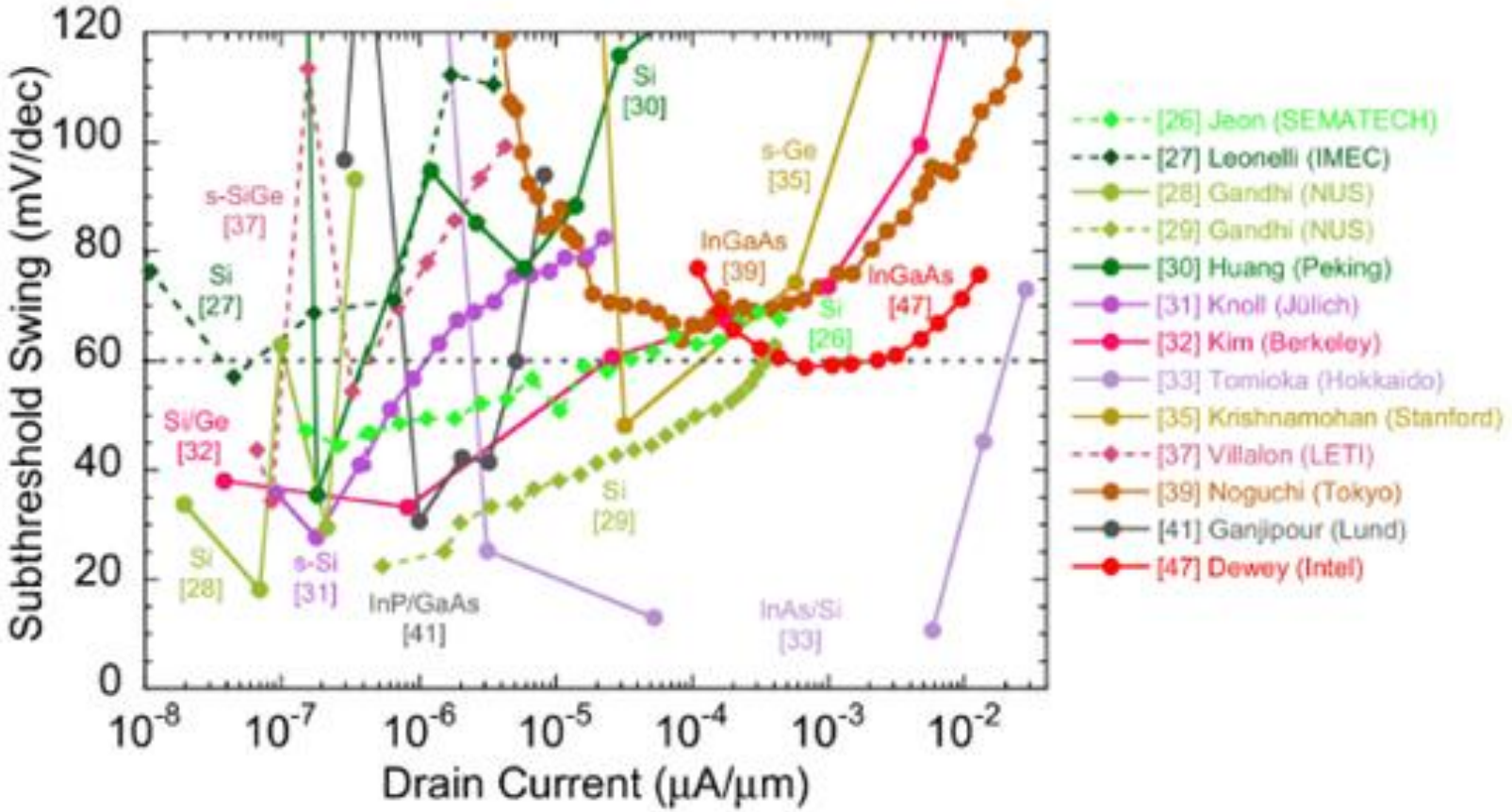


Intrinsic switching energy vs Switching time for various devices : CMOS, TFET (InAs and InAs/GaSb) and **2D TFET MoS2-WTe2** (**best results**)

Front and back SiO2, 0.35nm gap with ϵ=1, chemically doped MoS2 ($4.10^{12}cm^{-2}$) and electrostatically doped WTe2 with Vbg

Comparison TFET experimental results

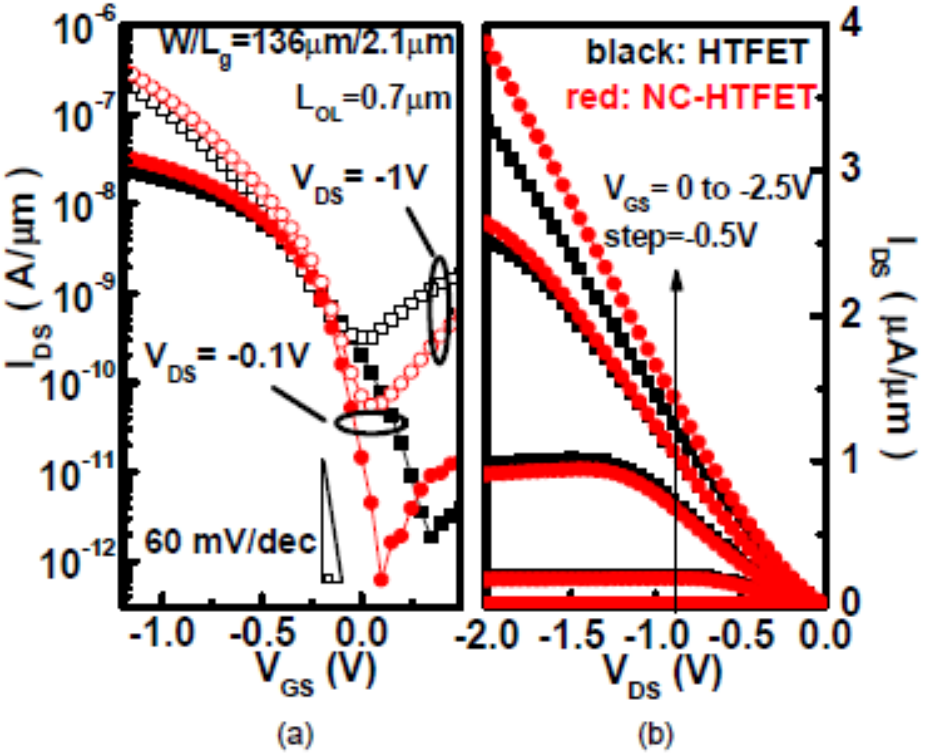
H. Lu, J. Electr. Dev.Soc. 2014



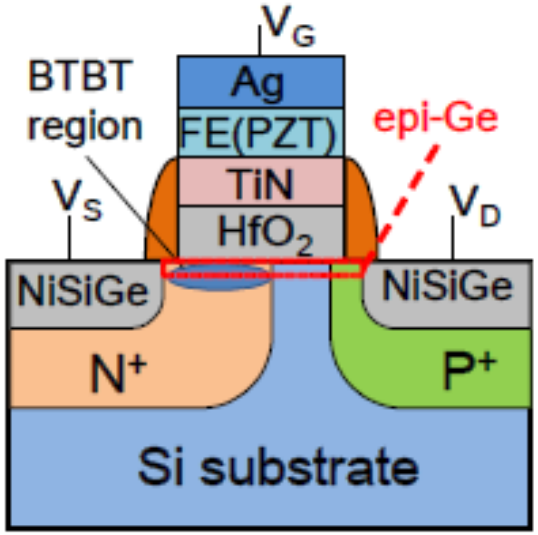
⇒ S < 60 mV/dec for Id < 10 nA/μm

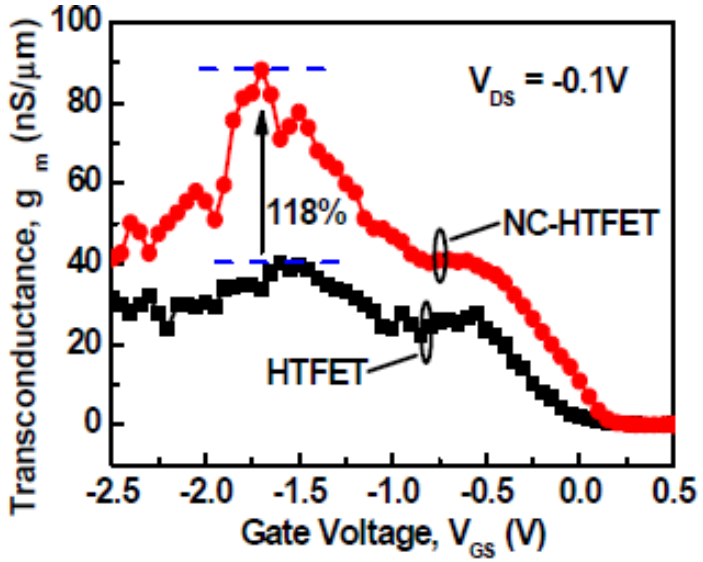
IMEP-LAHC

TFET-FeFET



(a) Transfer characteristic (b) Output characteristic of NC-HTFET. The subthreshold swing is improved significantly with NC. The current of NC-HTFET shows the enhancement with larger V_{GS}. Note that both HTFET and NC-HTFET are the same devices for comparison.



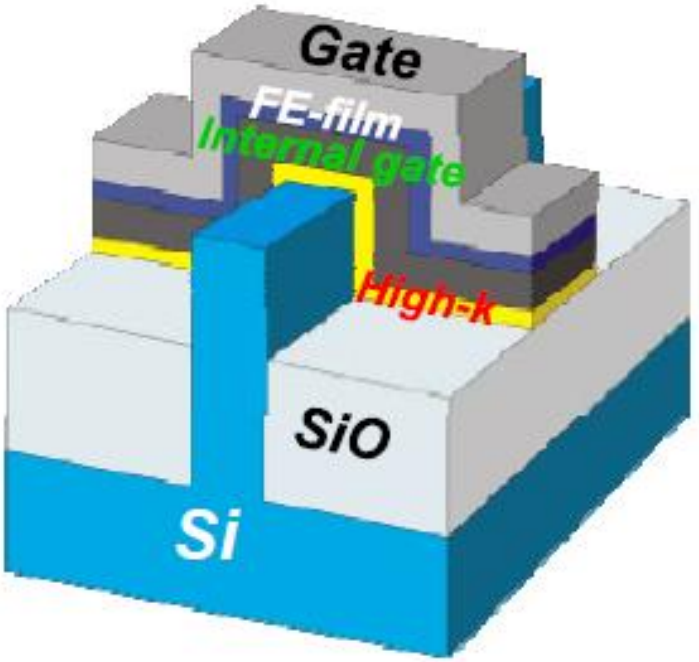


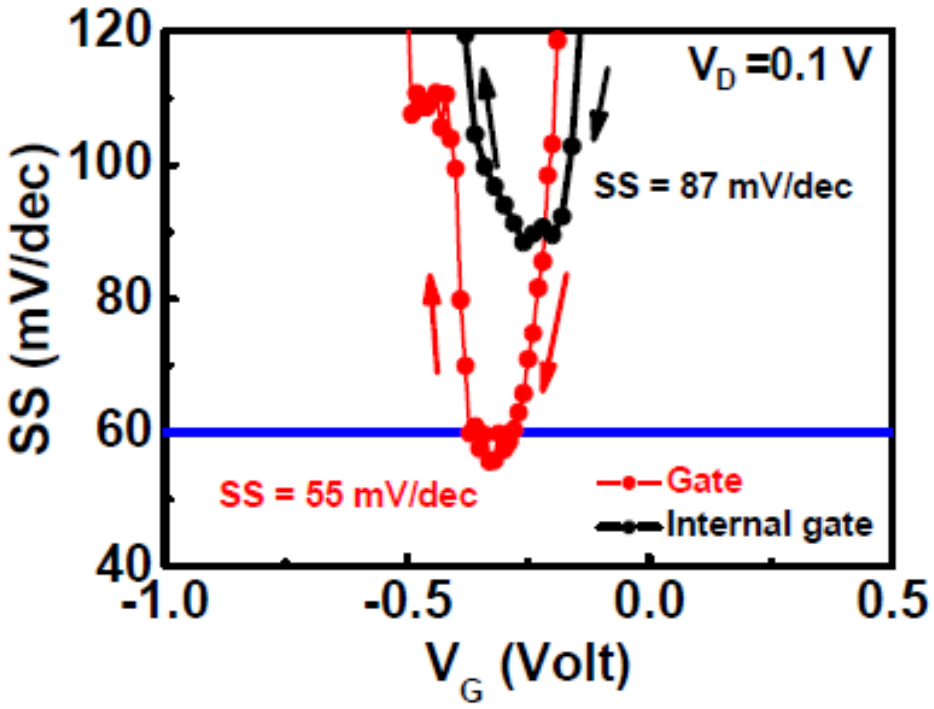
Transconductance (g_m) vs. V_{GS}. The peak g_m is enhanced 118% by the NC integration.

M.H. Lee, IEDM'2013

Fe FinFET

(*K.-S. Li - IEDM'15*)





SS ↓ for Fe FinFET / FinFET

Fe material : $Hf_{0.42}Zr_{0.58}O2$

Conclusion

- We are facing many challenges, scaling, performance and power reduction which is one of the most important challenge for future nanoscale devices
  =>requires **new physics and device structures** using **many novel materials**
  =>will enable to continue scaling and performance/**power improvement**

- **FD SOI**, **MG** Devices for for *Low power/high speed*

- **TFETs** (MG, SOI, GOI, III-V, NW, Strain, HTJ, Grad, QW, 2D), **TFET/FeFET**
  => for Ultra-low power:

  => **Best Small Slope Switch** up to now
  => allows for **sub-60mV/dec S** (simulation + experimental results)

  => **TFETs** simulations show promise for very good S, substantial Vdd reduction and high Ion but technology boosters especially **using new materials and devices** and ***additional process improvements (reduced defect density) are needed to improve real device performance***
  => *Applications:* *very low power/low-medium speed, Analog/RF, Sensors…… ?*

Thank you for your attention!

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Sinano Institute Members

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