



NanoElectronics Roadmap for Europe: Identification and Dissemination

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ABSTRACT:

This report of the Project "NanoElectronics Roadmap for Europe: Identification and Dissemination" (NEREID) describes the release of the first version of the NEREID roadmap, referred to as Mid-Term-Roadmap. It has been elaborated by the project consortium in a careful process of collecting expert information. For this purpose, NEREID organized a series of several workshops where experts exchanged their ideas while the NEREID partners took notes of this in order to take them as an inspiration for writing the roadmap. The Mid Term Roadmap has then been published on the NEREID website (https://www.nereid-h2020.eu/) on September 11, 2017. On the same day, the NEREID consortium introduced the roadmap during the Sinano-NEREID-Workshop embedded in the ESSCIRC/ESSDERC conference. Furthermore, the Mid Term Roadmap will be presented in the Speaker's Corner during EFECS 2017 in December 2017 in Brussels.

¹ PU = Public; CO = Confidential, only for members of the Consortium (including the EC services).

² R = Report; R+O = Report plus Other. Note: all "O" deliverables must be accompanied by a deliverable report.

³ eg DX.Y_name to the deliverable_v0xx. v1 corresponds to the final release submitted to the EC.

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Release	Date	Reason for Change	Status ⁷	Distribution
V0.1	11/24/2017	First version	Draft	SC
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⁶ Typically person(s) with appropriate expertise to assess the deliverable quality. 7 Status = "Draft"; "In Review"; "Released".

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Introduction

The objective of the H2020 NEREID Coordination and Support Action (n° 685559) is to elaborate a new roadmap for nanoelectronics, focused on the requirements of European semiconductor and applications. It will address societal challenges following advanced concepts developed by Research Centres and Universities in order to achieve an early identification of promising novel technologies covering the R&D needs all along the innovation chain. The final result will be a roadmap for European micro- and nanoelectronics, with a clear identification of medium and long term objectives.

Within this deliverable report, the release of the first version of this roadmap - referred to as Mid-Term-Roadmap - is described. It has been elaborated by the project consortium during the first 18 month of the project in order to be able to publicly discuss this first version in order to identify possible improvements.

1. Mid Term Roadmap

The Nereid roadmap for nanoelectronics is dedicated to be used as input for future research programmes at European and National levels in order to join our effort to overcome the main challenges in nanoelectronics and put the EU at the forefront of future technological developments. Therefore it takes into account the specificity of the European industrial and academic landscape, and helps to better coordinate academic and industrial research for equipment, semiconductors and application developments.

1.1 Character of the Roadmap

The NEREID roadmap is divided into several main technology sectors: Advanced Logic (including Nanoscale FETs and Memories) and Connectivity, Functional Diversification (Smart Sensors, Smart Energy, Energy for Autonomous Systems), Beyond-CMOS (Emerging Devices and Computing Paradigms), Heterogeneous Integration and System Design, Equipment, Materials and Manufacturing Science, and also includes cross-functional enabling domains.

The NEREID Roadmap, focused on medium and long term time horizons, is complementary to the industry driven AENEAS Strategic Agenda, the ECSEL MASRIA and the currently developed ECS Strategic Research Agenda, which are focusing on shorter terms. Besides the timescale, the NEREID Roadmap differs to the other agendas with respect to topics (no chapter dedicated to applications while applications are considered initially and "in the background"), method (s. below) and the treatment of figures of merit (more detailed view). Additionally the NEREID Roadmap covers the whole range of TRL's, starting with TRL 1 as the work is led by academia, not industry-driven (although, for each WP, there is an industrial ("shadow") co-leader, and the contributors come from the two communities).

NEREID has some commonalities and is developing joint collaboration with the new International IRDS Roadmap especially in the fields of More Moore, Beyond CMOS and computing systems, but is also complementary to IRDS with very important NEREID activities in the More than Moore domain (e.g. Smart Sensors, Smart Energy, Energy Harvesting), which is a sound European competence, leading to a large diversity of electronic systems useful for many applications. In the More Moore field, there are also strong interests in Europe for specific activities dealing with very low power systems, leading to possible disruptive applications for instance for future IoT systems.

Understanding the dependencies between short/medium term (e.g. More Moore and More than Moore) and long/very long term (e.g. Beyond CMOS) activities is also very important to speed-up technology transfer between academia and industry using disruptive technologies leading to possible new large future markets. Therefore, the Nereid Roadmap takes into account the specificity of the European industrial and academic landscape, and will be very important to better coordinate academic and industrial research for equipment, semiconductors and application developments, as well as serving as the input for future research programmes at European and National levels in order to join our efforts to overcome the main challenges in nanoelectronics and put the EU at the forefront of future technological developments.

1.2 Method to Build the Roadmap

The project solicits application and technology experts from leading industrial and academic research organizations to participate to General and Domain (WPs) Workshops while in return covering their travel expenses. These Workshops allow the consortium to better define the technology roadmap according to application requirements (in the fields of Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing) and technology evolution (Advanced Logic and Connectivity, Functional diversification, Beyond-CMOS, Heterogeneous Integration and System design, Equipment, Materials and Manufacturing Science). Structured discussion and debate provide the convergence between applications and technologies, as shown in the figure below:

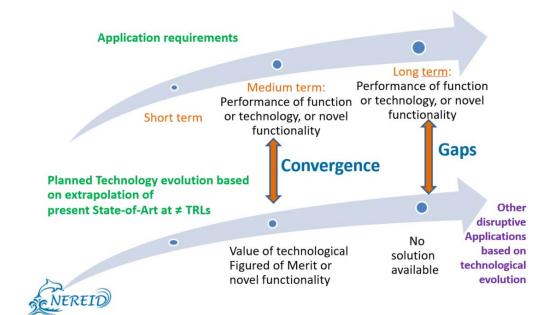


Figure 1: The NEREID roadmapping approach

The proposed idea is that the scenarios of evolution of the products/applications will result in performance evolution scenario for the functions, which could be generic enough to apply to many products. The next step in the roadmapping process is then to derive, from the evolution of functions, the evolution of the underlying technologies and devices using the expertise of technology experts. Insights on future technology evolution and availability can also prompt new ideas for disruptive products and applications, which are discussed in Domain Workshops and also presented by technology experts during the General Workshops.

This common work between technology and application experts leads to the early identification of the most promising technologies needing additional R&D actions, which could be very useful for the future electronic products of European companies leading to a strong impact on the European economy and society.

2. Roadmap Release

The development of the first version of the roadmap referred as Mid-term Roadmap was delayed with respect to the project proposal. The reason for this was that the collection and aggregation of expert input took quite longer than expected. As the quality of the first published release has been recognized as very important, the project partners and the project officer have decided to postpone the release of the first version by three month to M21. This time shift has been chosen as it seemed adequate to guarantee the desired quality of the Mid-term Roadmap and because of the choice of the event, where the Mid-term Roadmap could be published. The choice of the event fell on the ECCIRC/ESSDERC conference, where NEREID (in cooperation with the European Institute of Nanoelectronics SINANO (www.sinano.eu)) was invited to hold a workshop within the conference schedule. In this workshop, the

NEREID project reported on its recent findings documented in the Mid-term Roadmap and faced a vivid feedback situation with the audience of about 40 participants of the workshop aiming to verify the current results by discussing especially controversial points.

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	External Events Mid-term Roadmap Other Strategies & Roadmaps Publications Contact Imprint Advisory Board General Assembly	circuits and architectures with a view to the time when CMOS scaling begins to loose some ground. The document was compiled by the EU H2020 ICT project NEREID, based on presentations and discussions during the workshop series held between November 2015 and August 2017. Please fill in the form below to download your free PDF copy of the "NanoElectronics Roadmap for Europe" If you have an account at the edacentrum or NEREID website, it is useful for you to login first, before you register for this event, because your data will be filled in the online registration form.	Largeon Commission
	Internal Documents v WebDAV (OwnCloud) Information Connect as network drive by batch file	If you have any questions you can send an email to popp@edacentrum.de	Sol
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		Name of organization: * (as will be printed on participant badge) Email: *	
		Remarks to NEREID partners:	
		Declaration of Interest: * O Yes, I agree, you can contact me regarding the improvement of the NEREID roadmap. O No, I disagree. Do NOT contact me regarding the improvement of the NEREID roadmap.	
		We are very much interested in a collaboration on improving the NEREID roadmap until the final version will e released in autumn 2018. If you are interested to get information on the updating process or like to be involved in improving it, please select accordingly above. Privacy policy Submit	
		Login or register to post comments	
	The NEREID p	roject (ICT-CSA-685559) is supported within the Research and Innovation Programme Horizon 2020	ể by the EU.₽.

At the same time on September 11, 2017, the Mid-Term Roadmap has then been published on the NEREID website (https://www.nereidh2020.eu/). The roadmap is available for free download after filling in a web form, which collects the contact information of everybody who likes to download the roadmap. The Form looks as shown on figure 2 on the left. In this way, NEREID is enabled to contact the readers Mid-Term Roadmap in order to ask for their feedback.

Figure 2: Registration form at NEREID website: https://www.nereid-h2020.eu/roadmap)

Furthermore, the Mid Term Roadmap will be presented in the Speaker's Corner during EFECS 2017 in December 2017 in Brussels.

4. Conclusion

This report described the release of the Mid-term Roadmap of NEREID, which has been presented during a public workshop embedded in the ESSCIRC/ESSDERC conference while it has been published on the NEREID website. The procedure of the release considers the project's main purpose to bring the "NanoElectronics Roadmap for Europe" to a broad audience quickly and in particular, to all relevant decision makers engaged in micro- and nanoelectronics coming from industry and academia as well as to policy makers and public authorities especially at European level. Thus, the roadmap release will lead to a broad feedback from the micro- and nanoelectronics community in that way will help all project partners to improve the current version.

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