NanoElectronics Roadmap for Europe: Identification and Dissemination

D5.1	Report on Workshop 1 and their impact to system integration, and case studies for Task specific Workshops		
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ABSTRACT:

This Deliverable reports the discussions and the conclusions taken during the NEREID General Workshop 1, held in Grenoble 12-13 of April 2016, for WP5 “System Design and Heterogeneous Integration”.

During this meeting several discussions and round tables have been organized, for stimulating the interaction among the participants, linking industrial and academic partners.

In particular, related to WP5, most of the work has been focused on choosing the best approach for the preparation of the Roadmap. In fact, System Design and Heterogeneous Integration are two topics very difficult to insert in a specific grid, due to their intrinsic multidisciplinarity and broad range of topics. For example, in System Design must be taken in account the four different description levels (physical, device, architectural, system) for obtaining the correct description of the system and its related models.

For these reasons the conclusions reached after the Workshop interactions are that it is impossible to categorize and numerically measure the Figure of Merits in System Design roadmap, but a similar approach as the one used in System Design has to be applied: in a first step the System Design and Heterogeneous Integration Roadmap must be built with a top-down approach, starting from the application of reference, remembering that in this domain the right approach has to be Application-Driven. Then, individuated the tree description of the design roadmap, this has to be filled with a bottom-up process, where the detailed specifications and requests are indicated.

1 PU = Public; CO = Confidential, only for members of the Consortium (including the EC services).
2 R = Report; R+O = Report plus Other. Note: all “O” deliverables must be accompanied by a deliverable report.
3 eg DX.Y_name to the deliverable_v0xx. v1 corresponds to the final release submitted to the EC.

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1.0	13/06/15	Starting Version	Draft	WP5 members, Experts and Industrial Application Experts cited in Deliverable
2.0	30/06/2016	Last Version ready for WP5 and Application Experts Approvals and Feedbacks	Pre-Final	WP5 members, Experts and Industrial Application Experts cited in Deliverable
3.0	30/07/2016	Version with feedbacks received from Ralf Pferdmenges	Pre-Final	WP5 members, Experts and Industrial Application Experts cited in Deliverable
Final	07/08/2016	Amendments proposed by Benoit Clement	Final	WP5 members, Experts and Industrial Application Experts cited in Deliverable

[4] Person from the lead beneficiary that is responsible for the deliverable.

[5] Person(s) from contributing partners for the deliverable.

[6] Typically person(s) with appropriate expertise to assess the deliverable quality.

7 Status = "Draft"; "In Review"; "Released".

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Executive Summary

Goal of this Deliverable is to describe the process that was used for preparing the first preliminary structure of the Roadmap for System Design and Heterogeneous Integration, then to report the obtained results after the discussions and interactions among the partners, and in particular among Task Leaders and Technical Experts.

List of Figures

List of acronyms / abbreviations used in this document

WP WorkPackage
IoT Internet of Things
FET Field Effect Transistor
I/O Input/Output
ADC Analog to Digital Converter
DAC Digital to Analog Converter
PMR Professional Mobile Radio
TWG Technology Working Group
CMOS Complementary Metal-Oxide Semiconductor
MtM More than Moore

Introduction

The work during the Workshops has been organised in four different sessions:

- Session 1: eliciting which requirements/functions arise from future applications;
- Session 2: listing a set of possible technologies that are promising for the different time horizons;
- Session 3: converging the two views by eliciting a first set of technologies, which could be used for the (generic) functions, split in 6 groups;
- Session 4: presenting the results of Session 3, cross-refining and synthesizing them, for the individuation of next steps.

The participants of WP5 discussed in particular the Workpackage topics in Session 2 and 3, sharing the application requests of Session 1 and the synthesis in Session 4, with all the other Workshop participants.

For each of the 4 Sessions it was requested to prepare reference tables or structured documents in which to indicate:

- for Session 1 the answers for the 8 Application Domains
    - Energy
    - Automotive
    - Medical/Life science
    - Security
    - IoT/Smart connected objects
    - Mobile convergence
    - Digital manufacturing
    - Transportation
- for Session 2 to give the answers for each of the 10 Technologies, split in separated groups
    - Emerging devices
    - Computing paradigms
    - Nanoscale FET
    - Connectivity
    - Smart sensors
    - Smart energy
    - System design
    - Heterogeneous integration
    - Equipment and materials
    - Manufacturing science

  and so for WP5 the request was for ***System Design*** and ***Heterogeneous Integration***.
- for Session 3 to prepare an indication about “Which technologies can satisfy the required function performance for each application/function” of the 8 presented in Session 1
- to summarize the obtained results in Session 4.

1. Session1

In Session 1 different application domains were presented and for each have been elaborated the impacts on WP5 System Design and Heterogeneous Integration.

1.1 Application Domains Presentations

In the next sections are commented the presentations of the Application Domain Experts that raised the major interest for WP5 work. The ones with an impact on WP5 were on:

- Internet of Things
- Automotive
- Defence and Space

The other presentations are not reported or because they gave similar inputs, or because they were of not interest for WP5.

1.1.1 Ovidiu Vermesan, SINTEF, Oslo: Trusted IoT, Applications and Technology

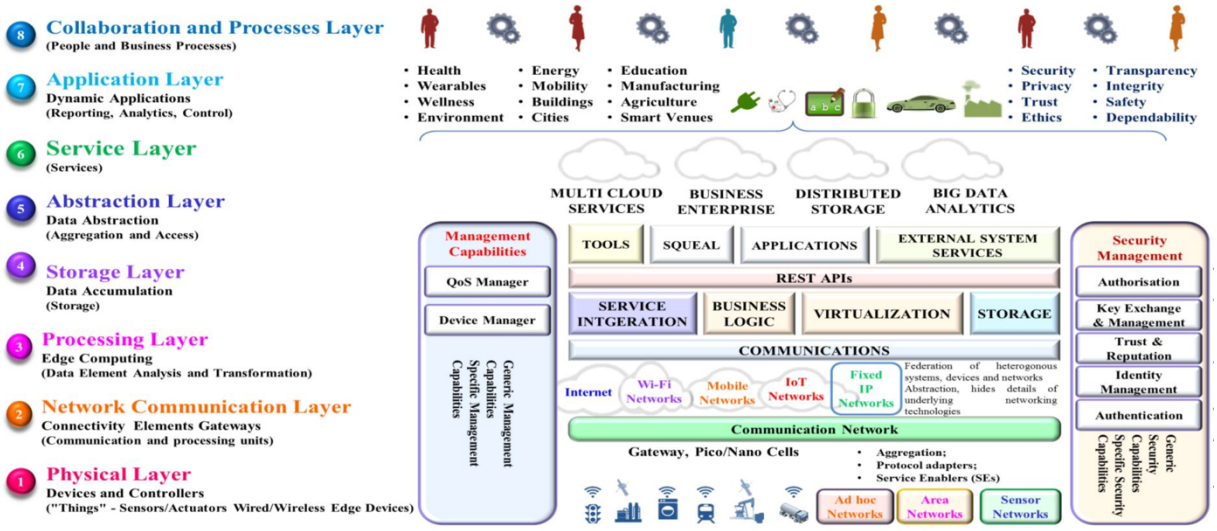


Figure 1: IoT Architectural View

Impacts on WP5

a. Multidisciplinarity
b. Convergence of Technologies
c. Systems of Systems and their Interconnections
d. Smart Environments, so different sensors and complex data elaboration
   => Cyber-Physical Systems
e. Different Application Domains and Markets, so different prices and marketing goals
f. Integration: Sensors, Devices, Gateways, Equipment, Mobile Assets
g. The Architectural Level of IoT, represented in Figure 1, where are clear the different levels of descriptions and so of System Level Design needs
h. Security Challenges

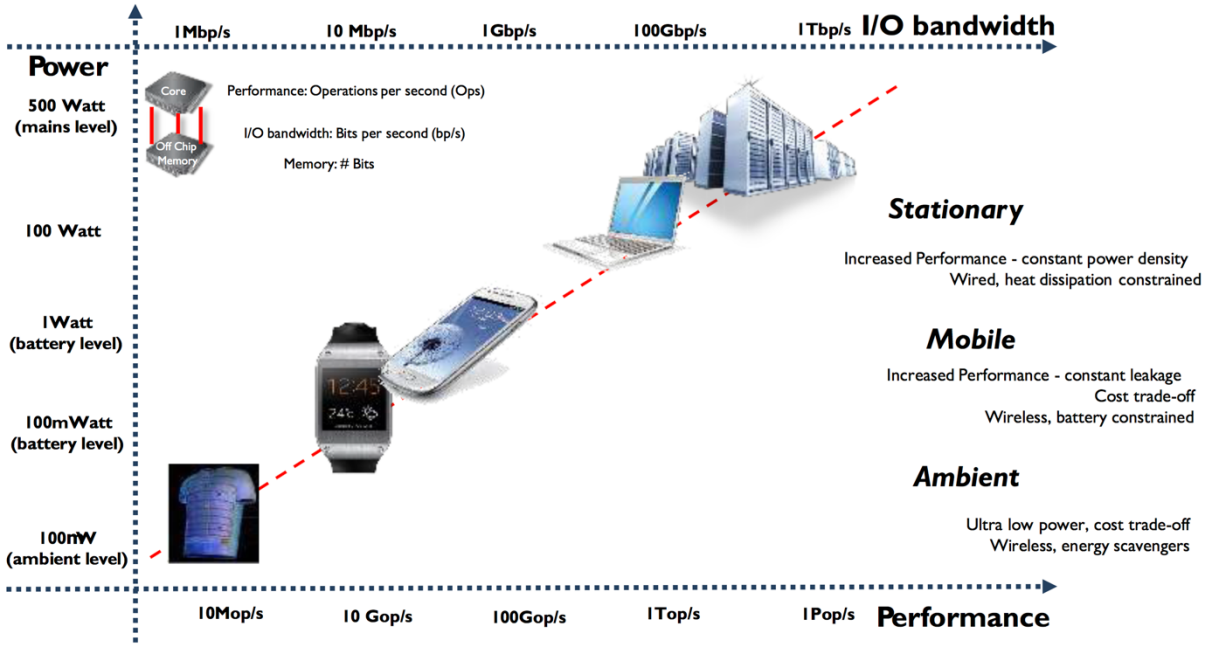


Figure 2: System Applications Requirements

In Ovidiu Vermesan's presentation has been showed a very interesting graph, useful for System Design in particular, as depicted in Figure 2, where the requirements in terms of Performance, Power and I/O Bandwidth are shown.

The reported figures have to be taken in account for the preparation of the Roadmap for WP5 goals. From this presentation it is immediately clear how a System Design must be Application-Driven, because as first in terms of Performance, Power and I/O Bandwidth the constraints and so the Design approach must be different.

As reported in Figure 2, for example, related to the different application environments, the constraints are different:

- Stationary
  - Increased Performance - constant power density
  - Wired, heat dissipation constrained
- Mobile
  - Increased Performance - constant leakage
  - Cost trade-off Wireless, battery constrained
- Ambient
  - Ultra low power, cost trade-off
  - Wireless, energy scavengers

1.1.2 Vincenzo Murdocco, CRF - Driver Assistance Systems Unit Manager: Automotive

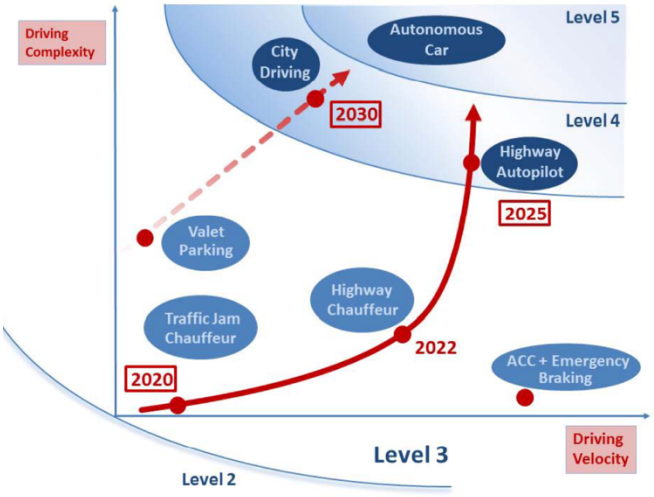


Figure 3: Automotive Roadmap

In this presentation very interesting inputs were given by Dr. Murdocco.

The vehicles of the future will continue the increase in the use of electronics and telecommunication systems, so a Roadmap for nanoelectronics must consider the challenges proposed by Automotive Industry. Some of the reported requests are equivalent to the ones presented in previous section, but the application in consumer market and the strong links to regulations raised a specific interest in standardization and safety.

In Figure 3 is depicted the presented Automotive Roadmap, from where is clear the goal of reaching an autonomous system in the next future, with the necessary impacts on System Design and Heterogeneous Integration.

Impacts on WP5

a. Standardization and certification
b. Redundancy
c. Safety for Humans and Data Security
d. Validation
e. Stability in different environments, mostly in large temperature ranges

f. Long life time

In the presentation, the most important highlights, useful for WP5 work, were:

a. The roadmap is covering key enabling technologies for sensing, system integration and communication architecture, handling of human factors and functional safety;
b. Further developments are required in the field of electronic components and systems;
c. New technology has to be able to filter, process and evaluate the data that are vital for the transport and the passenger (data safety and data privacy).

1.1.3 Airbus Defence and Space: PMR introduction and perspectives.

From this talk several points were in common with the previous ones. The most important focus was on Radio, in fact PMR stands for Professional Mobile Radio, and safety and reliability were again underlined. Currently widely spread PMR networks are, voice service oriented, Narrow-Band (NB-PMR) so called because they rely on few kHz wide channels. In addition, Public Protection and Disaster Relief (PPDR), new high speed data service for PMR based on LTE broadband technology (BB-PMR) is under definition and standardization.

Impacts on WP5

a. Networks reliability (mission critical).
b. Security and confidentiality.
c. Higher power than commercial radio equivalent.
d. Detailed technical requests:
    i. High quality factor tunable resonator for filter, oscillator, terminal factory alignment. Only for NB-PMR.
    ii. High dynamic low band pass ADC/DAC (flicker noise). Only for NB-PMR.
    iii. Power amplifier (PA) efficiency enhancement system.
    iv. Highly linear LNA / driver / PA (with two modes HandHeld or mobile)
    v. Low insertion losses switches

In the presentation two final issues were mentioned:

1. Function price shall be close to regular commercial solutions. Due to PMR competitiveness we can’t afford specific highly costly parts;
2. Part shall be available for over 10 years.

1.2. Results and discussion / Perspectives

Taking inspiration from the Industrial Application Experts, for WP5 the challenge is to merge the very different approaches and requests, for finding a harmonized structure of a possible Roadmap, that must consider the different aspects, but the most important message is that the process must be Application-Driven.

2. Session 2

In Session 2 were presented the results of the previous discussion held by WP leader, Task Leaders and WP Experts, who prepared the first table useful for opening the discussion.
The work started considering the paper presented by Prof. Kahng at the Design Automation Conference (DAC) of 2013 [1], where are highlighted the conclusions of ITRS Design Chapter's reports [2]-[5], containing several key messages, useful for WP5 Work:

- Software and system-level design productivity are critical to the roadmap of semiconductor value
- Design reliability roadmapping was a necessary addition to the roadmap
- System-level design techniques would ultimately be crucial to managing power
- Design technology innovations must keep on schedule through the end of the roadmap in order to contain design costs

New messages were indicated in 2011 and 2012 Design Chapter's reports:

- Roadmapping focus at the design-manufacturing interface has evolved from "manufacturability" to a more general "variability", which now entails an even broader question of how systems will maintain reliability and be resilient
- Design technology innovations must keep on schedule through the end of the roadmap in order to contain power
- The importance of cross-TWG (Technology Working Group) interactions is continually growing, whether for More Than Moore, 3D, Beyond CMOS, or even the basic device and lithography roadmaps

Starting from these considerations, the tables of the Figures of Merit related to System Integration were organized in:

- Targets requested from the market to the System Design (SD) Tools (Figure 5)
  -> The evaluation corresponds to the importance of the implementation of this target in SD
- Technologies/Solutions needed for System Design (Figure 4)
  -> The evaluation indicates the importance of the adoption of this Technology/Solution in SD

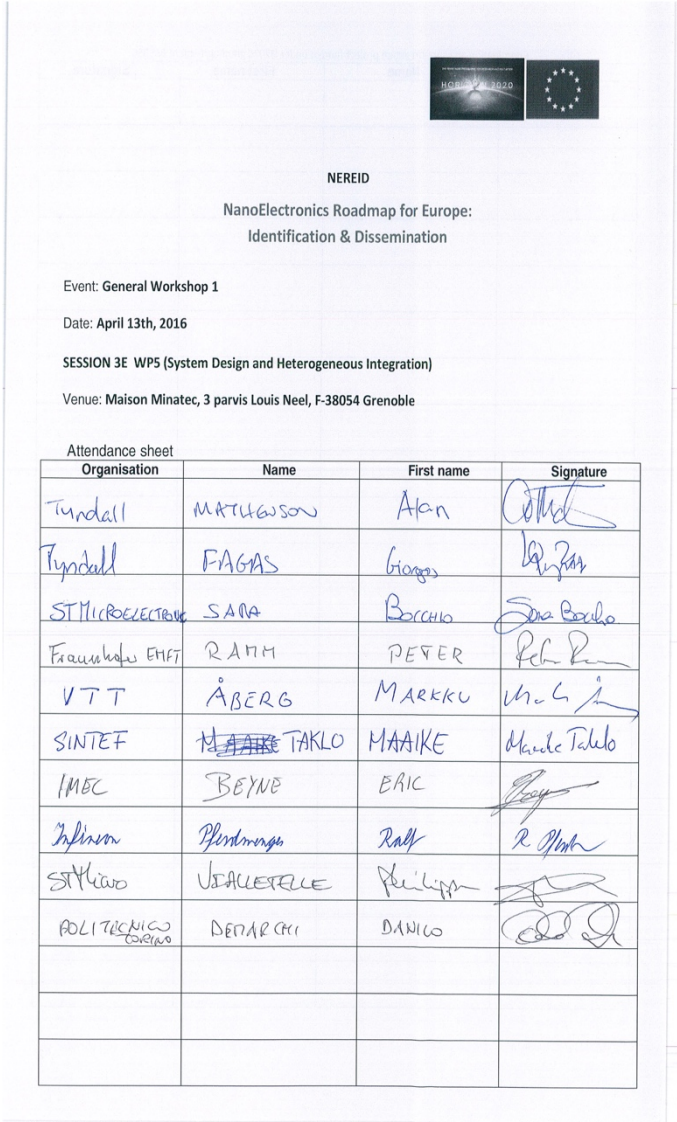
Criteria	Figures of Merit		
	<3 Years	<6 Years	>7 Years
Low Power	XXX	XXX	XXX
Co-Design (HW-SW? or Chip – Package- PCB ? or for heterogeneous IoT type components: electric – MEMS/Sensor or all of them?)	XXX	XXX	XXX
High Performances of Final System	XX	XX	XX
Automatisation – Customisation	XXX	XXX	XXX
Packaging Awareness & 3D	XX	XXX	XXX
Validation	XXX	XXX	XXX
Reliability in harsh environment	XX	X	X
Reliability – complexity	X	XX	XXX
Reliability – over life time (Ageing, updating the SW-part; reconfiguration during life time)	X	XX	XXX
Cost of Final System	XXX	XXX	XXX
Cost of Design (Big elapsed time and the big effort due to unsufficient automation)	XXX	XX	XX
Tool Cost (The design will happen more and more on the SW side where the tools are used by more people and therefore cheaper)	XXX	XX	X
Tool Flexibility and Customability	XX	XX	XX
Design for Manufacturability (The manufacturers have to care for it)	XX	XX	XX
Tool Performances (Speed, … We need the shift to higher abstraction levels and corresponding new methodologies)	X	X	X
System Level Tooling	X	XXX	XXX
(we still are in an infancy and we need a fast improvement)			
New methodologies (based on new capabilities like Big Data, Clouds, cognitive computing)	X	XX	XXX

Figure 5: WP5 Figures of Merit for Targets

Criteria	Figures of Merit		
	<3 Years	<6 Years	>7 Years
Propagation of Constraints	XXX	XXX	XXX
Multi Domain Integration	XX	XX	XXX
System Partitioning	XXX	XXX	XX
Open Tool	X	X	X
Reconfigurable Architectures	XX	XXX	XXX
Application aware Design	XX	XX	XXX
Architecture Optimization	XX	XX	XXX
Virtual Prototyping	XX	XXX	XXX
Multi Processor SOC	XXX	XXX	XXX
New architectures (like Neuromorphic Processors)	X	XXX	XXX
Re-Use infrastructure (Including standards, open interfaces, open/new languages)	XX	XXX	XXX

Figure 4: Figures of Merit for Technologies/Solutions

3. Session 3



NEREID

NanoElectronics Roadmap for Europe:
Identification & Dissemination

Event: **General Workshop 1**

Date: **April 13th, 2016**

SESSION 3E WP5 (System Design and Heterogeneous Integration)

Venue: **Maison Minatec, 3 parvis Louis Neel, F-38054 Grenoble**

Attendance sheet

Organisation	Name	First name	Signature
Tyndall	MATHESON	Alan	
Tyndall	FAGAS	Giorgos	
STMICROELECTRONICS	SARA	Bocchio	
Fraunhofer EMFT	RAMM	PETER	
VTT	ÅBERG	MARKKU	
SINTEF	~~MAAIKE~~ TAKLO	MAAIKE	
IMEC	BEYNE	ERIC	
Infineon	Pferdmenges	Ralf	
STMicro	VIALLETELLE	Philippe	
POLITECNICO TORINO	DEMARCHI	DANILO	

Figure 6: WP5 Session 3 Participants

In Session 3 the work was organized in a specific group were the topics related to System Design and Heterogeneous Integration were analysed and discussed in details.

The participants to this round table were, as depicted in Figure 6:

1. Alan Matheson, Tyndall
2. Giorgios Fagas, Tyndall
3. Sara Bocchio, STM, WP Expert
4. Peter Ramm, Fraunhofer EMFT
5. Markku Aberg, VTT
6. Maaike Taklo, Sintef
7. Eric Beyne, IMEC
8. Ralf Pferdmenges, Infineon, WP Expert
9. Philippe Vialletelle, STM
10. Danilo Demarchi, PoliTo, WP Leader

The discussion took in consideration the inspiring inputs received in Session 1, and the mapping with the results of Session 2 was done.

A first general comment can be related to the first part of the session, where it was examined in detail the best approach needed for extracting the correct structure of a Roadmap, from the very different approaches needed to map applications, technologies and solutions, to be integrated in a unique view for System Integration needs.

The solution was found in a two steps process, where a Hierarchical Tree has to be built, starting from the Application, with a Top-Down approach. Then, a Bottom-Up process is needed for filling the content of the Tree built in the first step.

Figure 7: Top-Down Tree for System Integration Roadmap

So, the final WP5 goal is to build 2 different Maps, for the 2 different needed approaches:

- Top-Down, where are listed the important issues to be considered and that will produce as output a Data Package describing the System;
- Bottom-Up, that is the list of requests to be given to the Tool Vendors, the Manufacturing Companies, … This is useful for System Planning mostly, because it contains the bottom-level important issues to be considered when the design of a System is started.

In Figure 7 is reported the first Draft of the Top-Down Map, to be completed and finalized in the next NEREID project activities. In principle, as can be seen, it is Application-Centric, and from the Application are derived the first important features/specifications:

- Functional Specs
- Interfaces
- Form Factor
- Energy/Power
- Response Time
- Manufacturability
- System Level Reliability
- Testing & Validation
- Cost
- Timeline
- Reconfugurability/Flexibility
- Lifecyle
- Security (hacking)
- Safety

The most interesting general comments, extracted from the group discussion are:

- In More than Moore devices the usual "run faster but consume less" is not the driving force, instead multi-objective and multi-constraints approaches have to be considered, as for example area and reliability are the major figures to be considered in design choices for smart power technologies
- It is important to integrate aspects like sensing and power management. In particular, the last one is an application independent issue:
  - all systems need to be powered, and in particular often in More than Moore devices needs to:
    - condition the energy or power supply in an usable form for the electronic circuit (e.g. dc-dc or ac-dc conversion)

        - scavenge any outside source of energy or power for supplying or complementing the supply of the integrated system (only for autonomous systems) store energy (e.g. capacitors) which is critical in case of intermittent energy or power supply
        - possibly supply energy or power through sources integrated in the SoC or SiP (e.g. micro-battery or integrated fuel cell)
- The system design should cover aspects for power in MtM devices: from one side we need software development tools for power management, from the other side we need a way to define specify and verify the power management and its integration in systems (not at gate level)
- Trend in sensor components is the integration of several sensing functions (e.g., the so called combo MEMS sensors where multi-axis inertial and magnetic field sensing are integrated) in a single module, together with specialized processing functions for the sensor signals
- In relation to connectivity (task 3.2) critical needs are at system level safety, security and certifications and the main topics in system design can be:
    - Specification, code generation & verification for Safe & Secure systems
    - Simulation & Certification
- The System must be considered in its complexity, so design tools must integrate Power, Sensors, Electronics, Packaging/3D, Wireless/RF, … all in a unique tool
- Integration of Heterogeneous parts must be considered at System Level for constraint propagations and process level impacts

Several conclusions can be derived from the brainstorming done in Session 3 in Grenoble Workshop related to System Planning and Design:

- The Use Case Application must be the main Target for extracting:
    - High Level Specifications
    - Physical Properties
    - Application Environment
    - Interface with Environment/Network
    - Human Interface
- The Top-Down information for the System Planning has to be described in a formal way, and the best solution seems to be an XML description of a Datasheet-Like document containing all the listed points in the Top-Down Map
- Constraint Propagation is a key issue
- Multi Domain Models and Awareness must be considered

- System Partitioning is the key issue for the correct structure of the Design and the related System Integration and:
  - It is a MUST to have a unique tool merging all the different modules/sub-parts/technologies
  - It is important to consider Module Reuse
- Standardization has to be mostly considered for:
  - Interfaces
  - Protocols
  - XML Data Package
- Virtual Prototyping is one of the novelest opportunities to be exploited, and it is important at the different levels:
  - For Designers
  - For Customers, showing a virtual view of the final System
  - 3D Printing for both
- Secure Model Extraction is important for System Reliability, but for Ecosystem Infrastructure too, for data/model exchange
- Manufacturability Issues can be summarized as:
  - Die Size
  - Quality of Separation (Dicing)
  - Fragility of System Level Component
  - Constraints
    - Thermal
    - Mechanical
    - ESD & Voltages
    - Chemical Compatibility with Processes
    - Radiation
    - Interaction among the different components (Yield, Reliability, Repeatibility, Performances)
  - Throughput
- Thermal Awareness has to be considered in System Design
- Metrology Indications must be implemented for:
  - Critical Parameters
  - Manufacturing
  - Extraction of Real System Characteristics

- Architectural System Level Processes must consider:
  - Routing
  - Stresses
  - Testability
  - Absence of Design Tools
- Integration of Passive Devices has to be taken in account
- Packaging Awareness at the First Level of Design is an important issue to be considered, having a direct impact on design and effectiveness of performances
- Interactions with Software Designers are needed for:
  - Performances
  - Optimal Operating Point
  - Power Consumption
- New Concepts in Computing and Architectures are appearing and it is time to start to consider them at System/Application Level, as for example:
  - Neuromorphic Architectures
  - Bio-Inspired Systems

4. Session 4 and Conclusions

In Session 4 the results of WP5 interactions were presented and shared with the rest of NEREID Workshop participants.

The further actions for WP5 will be to finalize the 2 proposed Maps, starting to focus to some Application Domains that will be taken as examples for demonstrating and validating the efficacy of the method.

The proposal is to work on:

- Automotive
- Biomedical Applications

These two application domains are considered enough complete, covering very different aspects of physics, technology, application requests and methodological approach.

5. References

[1] B. Kahng, "The ITRS design technology and system drivers roadmap: Process and status," Design Automation Conference (DAC), 2013 50th ACM/EDAC/IEEE, Austin, TX, 2013, pp. 1-6

[2] EDA Roadmap Workshop at DAC 2010, http://vlsicad.ucsd.edu/EDARoadmapWorkshop/

[3] J.-A. Carballo and A. B. Kahng, “ITRS Chapters: Design and System Drivers”, Future Fab International (36) (2011), pp. 45-48

[4] J.-A. Carballo and A. B. Kahng, “ITRS Chapters: Design and System Drivers”, Future Fab International (40) (2012), pp. 54-59

[5] J.-A. Carballo and A. B. Kahng, “ITRS Chapters: Design and System Drivers”, Future Fab International (44) (2013), pp. 52-56