NanoElectronics Roadmap for Europe: Identification and Dissemination

D1.2	Roadmap priorities from 1st General Workshop with applications		
Project :	NEREID H2020- 685559	**Start / Duration:**	16 November 2015 / 36 Months
Dissemination:	PU	**Nature:**	**R**
Due Date :	M7		
Filename:	D1.2 roadmap priorities- vFINAL		

Deliverable Contributors:	Name	Organisation	Role / Title
Deliverable Leader[1]	Enrico Sangiorgi	SINANO	Technical Coordinator
Contributing Author(s)[2]	Francis Balestra	Grenoble INP	Coordinator
	Pascale Caulier	SINANO	European Project Manager
	Sylvie Pitot	Grenoble INP	European Project Manager
Reviewer(s)[3]	Livio Baldi	AENEAS	Industrial co-Leader
Final review and approval	Francis Balestra	Grenoble INP	Coordinator

Document History:

Release	Date	Reason for Change	Status[4]	Distribution
V0		Creation		Management Team (GINP/SINANO)
V1	13/06/16	Update	Draft	Steering Committee & Applications experts
V2	12/07/16	Completion	In review	Management Team and Industrial co-leader
V4.2	22/07/16	Finalization	In review	General Assembly/Steering Committee for approval
VFINAL	27/07/16	Submission	Released	EC

1 Person from the lead beneficiary that is responsible for the deliverable.

2 Person(s) from contributing partners for the deliverable.

3 Typically person(s) with appropriate expertise to assess the deliverable quality.

4 Status = “Draft”; “In Review”; “Released”.

1 Executive Summary

After 5 months of operation, the first General Workshop was successfully organized on April 12-13, 2016 in Minatec, Grenoble, France, by Grenoble INP and SINANO Institute. It was devoted to confront cross-industry presentations spanning six wide and diverse applications (Security, Automotive, Energy, Digital Manufacturing, Internet of Things and Medical/Health) with the NEREID technology domains and project tasks (Beyond CMOS Technologies, Nanoscale FET & Connectivity, Smart Sensors & Smart Energy, System Design & Heterogeneous Integration, Equipment, Materials and Manufacturing Science). The overall method aimed at solving potential market competition problems among application experts by focusing the workshop on high-level abstracted functions and by inviting application experts from separated fields.

Structure and approach of the workshop enabled progress in three fundamental areas:

1) an overview of the future for six key application domains,
2) a comprehensive and synthetic assessment of the available technology base and
3) the definition of general guidelines for the possible alignment of future application requirements with evolving semiconductors technologies.

This preliminary alignment gave interesting results and useful indications, in particular about the main requirements for future applications in the investigated sectors and the possible gaps that could need increased performance of existing technology or the introduction of new functions, based on novel technologies. This first analysis will be further developed in the framework of future Domain (Task/WP) and General Workshops.

The possible ways to look for «generic functions» capable of generating a roadmap for industry will also be studied in the next steps of the project.

TABLE OF CONTENTS

1 Executive Summary: 3
2 Abstract 5
3 Workshop methodology 5
4 General outputs of the Workshop 5
4.1 Application Domains 6
4.1.1 Internet Of Things 6
4.1.2 Automotive 6
4.1.3 Digital Manufacturing 8
4.1.4 Medical/Health 8
4.1.5 Security 8
4.1.6 Energy 9
4.2 Scientific/Technical WPs and Tasks 10
4.2.1 WP2 - Beyond CMOS 10
4.2.2 WP3 Advanced Logic and Connectivity 11
4.2.3 WP4 Functional diversification: 14
4.2.4 WP5 – System design and Heterogeneous integration 15
4.2.5 WP6 – Equipment and Manufacturing science 17
5 Conclusions 17
6 Annex 19
6.1 1st General Workshop overall organization 19
6.2 Glossary 20

2 Abstract

The first General Workshop was successfully organized on April 12-13, 2016 in Minatec, Grenoble, France, by Grenoble INP and SINANO Institute. The distinguishing characteristic of the project is to combine technology push with market pull, building technology roadmaps starting from application needs. Following this approach, the General Workshop has involved in a lively dialogue 50 international technology and application experts, coming from about thirty institutions out of eleven countries.

Application Experts presented the scenarios and the requirements for future products while Technology Experts gave an overview of the evolution of the different technologies in the main Nanoelectronics fields. Then, mixed Technology-Applications Groups discussed in parallel sessions the priorities for technology development in order to satisfy the different applications. Finally, the conclusion of this first analysis was reported in a plenary session.

3 Workshop methodology

This first general workshop aimed at collecting the relevant knowledge base pertaining to six application domains and to the technology tasks covered by the NEREID project. About 30 institutions were represented through about 50 participants.

This first general workshop consisted in four sequential sessions lasting one half-day each:

1. Taking stock of future requirements of six large application domains.
2. Scanning the ten project's technology tasks (corresponding work packages 2 to 6) by defining the main figure of merits and enhancing the possible future evolutions (the technology options for the different time horizons).
3. Developing a list of critical points for future investigation by comparing the results from the above two steps. It allowed a preliminary analysis of the relevance of different technologies or possible gaps for the required functions/applications (top-down approach). Other ideas for disruptive applications coming from the technological evolution (bottom-up approach) are planned to be considered in the next steps.
4. Reporting and discussing the outcome in a plenary session, to obtain a comprehensive synthetic understanding of the status of the project and to start the planning of the next steps.

The horizon for all investigations was uniformly structured in short-term (less than 3 years), medium term (up to 7 years) and long-term (beyond 7 years) windows.

4 General outputs of the Workshop

The main outputs of the first NEREID General Workshop are presented in the following sections:

4.1 Application Domains

The first General Workshop included presentations from 6 Application domains, considered to be very important for the European Industry, Economy and Society (see the programme of the Workshop and the invited speakers in Annex):

4.1.1 Internet Of Things

The IoT, the technologies, architectures, and services that connect massive numbers of sensors, enabling uniquely addressable “things” to communicate with each other and transfer data over pervasive networks using Internet protocols, is expected to be the next great technological innovation and business opportunity.

IoT acts as a meta-driver for all other application domains. Several disruptive paradigms are operating. IoT is poised to create many new ecosystems, which bear a disruptive nature.

It is therefore important to capture the transformative power represented by IoT by expanding and exploiting the concept. IoT recaptures the value of previously independent systems and introduces a new collaborative value among them (leading to expended business models). Plus, IoT enables the «smartification» (ambient intelligence) and the analysis (knowledge integration) of everything, from personal applications (wearables, health…), robotics and machines to the local and wider environment, including material objects (vehicles, retail…), energy and derivatives (lighting, smart grid), home, building, farming, industrial systems, city, etc.

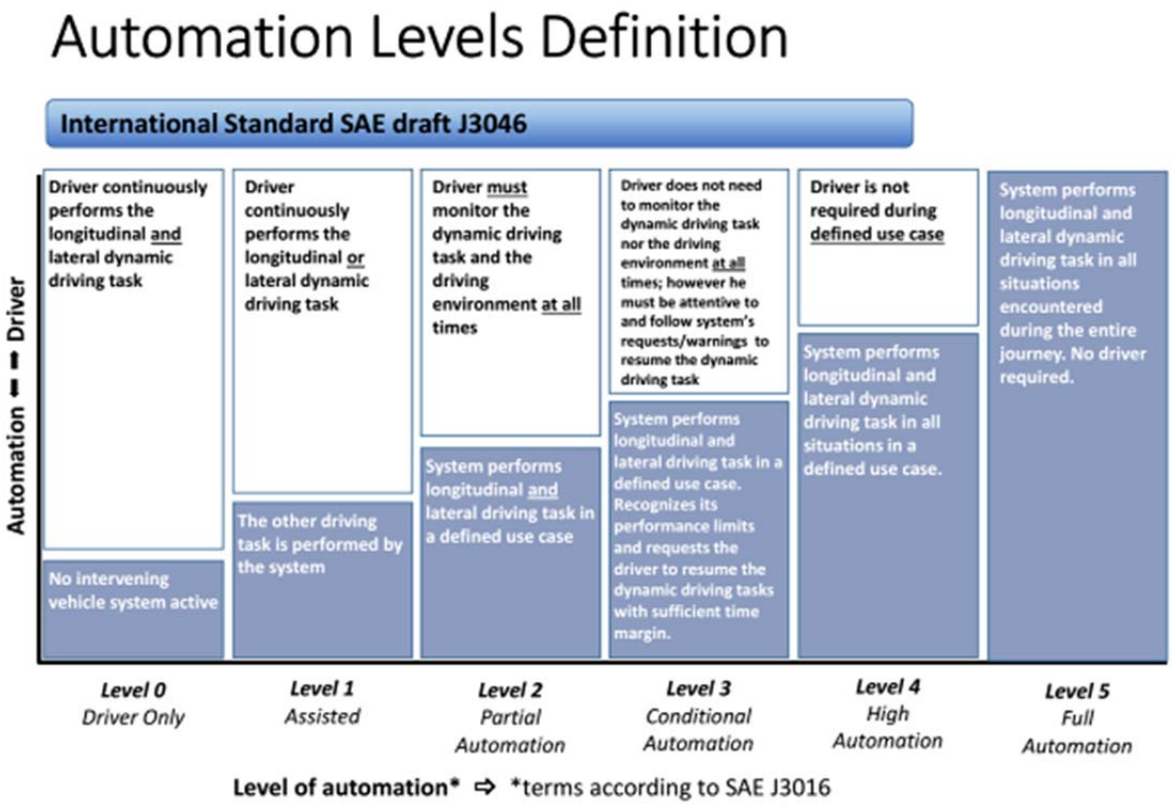
The needs cover the domain of Cyber-Physical System, including physical object and cyber capabilities, in particular in the fields of: Sensors/Actuators, Storage, Programmability, Control, Processing, Connectivity, ID.

The main requirements put forward in this domain are the following:

- Ubiquitous mobile computing, Mobile edge computing, Cloud computing
- Power: for ambient (ultra-low power, wireless, energy scavengers), mobile (wireless, battery constrained) and stationary (wired, heat dissipation constrained), ranging from 100nW to 500 W
- Performance: for ambient, mobile and stationary, ranging from 10 Mop/s to 1 Pop/s
- I/O Bandwidth: for ambient, mobile and stationary, ranging from 1M bits/s to 1T bp/s
- More data per watt: technology (transistor and memory improvements), circuit (e.g. near threshold computing), system (e.g. more on chip memory), architecture (e.g. multi-core, neuromorphic)
- Pervasive sensing
- Miniaturization
- Data/Network trust, security, privacy, safety
- Self-repair (materials, logic…)
- Operation in harsh conditions

4.1.2 Automotive

The automation of driving is the main goal presented in this field, with the following characteristics.



The roadmap is covering key enabling technologies for sensing, system integration and communication architecture, handling of human factors and functional safety.

Further developments are required in the field of electronic components and systems**.**

The new technologies requirements for Smart Systems for automated driving are the following:

- Provide all the features (high resolution and contrast for the camera) guided by safety rules
- Be able to filter, process and evaluate big data, data safety and privacy
- Be transferrable to all vehicle types
- Work in all weather conditions
- Be stable in large temperature ranges
- Be failsafe
- Have a long life-time
- Have a low power
- Have a sufficient computing power
- Have capacity for data storage
- Miniaturization of the functions
- Have redundancy
- Correlate to high quality standards and requirements
- Sensors have to be miniaturized and optimized (cost, resolution, form factor, lifetime…) in order to be able to adapt to future market demands.
- Low cost

4.1.3 Digital Manufacturing

The manufacturing processes implicate all WPs.

Older ‘manufacturability’ notion now evolves into ‘variability’ notion, which entails how systems maintain productivity, reliability, resilience, sustainability.

The main requirements mentioned in this field were:

- High specificity data processing
- Self-configurability
- Nano, Bio, Info, Cognitive requirements
- Energy efficiency
- Virtual modeling and product /process design
- Human centered production systems
- Interconnected planning systems
- Monitoring and control based on sensors and smart control systems
- Automated production processes based on IA and robots
- Predictive and remote maintenance
- Self-learning organization
- Innovative components: miniaturization, energy consumption, computing capabilities (faster), zetabit storage, terahertz clocks,
- New functionalities: sensors (environmental, biological, emotional…), nano-photonics/ communication, biological interfaces, etc.

4.1.4 Medical/Health

The domain of smart health is developing very fast.

The main requirements mentioned in this field were:

- Very low power
- Safety/security
- Miniaturization, weight
- Biocompatibility
- Computing capacity
- Various sensing functionalities (genes, ADN, proteins, chemical species, position and orientation, interaction with ultrasound, interaction with light, 3D surfaces, healthy or pathologic cells)
- Actuation: micro-pumps (drug delivery, micro-nano fluidics for biological samples analysis), movements (micro-robots, nano-particles), surgical tool control
- Energy harvesting (chemical EH…) and storage
- Implanted/absorbed devices (biocompatibility, biodegradability…)
- “Illumination” (smart array of X-ray, ultrasound or magnetic sources)

4.1.5 Security

The presentation focused on the very specific application of Professional Mobile Radio (PMR) narrow band, wide band, and broadband, motivated by network reliability (critical mission),

security and confidentiality. The network size is country wide with few tens thousands of subscribers for Public Safety to single cell with few ten of subscribers for a factory plan.

The main customers are:
- Public Safety for more than 50% of users: Police, Fire Brigades, Search and rescue units, Paramedics/Ambulances
- Armed Forces: Peace keeping soldiers, Military base guardians, Training camps
- Transport Utility Industry: Guardians of airports, harbors and factories, Transportation networks (train, subways).

PMR cell needs to be wider than commercial cell, so higher power with good penetration and propagation properties (i.e. < 1GHz) are used.

The main technological requirements are the following:
- Sensors:
  - 3D Sensors: indoor geo localization
  - Gas – chemical sensors
  - Health sensors
  - Environmental sensors

- Power:
  - Low insertion losses switches
  - Power amplifier efficiency enhancement system
  - 'Spurious free' high efficiency DC-DC converters (buck-boost type)

- Communication:
  - High quality factor tunable resonator (or capacitor/) for filter, oscillator, terminal factory alignment
  - High dynamic low band pass ADC/DAC
  - Highly linear LNA / driver
  - Network security

- Audio:
  - Hand free for group call (power amplifier efficiency and 'spurious free', sound quality improvement system)
  - Covert system

4.1.6 Energy

The needs for the energy of the future are the following: i) GHG emissions, energy costs, reliability and operational safety of energy system, ii) A whole range of nanotechnologies in the energy mix and along the energy chain. Materials, especially nanomaterials, for energy get larger view, iii) Products and services are designed ad-hoc. The energy chain (sourcing, changing, distributing, storing, using) is sequential and irreversible.

The main requirements that have been put forward are in the fields of:

- Photovoltaics (PV): Increase efficiency and lifetime, Storage integrated with PV, autodiagnostic
- Oil & Gas: High temperature components
- Nuclear: High radiation resistant components
- Grid: Wide Bandgap Semiconductors for power electronics (SiC, GaN)
- Smart cities/ buildings: Lighting, Low energy consumption RF devices
- Mobility: Power management devices

- Other devices needed:
- Nanosensors
- Wireless power transmission by lasers, microwaves… based on nanocomponents

4.2 Scientific/Technical WPs and Tasks

All the 10 NEREID Technical Tasks, covering the 5 Scientific and Technical WPs, have been included in the first General Workshop. For each Technical Task the main figures of merit have been defined and the possible future evolution has been sketched as a function of the different time horizons

The comparison of application requirements, coming from the first part of the Workshop with the planned evolution of the different Technology Tasks has produced a list of points for further investigation. A preliminary analysis has been made of the relevance of different technologies and of the possible gaps for the required functions/applications.

4.2.1 WP2 - Beyond CMOS

Task 2.1 Non-conventional information processing approaches and devices

and

Task 2.2 Designs and architectures for non-conventional information processing

The main challenges[5] to capitalise on-going research potentially leading to a technological (r)evolution, defining figures of merits and specifying basic requirements in this domain, include the following:

1. *Considerations of design and architecture at a sufficiently early stage in Beyond CMOS conceptual research*. As information processing is the main objective an essential issue is the approach to input/output physical realisations since it will at a later stage define, among others, the viability of becoming part of circuits and enable developments in design and architecture.

2. *Methodology developments to enable comparison of current and emerging Beyond CMOS concepts and technologies.* In Europe there is a rich conceptual landscape of concepts and emerging technologies, which have the potential to become a viable technology. Some of them are more advanced than others, for example, spintronics, molecular electronics, neuromorphic-oriented memristive devices and 2D layered materials, allowing devices and even circuits being envisaged although not yet systems, while others including, for example, nano-optomechanics, entropy-based computation, thermal computing, valleytronics and topological insulators need a stronger targeted research effort to enable comparison to be made and eventually benchmarking.

3. *Relating cutting-edge level of understanding to regular reality checks*. Three main considerations could become part of this challenge: Is it possible to show that initially the novel information processing device can be tested on a silicon platform? Can viable

[5] C M Sotomayor Torres, J Ahopelto, M W M Graef, A Cappy, G Larrieu, T Swahn, G Wendin, D Winkler, P Grabiec, G Fagas, R Popp and W Rosenstiel, *Beyond CMOS: NANO-TEC project recommendations for research in nanoelectronics*, PHANTOMS Foundation, e-NanoLetters **29**, 15-19, August (2014). Legal deposit BI-2194/2011. http://www.phantomsnet.net/Foundation/Enano_newsletter29.php

operational conditions concerning, for example, temperature and prospects of integration potential be demonstrated? At what stage needs the research to be at to enable statements on speed, key materials, power consumption per unit data, since it may not necessarily be a “traditional bit”, leading further on to statements to assess variability, reliability, integration potential, manufacturability and systemability?

4. *Advancing the research to map application areas of alternative computing paradigms*. Given that there is a wide scope of approaches, it is important to realise that future computation will not necessarily be of the kind “one size fits all” but may be limited to more specific needs to maximise its advantages. Complementary computation paradigms may be envisaged to serve system levels in subsets of application domains. For example, low power but slower computation technologies may be needed for systems operating in local system of environmental monitoring, while faster and more secured systems not necessarily autonomous may be needed in cases of sensitive and expensive data handling needs. Thus, a challenge is to map the landscape of advantages and suitability of problems that can be served by a given computational approach.

The theoretical or experimental gaps requiring more research are in the field of:

- While most of the current Beyond CMOS concepts have, to some degree, been experimentally and theoretically demonstrated, there is an urgent need to develop, e.g., *models, theoretical understanding, experimental techniques and materials* to ascertain ways in which these potentially promising state variable concepts may be useful for information processing.
- *Novel approaches in design and architecture*. Beyond CMOS devices and circuits need new modelling and simulation tools, ranging from physical level modelling of single devices to hardware description language (HDL) to describe a circuit with implementation of a realistic architecture. The desired operation, the performance and sensitivity to parameter variance have to be verified by simulations and supported by experimental characterisation. The simulations of the emerging devices and circuits can be combined with CMOS simulations to study the integration potential on CMOS platforms.
- *Identification of the needs and application fields of individual and or complementary future computation technologies*. This refers to speed, power and operating conditions, among others, which will determine the use of a given future computation technology or combination of some of them to, e.g., harsh environments, autonomous systems and to financial, educational, public health, security or other fields. Each application field has a different hierarchy of key metrics: For some cost is not an issue but security and reliability are paramount, while for others effective power consumption and cost are key factors. Consequently, methods need to be developed to compare the relative advantages and disadvantages of a given alternative computational paradigm, their application area and their research implementation.

4.2.2 WP3 Advanced Logic and Connectivity

T3.1 Nanoscale FET

The main technological evolutions, figures of merits and requirements in this domain for transistors and memories are the following:

1 Transistor scaling (1: further gate length scaling require device architecture evolution to e.g. Gate All Around; 2: transistor specifications become increasingly application specific as a single device and process cannot satisfy requirements for the full range of application; 3: sequential 3D integration becomes a key element for stacking different system components).

2 Nanoscale FET enables further area scaling, further performance improvement, improved frequency, reduced power and cost, allow co-integration of logic, I/O, Memories, analog…

3 Low power transistor technologies can be timeline plotted (FDSOI, FinFET, NW, TFET).

4 High performance transistor technologies can be timeline plotted (FinFET, Nanosheets).

5 Progress axes for non-charge-based memories (PCRAM, RRAM, MRAM) are: improvement of data retention at high temperatures, reduced power consumption, reduced resistance variability.

6 Application requirements: (very) low power energy/autonomy, more data/Watt, data fusion in real time and computing performance, data security, miniaturization, reliability, harsh environmental conditions, (high) T° range, embedded memory capacity, biocompatibility, self-repair, self-configurability and cost.

The theoretical or experimental gaps requiring more research are in the field of:

- High performance/HPC (e.g. ultimate CMOS) or low performance/ Ultra Low Power (e.g. low power for autonomous systems, small slope switches).
- Harsh environment: high T° (automotive, avionics…).
- Cost effective manufacturing.

The coming project domain workshops should deepen bottom-up approach analysis.

T3.2 Connectivity

The main technological evolutions, figures of merits and requirements in this domain are given below.

The main targets in this field are:

I) RF/mmW Wireless technology & design for access & short connections:

- Innovative ultra-low power components for IoT and Machine-to-Machine (M2M) communications
- Handheld devices technologies

II) RF/mmW Wireless & wireline technology & design for infrastructure:

- Highly integrated and cost effective solutions for small cell
- high speed (>10 Gb/s) and cost effective backhaul and front-haul
- Radio over fiber for “last mile” and electro sensitive environment

III) Optical/Photonics technology & design for high speed link:

- Cost effective 40Gb/s to 400 Gb/s silicon photonics enabled solution for data center & cloud computing
- 400 Gb/s system for long haul

Optical/RF components are varied and heterogeneous and systems connectivity is complex and characterized by a multiplicity of alternatives: low/high data rate, short/long distance, fixed/mobile, permanent/reconfigurable, point to point/omnidirectional, occasional/full time, connection with power plant or energy scavengers, always on/wakeup, low quality/high quality

channel, low/high frequency, narrow band/wide band, software/hardware, simple/complex interfaces.

The main technologies which have to be taken into account for future applications are the following: Ultra Low Power Design, RF mmW Wireless technology & design, Quantization & Synthesis in RF Front-Ends, mmW Beyond 200GHz, Antennas & Passives components, Optical Interconnect technology & Design, Reconfigurability, Packaging & 3D Integration, Testability & BIST, Coding, Modulation, Standardization

The Figures of Merits have to be defined at: the block level, the system level, higher-level functionalities.

For RF/mmW the Figure of Merits are at:

1) The block level: LNA, PA, VCO, PLL, Mixer, ADC, DSP
2) The system level : Energy per bit (RX and TX), Energy per useful bit (RX and TX), Total TX efficiency, Sensitivity, Selectivity, In-band blocking resistance, Linearity, Dynamic range, Spectral efficiency and purity, Turn-around time
3) Higher-level functionalities: Multi-standard capability (modulation, datarate, coding), Multi-band RF interfaces, Hardware accelerators (e.g. CRC, data encryption), Multi-level sleep modes, leakage currents and wake-up delays, Transceiver architecture portability vs. CMOS technology scaling, Single-chip vs. heterogeneous technology solution (FEM, µC for protocol stack implementation, application processor), Number of chip I/O, Chip area

For optical/photonics components, the Figures Of Merit (FOMs) are the following:

1) Optical I/O : Packaging (Active/passive/auto-alignment, Coupling Bandwidth, Optical loss, Size), Lasers (Off-chip component interconnects, Opportunities for silicon backend integration)
2) Electronic components : Receive Mode : Trans-Impedance Amplifiers (Gain, Trans Impedance value, Power Efficiency, Bandwidth), Transmit mode : Drivers (Speed, Peak-to-peak voltage range, pJ/bit efficiency)
3) Photonic components : Lasers FoM (Wall Plug Efficiency, Threshold, Frequency and spectral purity-linewidth, Thermal range)
4) Photodiodes : Responsivity, Optical Bandwidth, Electrical Bandwidth
5) Modulators (VCSEL, Mach-Zehnder, Ring) : Direct / Polarization modulation, Electrical & optical Bandwidth, Insertion loss
6) Wavelength Division Multiplexers (WDM) : Max output power per lambda, Max optical power per guide

Because of strong heterogeneity of topics, the Task should be translated into topological space. Applications descriptions should reduce to three dimensions: consumption, data rate, distance range and the issue is to make given technologies fit inside. A critical point is to convert technology criteria into application criteria and vice versa. Research tends to be specified with respect to application domains; Individual players do not seem to look for generic requirements; each application retains its specific roadmap.

For future Domain Workshop, we plan to search for progress in the definition of generic function by gathering several application domains and exploit heterogeneity of optical/RF components further. We also plan to reduce the working area according to European development in research and industry.

4.2.3 WP4 Functional diversification:

It includes two domains, Smart Sensors and Smart Power, with specific technological evolution, figures of merits and requirements.

T4.1 Smart Sensors:

A large diversity of sensors is developed:

- Non-invasive (industrial, wearable, …): Activity sensors, Gas sensors, Particle sensors, Biosensors, Light & radiation sensors, Self powered sensors…
- Implantable in humans: Monitoring, Therapies…

The main characteristics are:

1 Sensors retain close relation to Big Data and software/algorithms.
2 Future sensors are poised to perform multiple functions.
3 Power supply is a ubiquitous notion and power awareness is paramount for applications.
4 The combination of (low) power sensing, computing, communication and energy management is mandatory in smart systems.
5 Energy efficiency per electronic function needs progress.
6 The enabling zero-power approach will be disruptive for efficient future autonomous smart systems
7 The trillions sensors vision by 202x. Sensors are at the intersection of exponential tech progress versus functional diversification.

Sensors have many Figures Of Merit: Sensitivity, Selectivity, Power / sensed bit (sensor + read-out + ADC), CMOS compatibility, Robustness and reliability, failsafe, Packaging, Integration (hybrid, 3D, on flex), Maturity level, Ability to become self-powered, Integration and form factor (applications dependent).

New metrics should be identified for the NEREID roadmap (system level: power efficiency, reliability, size, weight, cost…), More efficient power management devices need to be developed, Sensor fusion

T4.2 Smart Energy:

Smart Energy has the ambition to ensure the European technological capabilities for generating, distributing and consuming electrical energy and for replacing with electrical energy other sources like mechanical, hydraulic or combustion engines.

The Smart Energy Task focus on the definition of the roadmap for technologies, materials, integration methodologies and processes for the realization of more efficient power management devices

The Roadmap is devoted to cover:

- New highly efficient power devices based on wide bandgap gap semiconductor materials, like SiC GaN on Silicon and later Diamond on Silicon or nanowire-based materials, to be investigated together with WP6. Power devices based on wide band-gap semiconductor devices carry a disruptive capacity for applications (power conversion, power circuits, smart

grids, compact convectors, wireless charges, envelope trackers, new topologies with low Qrr and fast switching, high T° operation, high power RF).

- Energy harvesting devices for very low power applications, as required for instance for IoT, including the development of power scavenging technology.
- Power technologies for medium-high power applications as required for e.g. train traction and medium-high voltage power grid
- High temperature capable packaging, serving new materials and 3D technologies with lifetimes fulfilling highest requirements and the integration capabilities for new kind of different interface conditions.

The technological and material issues that need to be solved in order to guarantee a large market penetration of these devices are in the field of: Material (substrates, quality, reproducibility, supply chain, wafer size, maximum thickness for heteroepitaxial growth), Processing issues (contacts, gate, isolation), Normally off operation (hybrid or intrinsic), Isolated gate (MIS) devices, Gate drivers, Sustainable breakdown, Operational (rated) voltage, Robustness (UIS, short circuit), Reliability, Passive components, Packaging (high power, low inductance, cooling, surface mount, ...) .

The classification of power devices is done according to three key parameters: Breakdown voltage, Power handling (max. current), Switching Speed.

The domain of Energy Harvesting could be essential in applications like IoT or Medical/Health applications as mentioned in this report. For this reason a sub-Task "Energy for Autonomous Systems" will be created to cover this area in the Smart Energy domain and experts will be invited in this field for future Domain Workshops.

The key FOMs are:

- Device level: Normally off –Vth > 2V, Low gate leakage at maximum gate voltage, Breakdown Voltage 650 V, 1200 V devices, Ron vs Qg (efficiency vs speed), Dyn RDS,ON < 20% at maximum voltage, Reliability/robustness > 20years, Maximum operating channel temperature.
- System level point of view: Passive components, Packaging (high power, low inductance, cooling, surface mount, ...), Gate drivers, Efficiency, Reliability, Size, Weight, Cost.

4.2.4 WP5 – System design and Heterogeneous integration

T5.1 System design:

The analysis of application requirements for System Design (partially valid also for Heterogeneous Integration has evidenced a few main points:

- In the field of More-than-Moore System Design must face multiple objectives and multiple constraints, differently from traditional More-Moore design constrained only by speed and power consumption.
- HW/SW co-design remains an issue, but solutions can be taken from More-Moore design, Analogue and RF design are already covered (also in ITRS), what is missing is the integration of aspects like sensing and power management, which are common to almost all applications.
- Power management in More-than-Moore Smart Systems, like IoT, must cover several aspects, like:

    - Energy conversion (e.g. dc/dc or ac/dc)
    - Management of energy scavenging solutions
    - Energy supply via integrated batteries or micro fuel cells.
- The system design should cover aspects for power in MtM devices: from one side, software development tools for power management, from the other a way to define specify and verify the power management and its integration in systems (not at gate level)
- Trend in sensor components is the integration of several sensing functions in a single module, together with specialized processing functions for the sensor signals
- In relation to connectivity (task 3.2) a critical need is at system level safety, security and certifications and the main topics in system design can be:
- 1. Specification, code generation & verification for Safe & Secure systems
- 2. Simulation & Certification

In summary, the system must be considered in its complexity, therefore design tools must integrate Power, Sensors, Electronics, Packaging/3D, Wireless/RF, … all in a unique tool.

The selected approach is to generate two different maps, for the two different needs:

- Top-Down, with the important issues to be considered and that will produce as output a Data Package describing the System
- Bottom-Up that is the list of requests to be given to the Tool Vendors, the Manufacturing Companies.

The main FOMs for System Design have been for the moment only identified in terms of generic requirements like:

- Power Aware Design
- System level management of connectivity
- Propagation of Constraints
- Multi Domain Integration
- System Partitioning
- ……

T5.2 Heterogeneous System Integration:

The main technological evolutions, figures of merits and requirements in this domain are the following:

- Performances of the components of smart electronic systems are optimal, when each components is built in a specific proprietary technology;
- Heterogeneous integration can potentially improve time to market and make such systems more affordable to manufacture:
    - Chip on interposer, 3D integration
    - Reliability and characterisation
    - Evaluation of cost models and yield
- System on Chip is normally in Heterogeneous System Integration but this should probably be in the design area. SoC needs many compromises to create a system and it takes a lot of design time and person effort to achieve a system that works first time
- Different applications provide different challenges and design specifications

The **main challenges and FOMs** in this field are:

- Interconnects (stress, thermal, contact resistance, low k, interposers…)
- Packaging (interposers, low k, alignment, cooling…)
- Materials (adhesives, thermal interfaces, moulding compounds …)
- Yield (visualization methods, inspection tools, test and analysis…)
- Passives and devices (RLC, MEMS, sensors, photonics, RF, analog…)

4.2.5 WP6 – Equipment and Manufacturing science

T6.1. Equipment and Materials

and

T6.2. Manufacturing Science

The main technological evolution, figures of merits and requirements in this domain are the following:

Material and equipment issues are present in all WPs.

The selection of topics needs to come from upstream in the supply chain:

- More Moore and/or More than Moore
- Applications
- Chip Sets
- Process Technology, and
- from the European market situation, since part of European equipment industry is linked to out of Europe customers.

There is a need to draw relevant horizontal axes across WPs and tasks that include WP6 topics.

The main areas to be covered are:

- Materials (semiconductors IV, III-V, II-VI, wide bangap, 2D ; high and low k ; piezo-electric ; spin-based ; ferroelectrics, advanced litho, precursors/chemistries ; porous materials ; packaging and bonding)
- Equipment – Process (metrology/characterization, thin film deposition ; litho and patterning ; cleaning and passivation ; …)

5 Conclusions

The first workshop methodology aimed at aligning both application domains and technologies at the same level of attention. These two-day sessions gathered the relevant background knowledge for establishing a common language between the two categories of experts (application and technology).

The process of deriving technology requirements from top application-level needs, as proposed in this first step of the project is based on a linear approach. It could become partly insufficient, due to the speed of change in customer habits and consequently in requirements on one side,

and at the same time the increasing complexity of technologies on the other. Therefore, a part of future applications (killer apps) cannot be foreseen by this methodology. A double unknown situation prevails whereby some future applications are yet unknown and technologies evolve at unprecedented pace, so some of them cannot be easily linked to applications. However, the bottom-up approach, starting from the planned evolution of technologies, could also lead to new ideas of disruptive applications. This last approach is also taken into account in the future steps of NEREID. This knowledge sharing and convergence between application and technology areas could lead to killer apps ideas, which usually result from a market-technology symbiotic vision.

In the conclusion of this Workshop during Session 4, we proposed the following strategy for our future roadmap activities:

- Propose to all Applications Experts to select 2 or 3 major application domains in their area, if possible with quantitative needs for different time horizons (short, medium and long terms)
- Ask the WP and Task Leaders together with Technology Experts to focus on the most promising technological options

In the case of too many possibilities for some Tasks (e.g. Smart Sensing) to cover all the planned applications, we proposed to focus on two applications areas, Automotive and Health, that seem to cover critical requirements for all WPs. For these Tasks, a detailed roadmap will be proposed for the focus applications, but some general/qualitative statements can be derived also for the other applications mentioned in the proposal (Energy, Automotive, Medical/Life science, Security, IoT/Smart connected objects, Mobile convergence, Digital Manufacturing). On the other hand, the other Tasks will be able to cover all the planned application areas with detailed technology roadmap activities (e.g. Nanoscale FET).

These selected applications will be used by technology experts to develop their specific roadmaps in future Domain (Task/WP) Workshops that will be held in the near future. The Planned activities will cover refinement of figure of merits, convergence of technologies and applications, possible gaps for which no solutions can be proposed up to now and where substantial research activities are required, proposal of possible novel disruptive -generic-functions/applications.

The 2nd General Workshop will be organized next year (in Athens on April 6 -7, 2017, at the same place and time as the EUROSOI-ULIS Conference) for presenting the results of this detailed analysis.

6 Annex

6.1 1st General Workshop overall organization

General Workshop Introduction	
NanoElectronics Roadmap for Europe: Identification and Dissemination	Francis Balestra, Grenoble INP
Session 1 (Application domains)	
Trusted IoT - Applications and Technology	Ovidio Vermesan, SINTEF, Oslo
Automotive	Vincenzo Murdocco, FIAT, Torino
Digital Manufacturing - Disruptive Paradigms: Emergences, Adjacencies, etc	Pierre Massotte, I2D, Mauguio
Roadmap for Medical Nanoelectronics	Philippe Cinquin, IMAG, Grenoble
PMR Introduction and Perspectives	Benoit Clement, AIRBUS, Elancourt
Energy	Laurent Thibaudeau, KIC Innoenergy, Grenoble
Session 2 (Work packages/Tasks)	
Introduction to Technology Areas Synthesis by Task Leaders	Enrico Sangiorgi, SINANO Institute
Beyond CMOS - Task 2.1, Task 2.2	Jouni Ahopelto, VTT, Espoo
Nanoscale FET	Anda Mocuta, IMEC, Leuven
Connectivity	Jean-Baptiste David, CEA-LETI, Grenoble
Smart Sensors	Hoël Guerin & Adrian Ionescu, EPFL, Lausanne
Smart Energy	Gaudenzio Meneghesso, IUNET, Padova
System Design	Danilo Demarchi, Politecnico di Torino, Torino
Heterogeneous System Integration	Alan Mathewson, Tyndall, Cork
Equipment and Manufacturing Science	Markus Pfeffer, Fraunhofer IISB, Erlangen
Session 3 - Project Tasks Groups Cross Discussion	
6 groups breakdown [app. domains versus tech. areas]	moderated by Task/WP Leaders
Session 4 - Synthesis (sub-groups reports and plenary discussion)	
Session 4 Introduction	Francis Balestra
Beyond CMOS-Nanoscale FET	Francis Balestra
Connectivity	Jean-Baptiste David
Smart Sensors	Hoël Guerin & Adrian Ionescu
Smart Energy	Gaudenzio Meneghesso
System Design- Heterogenous Integration	Markus Pfeffer
Animation of the Sessions	Patrick Corsi, CayaK-InnoV, Paris & Brussels

6.2 Glossary

2D layered materials: A family of 2-dimensional materials that can be stacked. Examples include graphene, transition metal dichalcogenides, black phosphorous and hexagonal boron nitride. Materials for tunnel FETs, spintronics, valleytronics and for very fast optoelectronic phenomena.

Beyond CMOS: A technology with potential to information processing that is not based on the complementary architecture of p- and n-type MOS transistors.

Entropy computation: A new idea based on stochastic thermodynamics and the dynamic interplay between energy and entropy, showing that local non-equilibrium can be used as resource for information processing.

FDSOI devices: Transistors with a Fully Depleted channel realized on a thin Si film

FinFET Devices: Transistor architecture realized with 3 gates

GAA devices: Transistors with a Gate-All-Around the conduction channel

Molecular electronics: An approach in which organic or biomolecules having a non-linear behaviour/property provide switching and memory elements potential to information processing.

Nano-optomechanics: Exploit the mutual interaction of photons and phonons enabling efficient and fast data transfer, e.g., from fibers, and has potential information processing.

Neuromorphic computing: A system which mimics the behaviour of biological neurons with capability to local decision making and learning.

PCRAM, RRAM and MRAM: Non-charged based Memories, where the information is stored using a variation of resistance instead of charge with Phase Change materials, Resistive materials with a conduction filament, or Magnetic materials.

Spintronics: A technology in which the spin acts as a state variable to carry information, together with a moving charge as an additional degree of freedom or as a spin wave (magnon).

TFET devices: Transistor with a tunnel conduction between source, channel and drain

Topological insulators: 2- or 3-dimensional material in which the bulk of the sample is insulating and the surface contains topologically protected 1-dimensional conducting channels, similar as in quantum Hall effect, but without an external magnetic field and with separate channels for spin-up and spin-down carriers.

Valleytronics: Typical in 2-dimensional materials. Spin polarised carriers populate separated energy minima in the momentum space and this effect can be used to process and store information.
Thermal computing: Temperature gradients (heat) or phonons are use as information carries and in information processing.