WP5 Domain-Workshop on the Challenges for Heterogeneous System Integration

2016/06/14

The **WP5 Domain Workshop** on **"Challenges for Heterogeneous System Integration"** has taken place on **September 16, 2016, 8h30 - 17.30** in Grenoble's World Trade Center [1] in room Cervin. It has been embedded as an associated event [2] into the 6th Electronics System-integration Technology Conference and Exhibition (ESTC [3]) in Grenoble from September 13 - 16, 2016. The Domain Workshop has been organized by Alan Mathewson, Danilo Demarchi and Giorgos Fagas.

Schedule:
Friday, 16
September 2016,
8:30 - 17.30

Location
World Trade Center, [1]
Grenoble, [1]
France

Heterogeneous Integration involves the development of technologies, design tools and methodologies for the integration of disparate and separately manufactured components that provide enhanced system level functionality when connected together. This is central to More-than-Moore technologies for the Internet of Things. This workshop aims at identifying challenging issues in Heterogeneous Integration and discussing the main roadblocks to define a new Roadmap for Heterogeneous System Integration. This is part of the activities of the NEREID Coordination and Support Action entitled 'NanoElectronics Roadmap for Europe: Identification and Dissemination' which was launched at the last European Nanoelectronics Forum in Berlin in December 2015 for a duration of 3 years. The vision of the NEREID project is to elaborate a new roadmap for Nanoelectronics, focused on the requirements of the European semiconductor and applications industries and the main societal challenges that technologies can address. This roadmap will integrate the advanced concepts developed by Research Centers and Universities in order to achieve an early identification of promising novel technologies, covering the R&D needs all along the innovation chain.

The final result of the NEREID activities will be a roadmap for European micro- and nano-electronics across all Technology Readiness Levels and with a clear identification of short, medium and long term objectives. The roadmap will be divided into main technology sectors (More Moore, More than Moore, Beyond-CMOS, Heterogeneous Integration, System design, Equipment and Manufacturing Science) and will include cross-functional enabling domains. In this workshop we will debate the Heterogeneous System Integration chapter of the new European Roadmap.

This common work between technology and application experts will lead to an early identification of the most promising technologies, useful for future research and development activities. The workshop will cover the technological requirements for heterogeneous integration, including an investigation of the different ways in which chips can be assembled inside a package, the chip-to-chip interconnections (TSV or TPV), multilevel interconnection schemes, chip scale partitioning, testing & validation, manufacturability, thermal management and reliability issues. The choice between different technologies largely depends on desired performance parameters (e.g., response time, energy/power, form factor, reconfigurability, security) and a cost/benefit analysis, including systems level reliability and ways of characterising it, will need to be performed.

The NEREID project (ICT-CSA-685559) is supported within the Research and Innovation Programme Horizon 2020 by the EU.

Links:
[1] http://www.congres-wtcgrenoble.com/en
[2] http://www.estc2016.eu/associated-event/
[3] http://www.estc2016.eu